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In-Place Evaluation of Powering and Signaling Within Fan-Out Multiple IC Chip Packaging

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***Abstract*— This article confirms the advantage of fan-out (FO) packaging in the electrical performance of power delivery among integrated circuit (IC) chips with the best use of land side capacitors (LSCs). On-chip in-place waveform measurements quantitatively evaluate the integrity of powering and signaling within FO wafer level packaging (FOWLP) multiple chip module (MCM) demonstrators, where a pair of IC chips are assembled with LSCs with different sizes and structures. The IC chip incorporates an array of 12 digital cores and on-chip waveform monitor (OCM) circuits. Each digital core consists of a low-voltage differential signaling (LVDS) transceiver channel that is backed by a static random access memory (SRAM)-based built-in self test (BIST) module and supplied by an on-chip voltage regulator module (VRM). The LSCs are placed on the bottom side of an FO interposer and inserted between the output of VRM and the ground plane almost ideally with the shortest length of physical traces. A Si membrane capacitor of 10 nF sustains the lowest power line impedance over the frequency range of 2.0 GHz more constantly than a multilayer ceramic counterpart, and attenuates the high-order harmonic frequency components to the clocking frequency at 750 MHz. The leverage of LSCs in powering also improves signaling and helps achieve the wider eye openings in LVDS channels. The implications are elaborated for the capacitor selections with respect to the physical types of capacitors, the size of capacitances, and the level of shares in power delivery among digital cores, all toward the higher level of integrity in powering and signaling in FOWLP MCMs.**

***Index Terms*— Fan-out (FO) packaging, low-voltage differential signaling (LVDS), multichip module, on chip monitoring, power delivery network (PDN), power integrity, power noise, signal integrity, Si capacitor (SiCap).**

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I. Introduction

ADVANCED packaging has evolved to accommodate multiple integrated circuit (IC) chips for unifying various functionality into a system in the form of multiple chips in a module (MCM). The demand is further extended for heterogeneously integrating multiple chiplets that are individually developed using suitable device technologies and supplied by associated semiconductor fabs. 3-D IC chip (3DIC) stacking [1]–[6] and fan-out (FO) wafer level packaging (FOWLP) [7]–[10] technologies have been extensively explored. Both of them fulfill the advanced packaging toward the higher performance and a smaller footprint as well as a lower profile. Stakeholders can share the cost of manufacturing and disperse the risk of investments, even tracking the level of integration under Moore's law that is continuously required by applications. Photonics and electronics integration [11] deploying FOWLP MCM achieves the high data bandwidth in a system where multiple chips of processors, memories, and opto-electronic interfaces are tightly connected. A machine learning device [12] uses FOWLP to unite IC chips for neural-network processing and memory and further exploits 3DIC for a high-density imaging chip to be placed on the top surface [13]. Those applications demand the design of MCM systems to strive for high data bandwidths, stable power supplies, and the maximized power efficiency all around IC chips.

To achieve the goal of system-level performance, the integrity in signaling and powering appears to be a challenge in practically implementing MCM devices with advanced packaging [14]–[18]. Once IC chips are assembled in a package, their power and signal lines are unified horizontally within membranes of an interposer or vertically through the Si substrate of IC chips, and fundamentally inaccessible by external measurement equipment. Chip-package-system board integrated simulation can provide analytical insights of internal states once models are properly prepared for electronic components including IC chips [19]–[21]. Packaging materials are electrically characterized for modeling passive impedance [22], [23]. The simulation concatenates the passive models and active circuits to solve dynamic behaviors of powering and signaling. Here, the accuracy of simulation remains being concerned by designers and needs to be confirmed or even

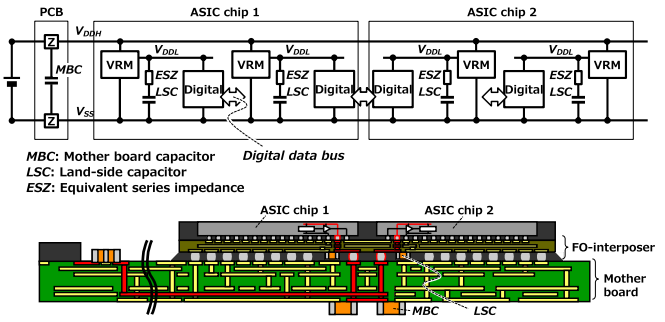


Fig. 1. MCM architecture in schematic (top) and in FO physical structure (bottom).

calibrated by the measurements on test devices with reference structures.

The 3DIC demonstrators have been developed and characterized [14], [24] and referred to the superiority of power noise mitigation and signaling performance. Those are attributed naturally to the construction of 3DIC stacks with vertically distributed capacitors among power delivery networks (PDNs) [25], [26]. The benefits of embedded capacitors in FOWLP devices were also exhibited by monitoring power and signal waveforms [27], [28]. The implications with the different property of interposers have been relevantly discussed with the same device architecture but integrated on a Si passive interposer differently from the fan-out one, which should be referred to [29]. Here, our demonstration was self-explanatory but limited only to qualitative observations in the previous reports, which were insufficient to discuss the selection of capacitors in the design of a PDN.

In this article, the electronic performance of PDN is precisely and quantitatively evaluated in FOWLP devices through on-chip measurements and equivalent circuit simulation. It is shown that the electrical impedance of power delivery can be strategically planned in a fan-out (FO) structure with the best use of land side capacitors (LSCs) with smaller series impedance that benefits from the very short connecting paths in nature to the stacked membranes in an FO structure. The implications of capacitor selections in the design of FOWLP MCM devices are elaborated through the in-place evaluation of power and signal integrity (PI and SI), for the first time.

The rest of this article is organized as follows. Section II describes FOWLP MCM demonstrators and associated experimental setups for in-place power noise and signal waveform measurements. Section III evaluates the electrical performance of powering and signaling and then discusses the design strategy of FOWLP MCMs with LSC selections. Section IV concisely provides conclusions.

II. FOWLP MCM Demonstrator

A. MCM Architecture

The MCM architecture of Fig. 1 is exemplified with two application-specific IC (ASIC) chips having multiple digital cores and being encapsulated in FO assembly. This architecture is intended for the PI and SI evaluation of a typical digital IC chip. An external high supply voltage, V_{DDH}, is converted by a voltage regulator module (VRM) into the local supply voltage V_{DDL} for digital circuits in each power domain. Digital signals are communicated over a chip-to-chip digital data bus using physical layer signaling schemes such as low-voltage differential signaling (LVDS). The electrical performance of PDNs fundamentally influences PI and SI, where a designer needs to carefully choose and locate capacitors throughout the physical structure of system-level FO assembly.

The chips are faced down on the FO interposer and their bumps on pads are connected to the wires patterned over metal layers in the interposer. The entire MCM in a ball-grid array (BGA) is then mounted on a mother printed circuit board (PCB). The LSCs are mounted in the backside of the MCM with the shortest length of physical traces to the associated pads of an IC chip. In addition, mother board capacitors (MBCs) are mounted on the PCB at multiple locations of the system-level PDN for decoupling.

B. MCM Demonstrator With Test IC Chip

We have prepared FO MCM demonstrators for the present study. The block diagram is given in Fig. 2(a). The demonstrator consists of the tile of digital cores involving LVDS channels with transmitter (Tx) and receiver (Rx) circuits, and static random access memory (SRAM)-based built-in self test (BIST) logic core circuits, all supplied by a dedicated VRM. In addition, the on-chip waveform monitoring (OCM) circuits are equipped for in-place PI and SI evaluation among the digital cores.

The VRM down converts the external voltage of 3.3 V into the internal digital core voltage of 1.8 V, which is locally stabilized by the dedicated capacitor, LSC.

The Tx drives the outgoing differential signals. The Rx vice versa receives and converts the incoming differential ones to the rectangular signal of bit streaming. The BIST core circuits of Fig. 2(b) continuously check the consistency between incoming received data (RXDATA) and expected data prestored in SRAM at the rate of received data clock (RXCLK). The number of inconsistent bits is counted in a bitwise way and then read by an external checker as the data bit error rate (BER).

The OCM circuits includes probing front end (PFE) modules for sensing individual analog voltage signals at respective probe inputs and a data processing unit (DPU) for digitizing voltage waveforms after a multiplexer (MUX) [29], [30]. The PFE module of OCM system, Fig. 2(c), senses V_{SIG} by a source follower (SF), and immediately compares its output voltage to the reference one, V_{REF}, by a latched comparator (LC) at the strobe timing T_{STRB}. External voltage and timing generators provide V_{REF} and T_{STRB}, respectively. The SF internally provides an offset dc voltage to V_{SIG} in order to match the input voltage range of the LC. This allows the PFE to effectively capture the V_{SIG} of interest in a rail-to-rail voltage range, namely, from the ground voltage to the power supply voltage. The single bit stream from the comparator is given to MUX. The probe selection is set through on-chip registers. The waveform data acquisitions are fully controlled by the software running on an off-chip computer (PC).

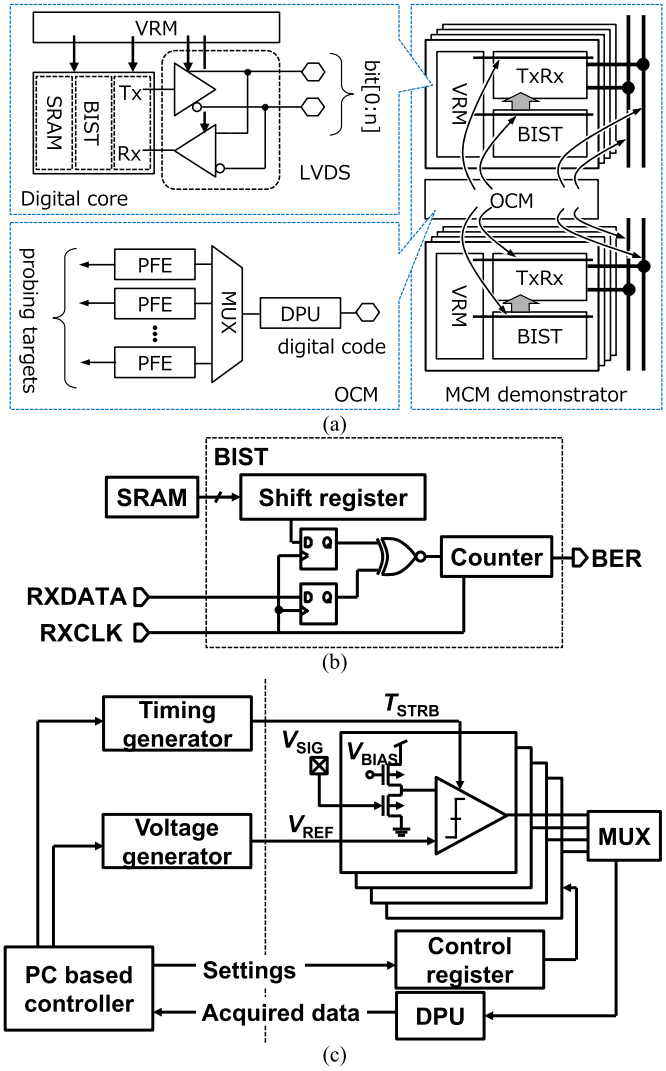


Fig. 2. Block diagrams of (a) MCM demonstrator, (b) BIST core circuit, and (c) OCM system.

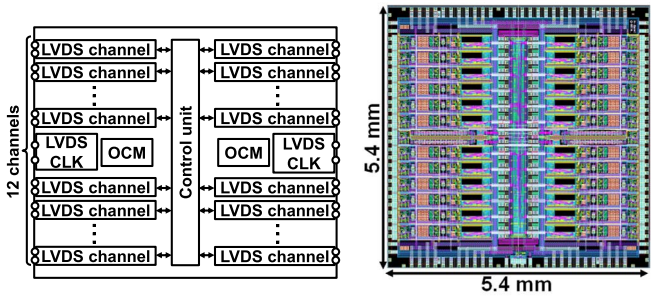


Fig. 3. Test chip overview. (a) Block diagram. (b) Chip layout.

The digital cores, represented by LVDS transceiver channels, are integrated on a silicon prototype chip shown in Fig. 3. Each left and right side of the chip holds 12 LVDS data channels that are managed by a central control unit. Another LVDS clock channel receives and drives the clock (CLK) signal that is shared by the data channels over multiple chips for synchronization. The chip has the area size of 5.4 mm × 5.4 mm and uses a 0.18-m standard CMOS technology.

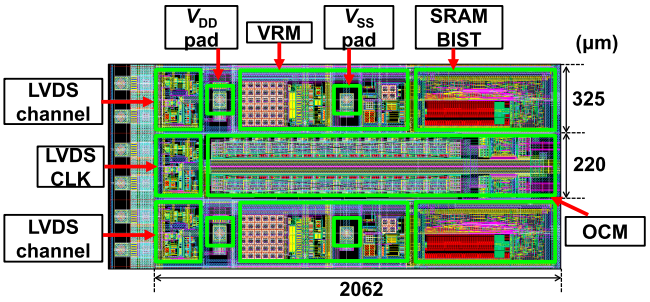


Fig. 4. Physical layout view of LVDS channels featured by in-place waveform capturing [27].

An in-place power and signal waveform capturing macro is realized with OCM circuits and aligned to adjacent LVDS channels in their physical layout, as shown in Fig. 4. The macro has the total of 20 PFE modules uniformly arrayed in two sides and associated probe wirings drawn to the nearest points of interest within respective LVDS channels. These points to capture waveforms include the plus and minus nodes of signaling, power supply, and ground nodes around SRAM and BIST digital cores as well as the output of VRM. There are pads for bumps to be connected to membrane metallic traces on the FO interposer for LVDS channels and CLK signals as well as V_{DD} and ground (V_{SS}).

C. MCM Demonstrator With Capacitors

The block diagrams of MCM demonstrators are given in Fig. 5. The identical chips are horizontally placed in a face-to-face way and the 12 data and one clock LVDS channels are one-to-one connected. We prepare two configurations in power delivery for exploring the effect of capacitors. The exploratory version of Fig. 5(a), where a single on-board power converter supplies every circuit in the MCM with the support of MBCs while on-chip VRMs are fully cut off and bypassed. In contrast, the main version of Fig. 5(b) utilizes on-chip VRMs locally powering circuits among the LVDS channels. The OCM circuits are powered by the dedicated PDNs and isolated from LVDS channels, in both versions.

We have manufactured the MCM demonstrators with nine different variations of electrical parameters, as listed in Table I, including the exploratory versions [see Fig. 5(a)] without and with LSC, and the main versions [see Fig. 5(b)] with different physical structures and sizes of LSCs. The main versions have some other variations where more than one LVDS channels are bundled and powered by a single VRM selected from the bundle, where the other VRMs are turned off. The LSCs are chosen from the structures of multilayer ceramic capacitor (MLCC) and Si capacitor (SiCap). The electrical parameters in Table II highlight the properties of MLCC and SiCap. The electrical series resistor (ESR) and inductor (ESL) are derived at the self-resonance frequency (F_{res}) and represented at the frequency of 1 GHz, respectively. The dielectric constant (Dk) and dissipation factor (Df) are assumed to be 4.4 and 0.02, respectively, in our FO interposer. These numbers are used in the simulation of electrical impedance in Section III.

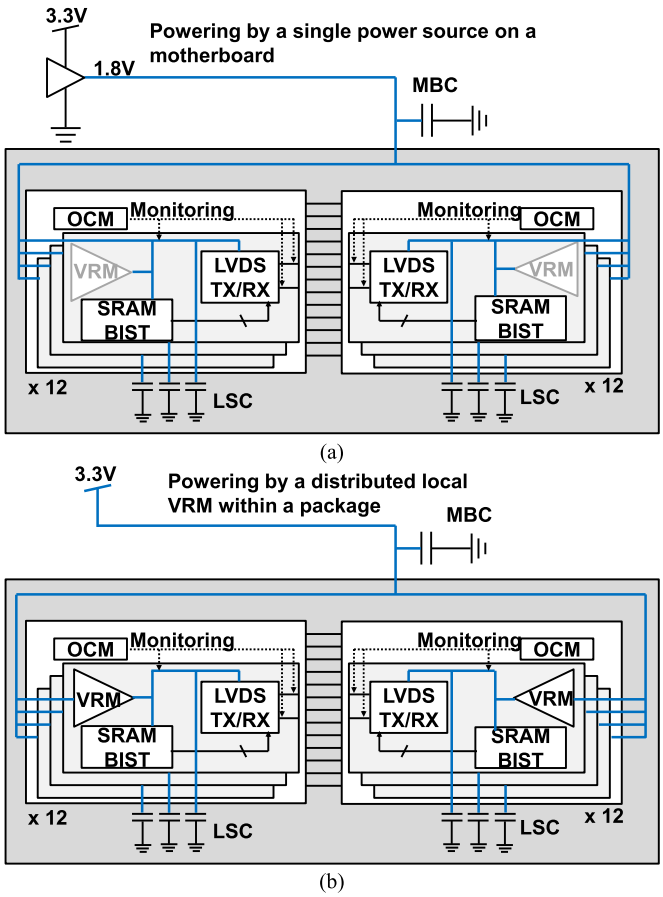


Fig. 5. Block diagram of demonstrators with different powering schemes. (a) Exploratory and (b) main versions.

TABLE I

MCM DEMONSTRATOR VARIATIONS. EXPLORATORY (EXP.) AND MAIN VERSIONS FOLLOW PDN CONFIGURATION IN FIG. 5(A) AND (B), RESPECTIVELY

MCM demonstrator	Number of channels / VRM	LSC type	LSC size (nF)	PDN configuration
#1	--	No cap.	--	Exp. (Fig. 5a)
#2	--	MLCC	1	Exp. (Fig. 5a)
#3	6	MLCC	10	Main (Fig. 5b)
#4	6	SiCap	10	Main (Fig. 5b)
#5	1	No Cap	--	Main (Fig. 5b)
#6	1	MLCC	3.9	Main (Fig. 5b)
#7	1	MLCC	10	Main (Fig. 5b)
#8	3	MLCC	3.9	Main (Fig. 5b)
#9	1	MLCC	1	Main (Fig. 5b)

The top and cross section views of the manufactured FOWLP MCM are shown in Fig. 6. The ASIC chips are faced down on the FO interposer while being attached to an alumina plate on the die backside [see Fig. 6(a)]. The MCM module has the external area size of 12.0 mm × 6.0 mm and the height of 1.45 mm excluding the ball diameter of nominally 50 μm. The space between ASIC chips is around 0.2 mm. Three membrane layers are, respectively, patterned for metal wirings and formed in the interposer [see Fig. 6(b)], with each thickness of 4 μm, for the following purposes; Layer 1: the pads to be connected to the bumps of ASIC chips and associated power and signal

TABLE II

LSC ELECTRICAL PARAMETERS.

MCM demonstrator	LSC type	LSC size (nF)	ESR*1 (Ohm)	ESL*2 (nH)
#3	MLCC	10	0.12	0.37
#4	SiCap	10	0.28	0.16

*1at F_{res} *2at 1 GHz

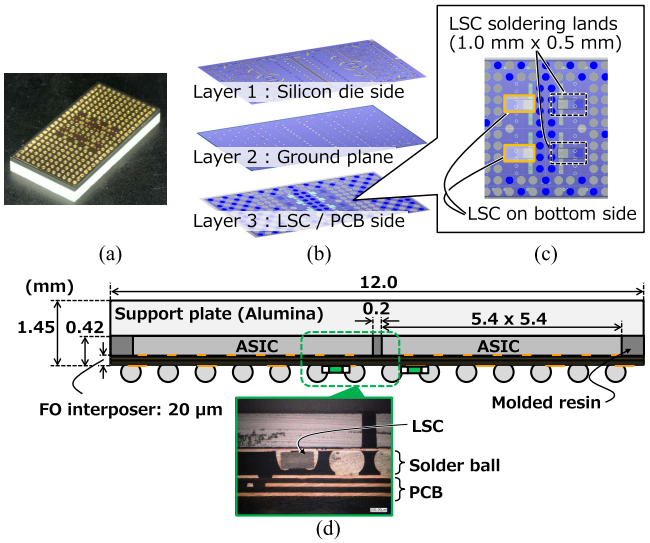


Fig. 6. MCM demonstrator in FOWLP (a) top view, (b) FO membrane layers' image, (c) LSC soldering location on bottom side, and (d) cross section view.

lines, Layer 2: the whole areas dedicated to the ground plane, and Layer 3: the lands to mount LSCs and the pads for balls connecting to PCB, respectively. The total thickness of the interposer is approximately 20 μm.

The LSCs are soldered on the bottom side of the FO interposer with the lands customized to fit the external size of the capacitors. The footprint of LSC shown in Fig. 6(c) is 1.0 mm × 0.5 mm for the MCM demonstrators #3 and #4. The LSC is mounted on the bottom side of the interposer and finely concealed within the ball diameter [see Fig. 6(d)]. This allows the die pad of VRM output to be located in the almost same place of the land to LSC and minimizes the physical length of power supply trace, which is 0.83 mm including metal routings and balls. The other land of LSC is connected to the ground plane of the interposer with the physical trace length of 0.95 mm. In comparison, the length from the power pad of IC chips to the land of MBC becomes as large as 3.39 mm that is mostly dominated by the metal routings on the mother PCB with the total height of 1.57 mm, in the MCM demonstrator #1 for direct powering without VRM [see Fig. 5(a)].

D. Experimental Setup

The whole experimental setup shown in Fig. 7 is fully automated, according to the measurement sequence of Fig. 8. A photo is also given and shows its compactness. The field-programmable gate array (FPGA) device intermediates the transactions between the software on PC and the MCM demonstrator as well as the generators of V_{REF} and T_{STRB}.

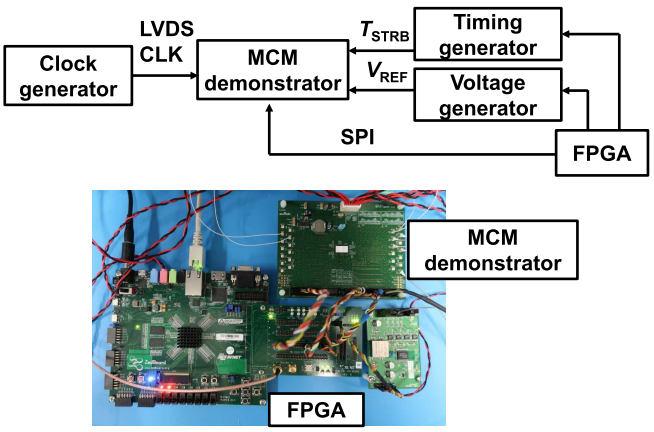


Fig. 7. Experimental setup.

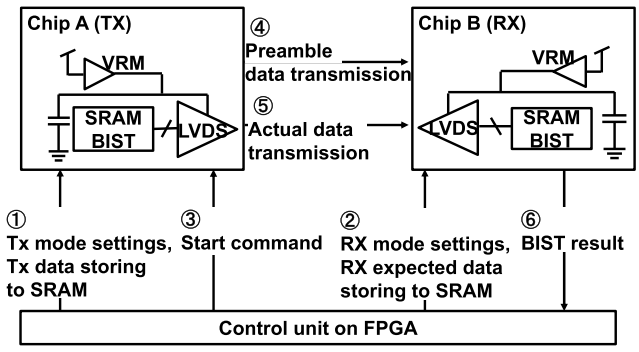


Fig. 8. Experimental measurement sequence.

An external clock generator provides the system clock through LVDS CLK channel.

There are several registers for commanding measurements in the sequence (1, 2, 3, and 6 in Fig. 8), which are written and read between the demonstrator and FPGA through serial-parallel interface (SPI). The OCM probe selections are similarly led by additional registers in the analog power domain dedicated to the OCM system. Data bits are prestored to the SRAM core on one of the chips that is set in Tx mode. The same data are also stored to the other one in Rx mode for BIST operation. Once the sequence is triggered, the data transmission starts with preambles and then repeats with the prestored data. The BIST results are also collected. The waveform acquisition by the OCM proceeds in parallel, where T_{STRB} to sample the voltage waveform of interest moves incrementally forward with the time step of ΔT in every iteration of the transmission. In contrast, V_{REF} in the voltage comparison also increases with the increment of ΔV to search the nearest voltage. In the present setup, ΔV and ΔT are set to be 100 μV and 100 ps, respectively, which determine the resolution of waveform capturing. The waveform acquisition algorithm associated with the OCM circuits has been explored [30], [31] and utilized for the in-place waveform-based evaluation of undesired noise coupling in automotive IC chips [32], [33]. Here, our MCM demonstrator adopts this technique in a customized way to evaluate the powering and signaling within the FO interposer featuring stacked membrane layers and proximate LSCs.

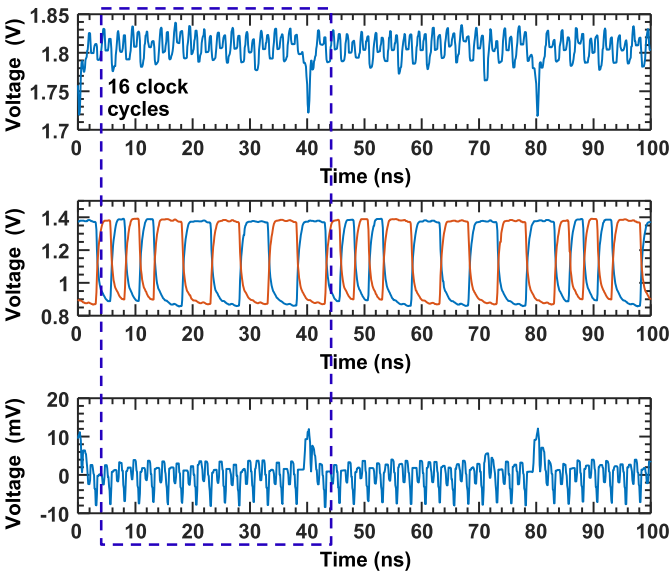


Fig. 9. On-chip power supply and signal waveforms during LVDS data transmission [27].

III. Experiments

A. On-Chip Captured Waveforms

The waveforms in-place captured on the power supply (V_{DD}), differential signaling ($V_{\mathrm{SIG+}}$, $V_{\mathrm{SIG-}}$), and ground (V_{SS}) nodes are exemplified in Fig. 9. The all 12 LVDS channels are synchronously transmitting 16-bit (2-byte) data of "1010110011001100" with the LVDS CLK frequency at 400 MHz. One of the LVDS channels adjacent to the on-chip waveform acquisition macro is measured. The powering nodes exhibit the periodic voltage variations of roughly 40 mV and 10 mV for V_{DD} and V_{SS}, respectively, that are regularly seen with the interval of 1.25 ns due to the power current consumption of logic circuits at either rise or fall edge of clocking. There is an additional large drop in every 16 clock cycles, according to the access to SRAM cores for reading 2-byte data to send (in Tx side) or to compare (in Rx side). The simultaneous occurrence of drops among V_{DD} and V_{SS} is the natural consequence of power current flowing in the core PDN. The differential signaling also exhibits clear transitions associated with the bit sequence. The vertical axes are calibrated in advance with regard to the offset voltage and voltage gain.

The power supply waveforms are compared in Fig. 10 on the individual V_{DD} nodes of the two chips in Tx and Rx operation modes, respectively, within the MCM demonstrator (#3). The LVDS channels operate at 750 MHz, which is the highest operating frequency with no erroneous bit found in the BIST outputs over the time of OCM waveform measurements. The higher level of voltage peaks is seen in the Tx than in the Rx mode, since the Tx circuits drive signal lines between the chips over interposer laminates. The Rx circuits receives the incoming signals regenerate digital data under the presence of power noise. We focus on the Rx mode in the following measurements.

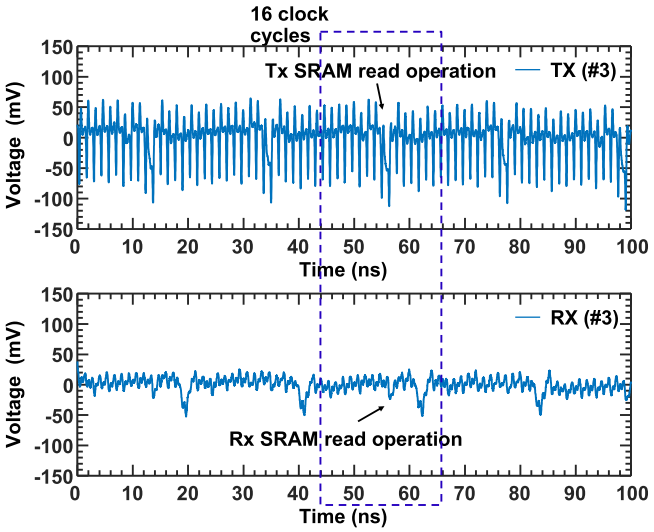


Fig. 10. Power noise waveforms in Tx and Rx operation.

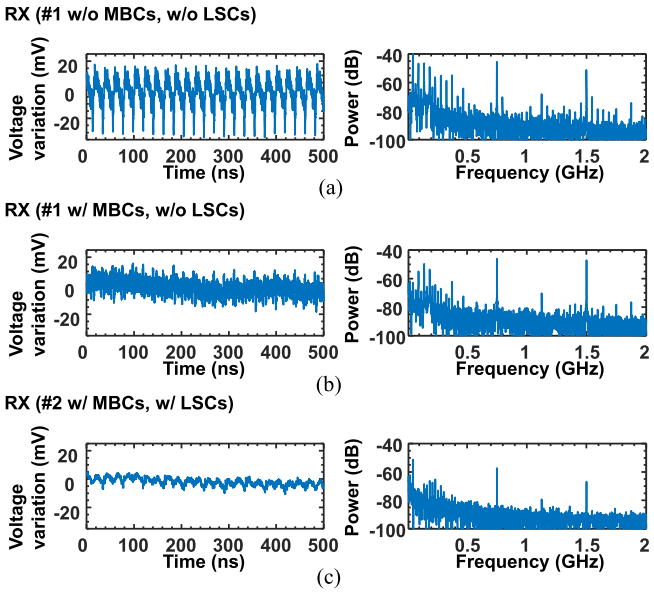
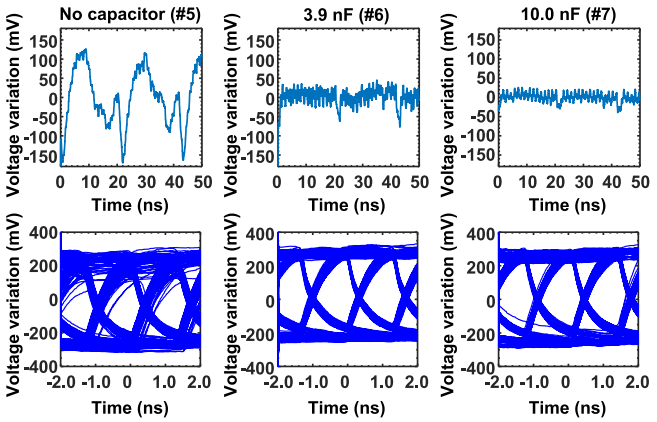


Fig. 11. Power noise suppression by capacitors. (a) No capacitor, (b) with MBCs, and (c) with MBCs and LSCs.

B. Power and Signal Integrity

The power supply voltage variations are compared among the MCM demonstrators with different capacitor configurations, as shown in Fig. 11. The MCM demonstrator (#1, #2) in the exploratory version [see Fig. 5(a)] is tested in the different combinations of with and without MBCs and LSCs. The frequency–domain analysis results are also plotted, which are in general dominated mainly by the 1st and 2nd harmonic components of the clock frequency at 750 MHz. While the demonstrator without any PDN capacitors gives the largest voltage variations in the frequency below 750 MHz [see Fig. 11(a)], the variations become slightly attenuated if MBCs with the total capacitance of 1.2 μF are provided on the PCB [see Fig. 11(b)]. The power supply voltage becomes very much stabilized with LSCs [see Fig. 11(c)], which is explained by the proximate position of LSCs to the source of power current consumption among LVDS channels.



	#5	#6	#7
Eye length (mV)	295.7	376.2	382.0
Eye widths (ns)	0.96	1.16	1.15
Jitter (ns)	0.39	0.19	0.18

Fig. 12. Power noise waveforms and signal eye diagrams.

The effect of LSC is further examined in Fig. 12 for powering and signaling among the MCM demonstrators (#5, #6, and #7) in the main version [see Fig. 5(b)] using VRMs. The waveforms in the Rx mode are captured on the internal V_{DD} pad as the output of VRM to be connected to LSC and also the signal pads of V_{SIG+} and V_{SIG-}. While the power supply voltage variation is more attenuated with the larger size of LSC capacitors, synchronously, the signaling eye diagram becomes clearer. The size of eye openings as well as the time width of jitters are summarized in the table.

The VRM makes the PDN of LVS channel isolated from the other PDNs and also decoupled from the on-board part of power delivery. The LSC becomes the necessary part for an on-chip VRM to suppress power noise spikes in its isolated power domain.

The voltage variations on the V_{DD} pad as the output of VRM are compared with those on the other V_{DD} node located nearby the BIST circuits, for the frequency–domain components of Fig. 13. Both nodes have the relative distance of approximately 900 μm in the physical layout of LVDS channel (see Fig. 4). The magnitude of frequency components becomes large in the distant location from the output terminal of VRM, roughly from +3 to +6 dB over the frequency range of 2.0 GHz. We have also simulated the series impedance on the power line from the land of LSC to the pad in the LVDS channel for the same frequency range. There is a consistency between the larger series impedance and the higher magnitude of frequency components in the voltage variation. The proximate placement of LSCs is suggested for the superior noise attenuation and the better signal quality.

C. Design Exploration

The selection of capacitor physical types is explored with the waveforms on the V_{DD} pad as the output of VRM when the LVDS channels operate at 100 MHz. The frequency components are compared between the MCM demonstrators (#3 and #4) in the main version with MLCC and SiCap of equally 10 nF, as shown in Fig. 14 for the frequency range

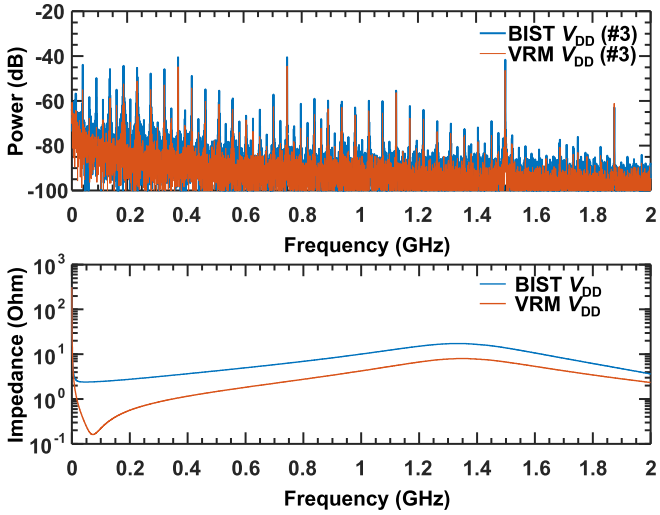


Fig. 13. Comparison of power noise components at VRM (top). Power line impedance is also shown by simulation (bottom).

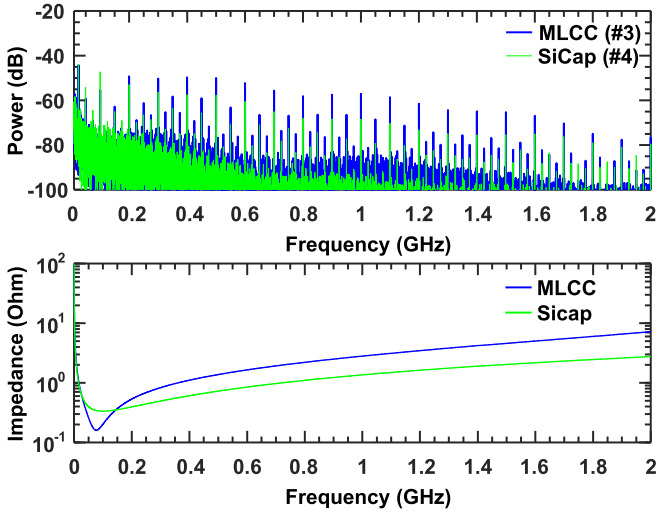


Fig. 14. Comparison of MLCC and SiCap for power noise suppression (top). The clocking frequency is fixed at 100 MHz. Power line impedance is also shown by simulation (bottom).

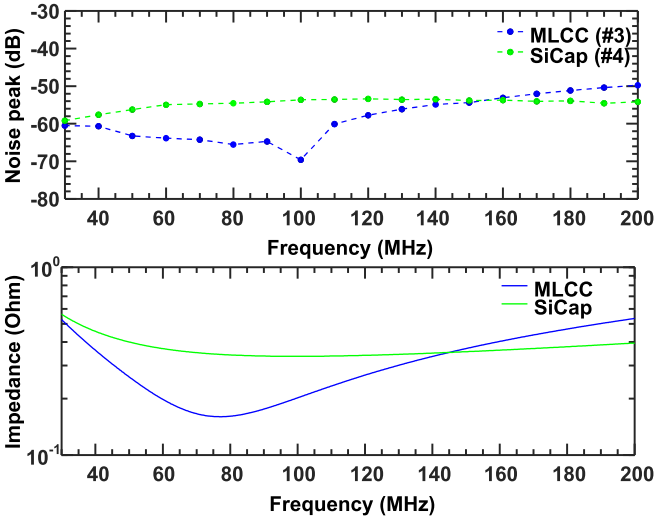


Fig. 15. Comparison of MLCC and SiCap for power noise suppression at different operating frequencies (top). The largest frequency components at 2× of clocking frequency are plotted. Power line impedance is also shown by simulation (bottom).

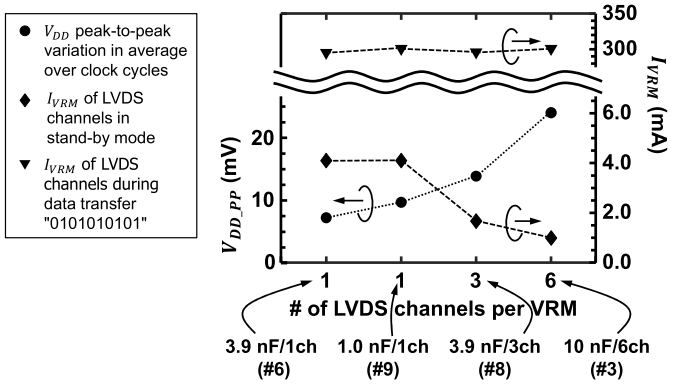


Fig. 16. Comparison of power noise and power current for different number of LVDS channels per VRM.

of 2.0 GHz. The power line impedance is also simulated with equivalent circuits. It is clearly observed that the power voltage variations follow the impedance trends of respective capacitor types. The smaller electronic series inductance (ESL) inherently to SiCap provides the continuous attenuation in a broad frequency range, while the smallest impedance gives the highest suppression by MLCC but only within the spot frequency of its resonance.

The follow-up measurements are executed in Fig. 15 where the LVDS channels operate at different frequencies from 15 to 100 MHz. The largest frequency components, which are often seen at the twice clocking frequency owing to rise and fall transitions, are compared among MLCC and SiCap types. The obvious trends again confirm the influence of the wide frequency impedance, ESZ, parasitic to capacitors.

The impact of the number of LVDS channels powered by a single VRM is investigated in Fig. 16, where the in-place waveforms on the V_{DD} pad as the output of VRM are evaluated. The peak-to-peak voltage variation is averaged over clock cycles and denoted as V_{DD_PP}, during the data transmission among 12 LVDS channels at 750 MHz with the largest bit activities of "0101010101010101." The V_{DD_PP} is minimized if every LVDS channel is powered by its dedicated VRM, where a single LSC is also exclusively prepared. The smaller V_{DD_PP} is observed for the larger capacitance if we compare #6 and #9. The V_{DD_PP} enlarges with the number of LVDS channels that share a single VRM and an associated LSC, where the capacitance per an LVDS channel is chosen to be roughly equal to the order of 1 nF among the demonstrators (#3, #8, and #9). The V_{DD_PP} becomes roughly 2.5 times larger in #3 than in #9. Here, the tradeoff needs to be taken into account between the power integrity and power consumption. The total power supply current among VRMs, I_{VRM}, is also measured in Fig. 16 (on the right axis) and compared among the demonstrators. The quiescent I_{VRM} simply increases with the number of VRMs when LVDS channels are all in the stand-by mode (no data transmission). In contrast, the I_{VRM} becomes almost constant accordingly to bit activities, independently of the number of channels supplied by the single VRM (with sufficient power current capacity).

It is reasonable to share a single VRM by some LVDS channels in low-power applications often provided with intermittent operation modes. In contrast, a per-channel VRM with dedicated LSCs is preferable to prioritize the power and signal integrity in high-performance data storage and server applications, where data transmission is active almost all the time. We think that the demonstrator #3 represents the one best point of design explorations with the power noise reduction, power current consumption, the number of components, and associated footprints [see Fig. 6(c)].

IV. Conclusion

Powering and signaling among digital cores were in-place evaluated by using OCM circuits within MCM integration in FOWLP assembly. The digital cores in a system-on-chip integration were represented by the array of multichannel LVDS transceivers with SRAM-based BIST functionality for chip-to-chip data communication.

Power and signal waveforms were not observable from the outside of IC chips in flip-chip assembly, which excluded the quantitative measurements of the electronic performance of PDN. This problem was solved by the construction of MCM demonstrators in this article.

The superiority of power noise suppression is proven in FOWLP thanks to the LSC proximately placed at the output of VRM and the immediate bottom side of FO interposer, providing the shortest length of physical power delivery traces. This benefits clearly from the selection of lower equivalent series impedance (ESZ) capacitors. These implications came only from the given in-place evaluation with the support of equivalent circuit simulation and were elaborated for the careful capacitor selections and placements in the design of FOWLP MCMs toward the higher level of PI and SI.

It is quantitatively shown that the leverage of LSCs in the FO PDN well suppresses power voltage variations in the wide frequency range of 2.0 GHz when LVDS channels operate at 750 MHz. This also improves signaling with the wider eye openings in LVDS. The SiCap of 10 nF sustains the effectiveness over the full frequency range, and better than MLCC overall, due to low ESR and ESL to the capacitor itself and also to the membrane wirings on an FO interposer. The attenuation was confirmed even for the high order harmonic components up to 20th to the clock frequency at 100 MHz, as well as that for the primary frequency components at various clock frequencies up to 100 MHz. The equivalent circuit simulation supports the results.

Further explorations beyond our experiments in this article will be pursued for the co-design flow of PDN on FOWLP MCM devices among the circuits on a chip, structures in the FO interposer, and the selection and placement of discrete electronic components. The equivalent circuit simulation needs to be more capable of handling all the components and to be desirably calibrated with physical test vehicles.

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