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Density functional theory study on the effect of NO annealing for SiC(0001) surface with atomic-scale steps

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The effect of NO annealing on the electronic structures of the 4H-SiC(0001)/SiO_2 interface with atomic-scale steps is investigated. The characteristic behavior of conduction band edge (CBE) states is strongly affected by the atomic configurations in the SiO_2 and the step structure, resulting in the discontinuity of the CBE states at the step edges, which prevents electrons from penetrating from the source to drain and decreases the mobile free-electron density. We found that the behavior of the CBE states becomes independent from the atomic configuration of the SiO_2 and the density of the discontinuities is reduced after NO annealing. © 2024 The Author(s). Published on behalf of The Japan Society of Applied Physics by IOP Publishing Ltd

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SiC is a technologically important material for future power electronic devices for MOSFETs.[1–4] However, the high channel resistance of SiC-MOSFETs limits their performance.[5,6] This high resistance is expected to be attributed to the low field-effect mobility in SiC-MOSFETs, which is much lower than the ideal electron mobility (~1000 $cm^2V^{-1}s^{-1}$).[7] *n*-type MOSs, in which the inversion layers are composed by the conduction band edge (CBE) states, are more commonly used than *p*-type MOSs in the SiC-MOSFETs. The behavior of the CBE states of a SiC bulk is similar to that of free-electrons, which are the so-called "floating states",[8] and sensitive to the local atomic structure at the interface.[9] In practical devices, off-oriented 4H-SiC(0001) surfaces by 4 degrees are widely used and thus the SiC-MOS intrinsically possesses atomic-scale step and terrace structures, even for the atomically flat surfaces.[10] Furthermore, it has been reported that thermal oxidation causes atomic-scale roughness even on the oriented 4H-SiC (0001) surfaces,[11] suggesting that atomic-scale steps also exist on the terrace at the SiO_2/SiC interface. Atomic-scale steps affect the behavior of the electrons of the floating states, as well as the electronic structures of the interface over a wide area of the interface. By interface nitridation by post-oxidation annealing with nitric oxide (NO),[12,13] one can increase the maximum field-effect mobility from 1-7 $cm^2V^{-1}s^{-1}$[14] to 25-40 $cm^2V^{-1}s^{-1}$ for 4H-SiC(0001) MOSFETs.[15–17] Field-effect mobility is extracted under the assumption that the mobile electron density is uniquely determined by the oxide film capacitance, and thus does not properly reflect electron mobility. Hatakeyama et al. reported that the electron Hall mobility is not increased by NO annealing; on the other hand, the mobile free-electron density increases and the increase in field-effect mobility is due to the increase in mobile free-electron density.[18] In addition, the side effects of NO annealing are reported; the inserted N atoms become a source of interface defects[19] and/or cause negative bias instability.[20] Although a lot of efforts have been made thus far, the microscopic information of the effect of NO annealing on a decrease of channel resistance of the SiC-MOSFET with atomic-scale steps is not fully clear.

In this paper, we investigate the effect of NO annealing on the increase of mobile free-electron density of the SiC(0001)/SiO_2 interface using the density functional theory (DFT) calculations.[21] It is found that the CBE states are affected by the Coulomb interaction of the O atoms in the SiO_2 region, which results in the discontinuity of the inversion layers at the step edge under the gate bias. Since the discontinuities of the inversion layers markedly prevent the electrons from conducting from the source to the drain, the mobile free-electron density is decreased. After annealing, the inserted nitrided layers screen the Coulomb interaction of the O atoms in the SiO_2 region, the behavior of the CBE states becomes independent from the atomic configuration of the SiO_2 region, and the density of the spatial discontinuities of the inversion layer decreases. These results suggest that the nitrided layers inserted by NO annealing make the inversion layers continuous by screening the Coulomb interaction of the O atoms in the SiO_2 regions so that the mobile free-electron density increases.

We perform the DFT calculation for the electronic structures of 4H-SiC(0001)/SiO_2 interfaces with atomic-scale steps and compare the local densities of states (LDOSs) before and after NO annealing. As an example, we show the computational models where the trench structure models are employed to imitate the step model as shown in Fig. 1. Since most of SiO_2 in the SiC(0001)/SiO_2 interface is amorphous as shown by a scanning transmission electron microscopy (STEM) image,[22] it is not straightforward to characterize the interface atomic structure. Here, we assume the crystalline atomic structures that can exist locally at the SiC(0001)/SiO_2 interface and employ the interface atomic structures proposed in our previous study on the basis of STEM images.[22] Our model contains a crystalline substrate with seven SiC bilayers (17.5 Å thick) connected without any coordination defects to a crystalline SiO_2 region with a thickness of 8.2 Å for the upper terrace. In a 4H-SiC bulk, SiC bilayers are stacked on the quasi-cubic (*k*) and hexagonal (*h*) sites alternatively along the [0001] direction. For the SiO_2 side, the computational models where the 4H-SiC(0001) bilayer faces the one-hold or three-hold structure of SiO_2,

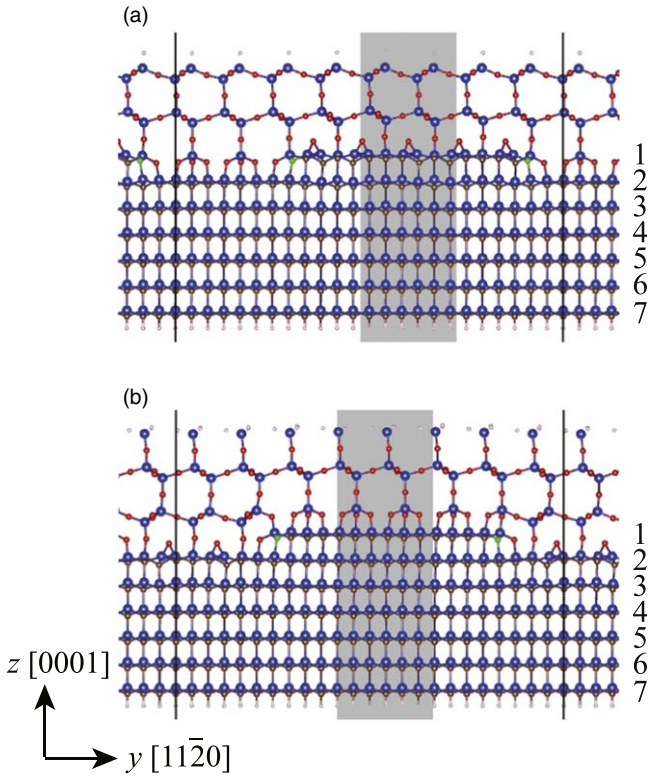

Fig. 1. Interface atomic structure with steps for (a) k1/h3 (h1/k3) and (b) k3/h1 (h3/k1) models. Green, blue, red, and white balls represent N, Si, C, and O atoms, respectively. Black lines are the boundaries of supercells. The LDOS in the shaded area is calculated. The numbers written on the right-hand-side of the atomic structures are the indices of the atomic layers counted from the upper terrace.

where the Si atoms at the interface of the SiO_2 region are connected to the Si atoms in the SiC substrate via one or three O atoms, respectively, are proposed.[22] The interface model, where the atoms in the *k* site of the 4H-SiC(0001) bilayer face the one-hold SiO_2 structure, is referred to as the k1 model. The other interface models are also similarly named the k3, h1, and h3 models.

For the interfaces with steps, following the STEM image,[22] the step terrace structures where the step edge is aligned parallel to the [1$\bar{1}$00] direction are employed. When the upper terrace of the 4H-SiC(0001) bilayer is at the *h* site, the lower terrace is always at the *k* site. In addition, when the SiO_2 layer at the upper terrace has the three-hold structure, that at the lower terrace has the one-hold structure. To terminate the dangling bonds, the C atoms at the step edges are replaced with N atoms. The interface model with steps, in which the k1 and h3 interfaces are the upper and lower terraces, respectively, is named the k1/h3 model. The other interface models with steps are similarly referred to as the k3/h1, h1/k3, and h3/k1 models.

The RSPACE code,[23–25] which uses the real-space finite-difference approach[26] for the DFT,[21] is employed. The periodic boundary condition is imposed on all the directions. The supercell size for the interface with steps is $5.33 \times 36.96 \times 40.44$ Å^3 and a vacuum gap of 14.1 Å thickness separates the slabs. The back side is flattened at the atomic level and the dangling bonds at the top surface of the SiO_2 layer and the bottom surface of the SiC substrate are terminated by H atoms. Integration over the Brillouin zone is performed using a $6 \times 1 \times 1$ k-point grid including Γ point. The grid spacing in real space is taken to be sufficiently small, $0.18 \times 0.19 \times 0.18$ Å^3, so that the discreteness of the grid points does not affect the interface atomic and electronic structures. The exchange-correlation functional is treated within the local density approximation.[27] The projector-augmented wave method[28] is adopted to describe the electron–ion interaction. We implement structural optimization until all the force components decrease to below 0.05 eV Å^{-1}, whereas the atomic coordinates of the SiC bilayer in the bottom layer and the H atoms terminating C dangling bonds are fixed during the structural optimization.

The LDOS is calculated as

$$\rho(z, E) = \Sigma_{i,k} \iint |\Psi_{i,k}(x, y, z)|^2 dxdy \times Ne^{-\alpha(E-\epsilon_{i,k})^2} \Delta_k,$$

where $\epsilon_{i,k}$ is the eigenvalue of the wavefunction $\Psi_{i,k}$ with indexes i and k denoting the eigenstate and the k-point, respectively, z is the coordinate of the plane where the LDOS is plotted, Δ_k is an areal element in the two-dimensional Brillouin zone, and $N(=\sqrt{\frac{\alpha}{\pi}} \cdot \frac{1}{N_k})$ is the normalization factor with α as the smearing factor and N_k as the number of k-points in the Brillouin zone. Here, α is set to 16.4 eV^{-2} so as not to reflect the discreteness of the k points on the LDOSs and not to deteriorate the distribution of eigenstates.

The second column of Table I shows the topmost interfacial SiC bilayer where the CBE states appear for the flat interfaces. As reported in our previous papers,[9,22] the CBE states are absent at the first interfacial SiC bilayer when the first bilayer is the *k* site. On the other hand, when the first interfacial bilayer is the *h* site, the CBE states are absent at the first and second interfacial bilayers in the h1 model, whereas they lie at the first interfacial bilayer in the h3 model.[9] Matsushita et al. reported that the behavior of the electrons in the CBE states is similar to that of free-electrons, which are called the floating states. 4H-SiC bulks consist of tetrahedrons surrounded by Si atoms and those by C atoms. The electrostatic potential in the Si tetrahedrons is lower than that in the C tetrahedrons because of the difference in electron negativity between the Si and C atoms. The Si and C tetrahedrons spatially overlap at the *k* site, whereas they are separated at the *h* site, resulting in the formation of the floating states in the Si tetrahedrons at the *h* site.[8] Since O atoms bridge the Si atoms of the first interfacial bilayer in the h1 model, the electron negativity of the O atoms increases the Coulomb potential at the first interfacial bilayer, resulting in the increase in energy of the floating states.[22] The CBE states do not appear at the second interfacial bilayer because the second interfacial bilayer is the *k* site in the h1 model; the

Table I. Position of the topmost interfacial SiC bilayer where CBE states lie.

Model	Flat (before annealing)	Model	Step (before annealing)	Step (after annealing)
k1	2	k1/h3	2	4
k3	2	k3/h1	4	4
h1	3	h1/k3	3	5
h3	1	h3/k1	3	5

topmost SiC bilayer where the CBE states appear is the third bilayer. The partial charge densities of the flat interface are also shown in the supplementary data, which are consistent with the conclusion derived by the LDOSs.

We show in Fig. 1 the computational models for the interface with steps. Since the atomic structures of the *k* and *h* sites appear the same when they are seen from the $[1\bar{1}00]$ direction, only the k1/h3 and k3/h1 models are illustrated. Figure 2 shows the LDOS of the upper terrace of the interface with steps. The regions where the LDOS is integrated are indicated by the shaded rectangle in Fig. 1. The positions of the topmost interfacial SiC bilayers of the CBE states are listed in the fourth column of Table I. In the k1/h3 (h1/k3) model [Fig. 2(a) [Fig. 2(c)]], the position of the topmost interfacial SiC bilayer at the upper terrace is the same as that in the k1 (h1) model. Interestingly, the CBE states are absent at the second and third (the first and second) interfacial SiC bilayers in the k3/h1 (h3/k1) model [Fig. 2(b) [Fig. 2(d)]], whereas they appear at the flat interface. The partial charge density listed in the supplementary data also gives the same results. Owing to the finite size effect along the direction parallel to the interface at the step edge, the energy of the floating states increases. This result indicates that the positions of the topmost layer of the CBE states are strongly affected by the atomic configuration of the SiO_2 region, i.e., one-hold or three-hold structure, as well as the site of the SiC surface at the step edges. As shown by the partial charge density in the supplementary data, this result is unaffected when the dangling bonds at the step edges remain. Since the finite size effect appears more significantly at the step edge, i.e. the end of the terrace, than at the middle of the terrace, we have assured that the CBE states do not appear on the upper terrace even in the area separated from the step edge by more than 10 Å. Since the terrace length of the single atom step is ca $36(=l/\tan\theta)$ Å in the substrate with the off angle θ of 4 degrees and interlayer distance l of 2.51 Å, the effect of the step edge is not negligible.

The SiO_2/SiC(0001) structure is usually fabricated on an off-oriented substrate and the atomic-scale single steps of the SiC substrate at the interface are observed by STEM. When the gate bias is applied, inversion layers are formed by the CBE states at the interface. Since SiO_2 at thermally oxide SiC-MOS is usually amorphous, the atomic configuration of the SiO_2 region changes on the same terrace and the one-hold and three-hold structures coexist at the same terrace in some cases. The inversion layers formed by the CBE states are spatially separated and discontinuous at the step edges in the h1/k3 model. The electrons trapped at the discontinuous inversion layers are immobile, as shown in Fig. 3(a), resulting in the low mobile free-electron density at the interface.[17] In addition, since the behavior of the CBE states is sensitively affected by the interface atomic structure, the electron Hall mobility of SiC-MOS is low.[29] Therefore, the channel resistance, which is the inverse of the product of the electron Hall mobility and the mobile free-electron density, increases.

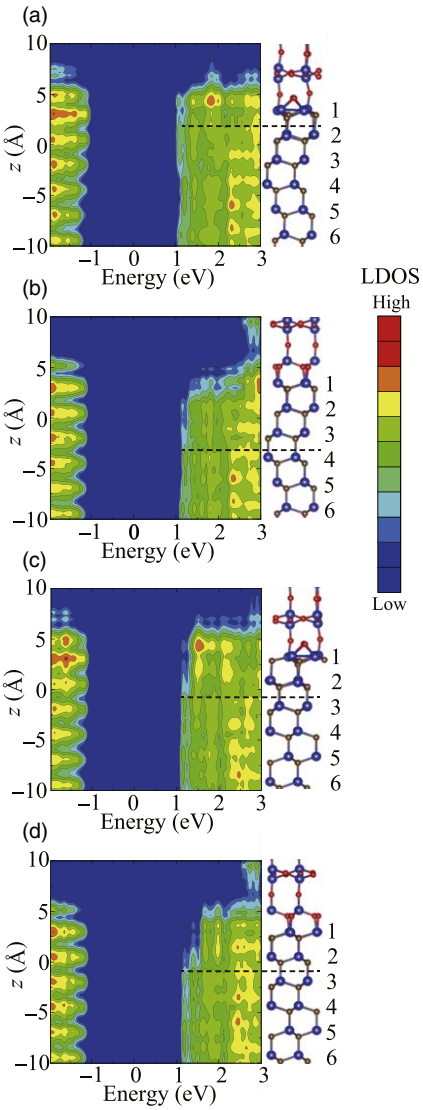

Fig. 2. LDOSs of interface with steps before annealing for (a) k1/h3, (b) k3/h1, (c) h1/k3, and (d) h3/k1 models. Zero energy is chosen as the Fermi level. Each contour represents twice or half the density of the adjacent contours, and the lowest contour is 6.94×10^{-4} electrons/spin/eV/Å. LDOSs in the shaded area in Fig. 1 are calculated. Atomic structures are illustrated as a visual aid and the numbers written on the right-hand-side of the atomic structures are the indices of the atomic layers counted from the upper terrace. The dashed lines indicate the position of the topmost interfacial SiC bilayer.

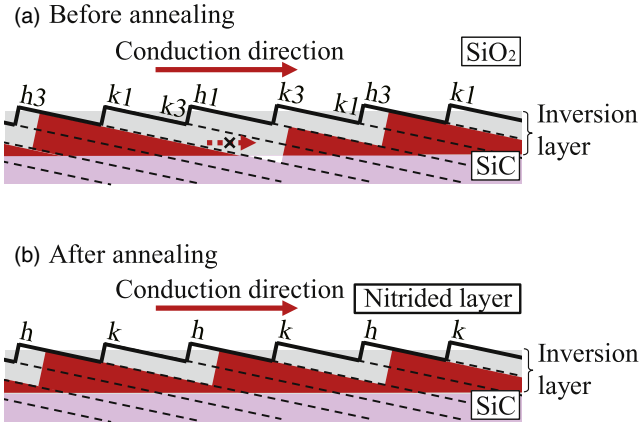

Fig. 3. Schematic of electron conduction at interfaces (a) before and (b) after annealing. The gray shaded areas indicate the inversion layers. The red and pink areas are the spatial distributions of the floating states below and above the Fermi level under the gate bias, respectively. The CBE states are absent on the upper terrace in the vicinity of the step edge due to the finite-size effect.

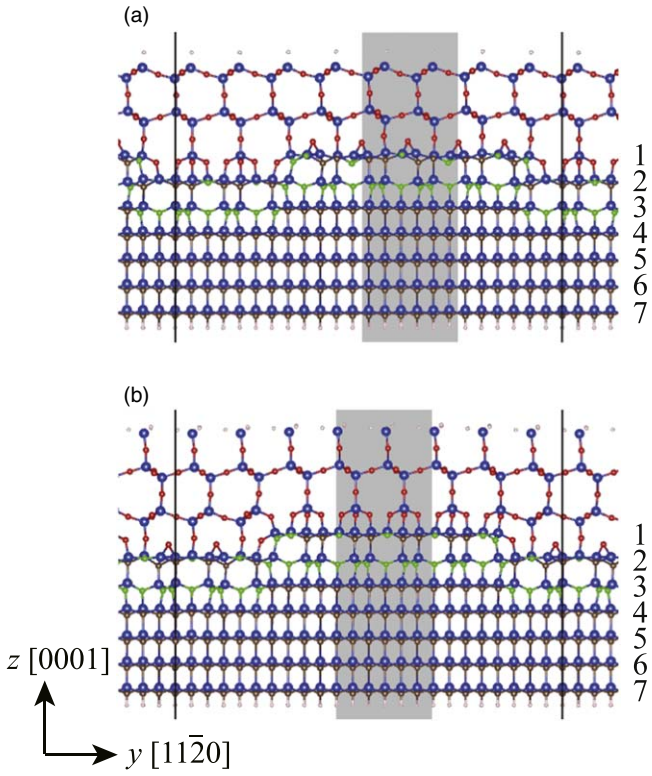

Fig. 4. Atomic structure of the interface with steps after insertion of nitrided layer for (a) k1/h3 (h1/k3) and (b) k3/h1 (h3/k1) models. The meanings of the symbols are the same as those in Fig. 1.

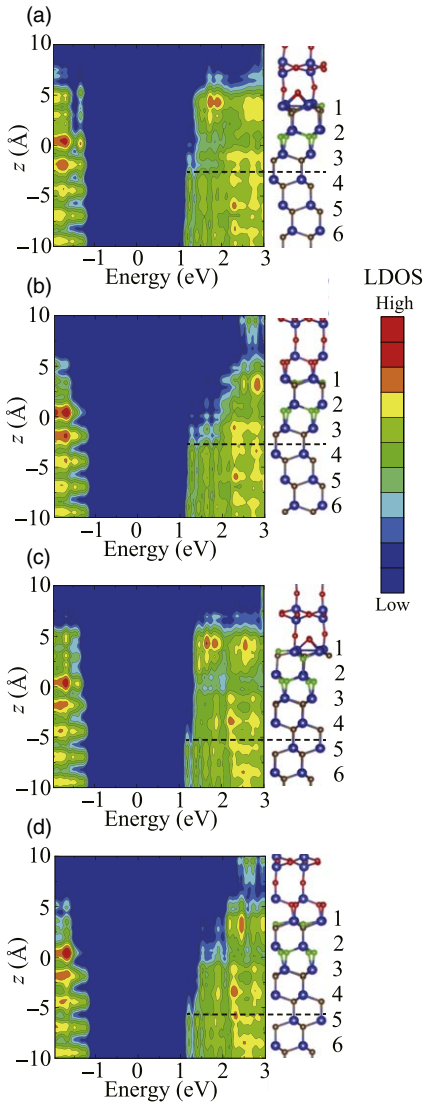

Fig. 5. LDOSs of the interface with steps after annealing for (a) k1/h3, (b) k3/h1, (c) h1/k3, and (d) h3/k1 models. LDOSs in the shaded area in Fig. 4 are calculated. The meanings of the other symbols are the same as those in Fig. 2.

Next, the electronic structure of the interface with steps after NO annealing is investigated. The computational models for the interfaces with steps after NO annealing are shown in Fig. 4. Shirasawa et al. proposed a model of the N-annealed 6H-SiC(0001)/SiO_2 interface, which constitutes epitaxially stacked SiO_2 and Si_3N_2 monolayer SiC.[30] To set up a similar structure for the nitrided layers, four C atoms adjacent to a Si vacancy are replaced by N atoms. The interface structures have been proposed in our previous paper[31] and the areal N atom density of 1.2×10^{15} atoms/cm^2 corresponds to that observed in experiments.[32,33] We have also reported that the insertion of the nitrided layers is an exothermic reaction and the nitrided layers are preferentially formed immediately below the SiO_2 region.[34] We plot in Fig. 5 the LDOS of the interface with steps after NO annealing and show the positions of the topmost interfacial SiC bilayers of the CBE states in the fifth column of Table I. Note that the indices of the topmost bilayers are added two to those before NO annealing due to the insertion of the nitrided layers in the k1/h3, h1/k3, and h3/k1 models. On the other hand, the topmost bilayer is the same in the k3/h1 model, because the bilayers in which the CBE states are absent are nitrided. These results also agree with those obtained by the partial charge density in the supplementary data. The CBE states appear at the fourth (fifth) interfacial SiC bilayer in the k1/h3 and k3/h1 (h1/k3 and h3/k1) models, indicating that the atomic configuration of the SiO_2 region does not affect the position of the topmost layer of the CBE states. The Coulomb interaction of the O atom in the SiO_2 region on the floating states of SiC is screened by inserting the nitrided layer. Because the effect from the O atom in the SiO_2 region on the floating states is suppressed, the inversion layers become continuous, as shown in Fig. 3(b). Some immobile electrons become mobile free-electrons by removing the discontinuities of the inversion layer at the step edges, where the electrons can hardly penetrate, resulting in the decrease in channel resistance.[17] On the other hand, the nitrided layers do not improve the electron Hall mobility; because the insertion of the nitrided layers is not uniform at the practical MOS interface, the small deviations of the behavior of the electrons in the CBE states as well as the interface defects remain. The scatterings at the deviations decrease the electron Hall mobility. It is intuitive that the density of these discontinuities is low in the oriented (0001) interfaces because the atomic configurations of the SiO_2 region are significantly changed between the upper and lower terraces in the vicinity of the atomic-scale step. Thus, the investigation of oriented (0001) interfaces without NO annealing is in progress.

We have investigated the effect of NO annealing on the electronic structures of the 4H-SiC(0001)/SiO_2 interfaces with steps by the DFT calculations. In the experiments, the mobile free-electron density of SiC-MOSs is increased by NO annealing, whereas the increase in electron Hall mobility is

negligible. Our results indicate that the CBE states are absent below the upper terrace in some models before NO annealing owing to the finite-size effect and the Coulomb interaction of the O atom in the SiO_2 region, resulting in the discontinuities of the inversion layers under the gate bias. The discontinuities seriously prevent the electrons from penetrating along the channel direction and decrease the mobile free-electron density. On the other hand, when NO annealing is performed, the effect of the atomic configuration of the SiO_2 region is screened by the nitrided layer and the density of the discontinuities in the inversion layers is reduced. Since the spatial deviation of the behavior of the CBE states due to the disorder of the atomic structure at the interface cannot be eliminated completely, the electron Hall mobility remains low. Thus, the increase in the mobile free-electron density by NO annealing reduces the channel resistance, which is the inverse of the product of the electron Hall mobility and the mobile free-electron density. Since the density of the atomic-scale steps, which are one of the sources of the discontinuities of the inversion layers, is low in the oriented (0001) interfaces, these results will also aid future work in determining the channel resistance of SiC-MOSFETs using the oriented (0001) substrates without NO annealing.

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Authors' contributions

M.U. and N.F. contributed equally to this work.

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