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Liu, Shiqiang
Dong, Guiyi
Mishima, Tomokazu
Lai, Ching-Ming

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# Over 98% Efficiency SiC-MOSFET based Four-Phase Interleaved Bidirectional DC-DC Converter Featuring Wide-Range Voltage Ratio

Shiqiang Liu, *Student Member, IEEE,* Guiyi Dong, *Student Member, IEEE,*
Tomokazu Mishima, *Senior Member, IEEE* and Ching-Ming Lai, *Senior Member, IEEE*

***Abstract*—A novel floating four-phase interleaved charge-pump bidirectional dc-dc converter (F4P-ICPBDC) with wide Buck/Boost voltage ratio is proposed in this article. The interleaved structure is employed to mitigate the current ripple across the low-voltage side capacitor and inductors, while the floating configuration facilitates the high Buck/Boost voltage conversion ratio. To ensure a balanced average inductor current throughout the entire range of duty cycle, a cost-effective asymmetric duty limit control strategy is implemented. In addition, bidirectional synchronous rectification operations are seamlessly carried out without the need for additional hardware, thereby enhancing the overall converter efficiency. Furthermore, the full operating principles, device stresses, current ripple characteristics, as well as parameters design guideline of the converter are illustrated. Finally, A 1kW-50kHz prototype, utilizing SiC-MOSFETs, is developed to validate the wide Buck/Boost voltage ratio of the proposed converter between the constant low-voltage side (72 V) and the adjustable high-voltage side (400-800 V). The maximum efficiencies of the converter are recorded as 98.3% in the Buck mode and 97.6% in the Boost mode, respectively. Experimental results validate the feasibility and the efficacy of the proposed converter.**

***Index Terms*—Asymmetrical duty limit control (A-DLC), bidirectional dc-dc converter, charge-pump, floating interleaved topology, synchronous rectification (SR), wide buck / boost voltage ratio.**

## I. Introduction

Nowadays, the escalating issue of greenhouse gas emissions, a significant factor to climate change, has emerged as a formidable challenge. To mitigate this issue, one solution being promoted is the use of electric vehicles (EVs) [1], which are equipped with rechargeable batteries offering the capability of serving as mobile electricity storage units [2]. This feature positions EVs as potential auxiliary sources of electricity, addressing additional demand and forming the foundation for vehicle-to-grid (V2G) and vehicle-to-anything (V2X) technologies [3]–[7]. Researchers are now exploring into the possibility of utilizing EV-connected dc-microgrids (EV-DCMGs) as a backup power source [8]–[10].

S. Liu, G. Dong and T. Mishima are with Div. of Marine Technologies and Engineering, Faculty of Oceanology, Kobe University, Hyogo, Japan (e-mail: mishima@maritime.kobe-u.ac.jp).

C.-M. Lai, the corresponding author, is with the Department of Electrical Engineering, National Chung Hsing University, Taichung, Taiwan (e-mail: pecmlai@dragon.nchu.edu.tw).

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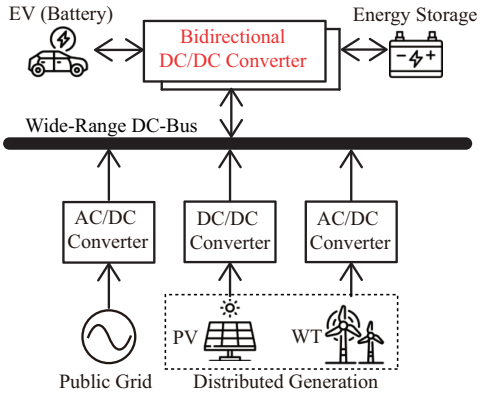



Fig. 1. System architecture of EV-connected dc-microgrid.

The architecture of an EV-DCMGs system is illustrated in Fig. 1. The bidirectional dc-dc converter (BDC) emerges as a significant unit for interfacing dc energy sources, such as EV battery packs or energy storage units, with the dc-bus. The typical dc-bus voltage is 400 V or higher [11], while the battery voltage of EVs usually ranges from 400 V to 800 V. On the other hand, energy storage systems' voltage often varies from tens of volts to tens of kilovolts. Therefore, BDCs with a wide voltage conversion ratio are essential for directly interfacing with the energy storage systems and EV batteries [12]–[15]. In particular, a high voltage ratio is also crucial for efficient energy utilization and power conversion in EV-DCMGs systems.

The BDCs are primarily categorized into isolated and non-isolated types. Isolated converters, such as flyback and full bridge, achieve substantial voltage ratio by modifying the turns ratio of high-frequency transformer (HF-X). However, the leakage inductance of HF-X can inherently cause high voltage spikes on power devices. To address this technical issue, circuit topologies such as full bridge BDCs with a flyback snubber circuit or an active clamp circuit have been proposed [16], [17]. These methods facilitate recycling of energy from the leakage inductor, but request for additional auxiliary components. In addition, misalignment between input and output voltages and the transformer's turns ratio can significantly increase switching losses due to increase of reactive power [18].

Nonisolated converters encompass conventional buck/boost, coupled inductor, switched capacitor and multilevel convert-

ers [19], [20]. Coupled inductor converters, capable of high voltage ratio through turns ratio adjustment, still face challenges with leakage inductance [21]. The multilevel converters, offering high voltage ratio and low voltage stress on power semiconductors, require more components and complex control strategies. Conventional buck-boost converters are efficient and cost-effective for low-voltage applications while suffer from limitations in a voltage conversion range and high voltage stress, making them unsuitable for energy storage applications [22]. Due to interleaved dc-dc converter topologies can reduce the inductor current ripple, enhance power rating, and improve overall efficiency, thus it is widely adopted in dc-dc applications [23]. For bidirectional power conversion, two-phase interleaved buck/boost converters have been extensively studied. However, these converters have limited voltage ratio and are suitable only for scenarios where the input and output voltages do not change significantly. Switched capacitor converter structures, known for their simplicity and scalability, transfer energy of capacitors via different charging and discharging paths to achieve high voltage ratio [24]–[26]. To reduce the input current ripple, interleaved switched capacitor converters have been proposed. The converter in [27] achieved high voltage ratio through dual-stage cascading while incurred high voltage stresses, which will increase the switching losses and reduce the conversion efficiency. In addition, it can only achieve the inductor currents balance when the duty cycles are equal to 0.5. In [28], an interleaved technique was used to smooth low voltage side current ripple. However, the low voltage side current ripple is sensitive to the number of interleaved phases and the duty cycle of active switches. In addition, its achievable voltage conversion ratio is narrower than that of the existing topologies. A bidirectional converter with zero current ripple cell and an auxiliary capacitor cell was proposed in [29]. While the reported converter exhibits low current ripple, its relatively high device voltage stresses and moderate voltage conversion ratio make it less suitable for high-voltage EV battery systems. In [30], the converter adopts a three-phase interleaved cascade structure with switched capacitor cells to achieve low voltage stresses across power switches. However, due to the cascaded configurations of three stages, power conversion efficiency is lower. Converters in [31]–[35] utilize multiple coupled inductors and built-in transformers, respectively, for achieving high voltage conversion ratios and soft switching. Although high voltage ratio can be obtained by adjusting the turns ratio of magnetic components but faced limitations by transfer capabilities. Furthermore, the maximum voltage stress of capacitors in the topology [32], [33], [35] is very high. The converter presented in [36] incorporates a charge pump, offering enhanced characteristics in inductor current balance and reduced component count. Moreover, due to the adoption of Silicon-Carbide Metal-Oxide-Semiconductor Field-Effect Transistor (SiC-MOSFET), the converter efficiency can be expected over 97%. However, it is constrained by a narrow voltage conversion ratio, which is similar to the converter in [28], limiting its applicability in wide voltage ratio operations. Additionally, it suffers from high maximum voltage stress, rendering it unsuitable for high-output-voltage applications.

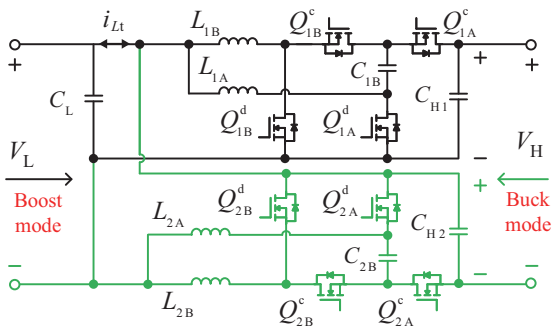



Fig. 2. Proposed F4P-ICPBDC topology.

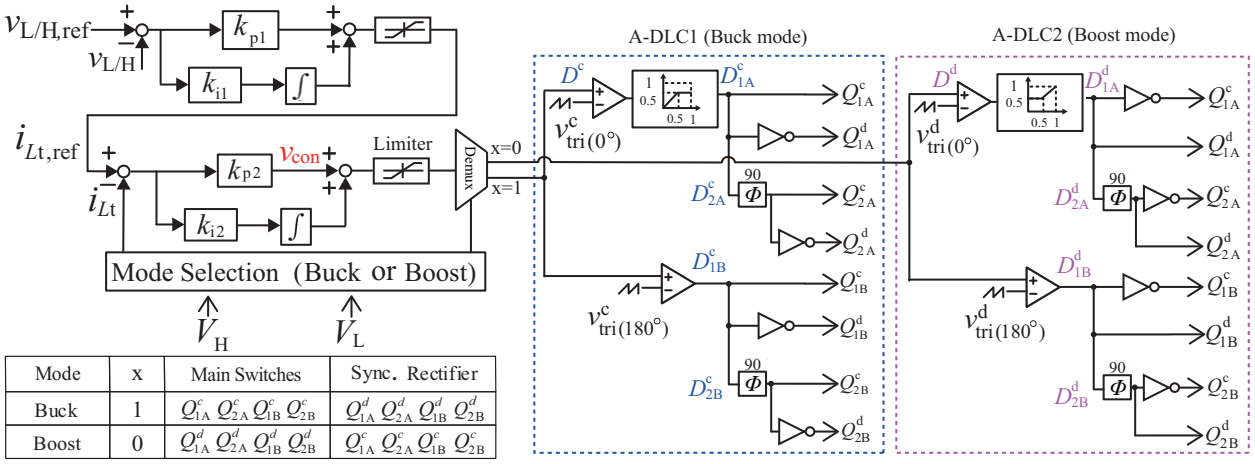
In order to address these limitations of the existing BDCs, a new circuit topology and control scheme are introduced in this article; a switched-capacitor based floating four-phase interleaved charge-pump bidirectional dc-dc converter (F4P-ICPBDC) with asymmetrical duty limit control (A-DLC) strategy. The proposed interleaved BDC demonstrates a superior voltage ratio compared to those in [28]–[30] and [36]. It also achieves naturally self-balancing of the inductor currents across the full duty cycle range both in buck and boost modes.

The remainder of this article is structured as follows: Section II details the topology and control strategy of the proposed floating four-phase interleaved charge-pump bidirectional dc-dc converter. Section III is dedicated for analysis of the steady-state characteristics of the converter based on its operating principles. The parameters design guideline of the proposed BDCs are described in Section IV. Experimental results with a SiC-MOSFET-based $1\,\mathrm{kW}$-$50\,\mathrm{kHz}$ prototype are discussed in Section V, where the essential performances of the proposed BDC are demonstrated in details. Finally in Section VI, the effectiveness of proposed circuit topology with the A-DLC control scheme are summarized and evaluated from the practical point of views.

## II. Proposed Converter and Control Strategy with A-DLC

The proposed F4P-ICPBDC is presented in Fig. 2. It is composed of two sets of power semiconductor switches $\mathrm{Q^c_{1A}}, \mathrm{Q^d_{1A}}, \mathrm{Q^c_{1B}}, \mathrm{Q^d_{1B}}$ and $\mathrm{Q^c_{2A}}, \mathrm{Q^d_{2A}}, \mathrm{Q^c_{2B}}, \mathrm{Q^d_{2B}}$ , charge-pump capacitors $C_{1\mathrm{B}}$ and $C_{2\mathrm{B}}$, power inductors $L_{1\mathrm{A}}$, $L_{1\mathrm{B}}$, $L_{2\mathrm{A}}$, and $L_{2\mathrm{B}}$, low-voltage side filter capacitor $C_{\mathrm{L}}$ and high-voltage side filter capacitors $C_{\mathrm{H1}}$ and $C_{\mathrm{H2}}$. In order to simplify the analysis and design of the circuit parameters, the operating conditions of the main circuit are given as; i) all the active and passive components are considered as ideal, ii) the dc inductor currents $i_{L_{1\mathrm{A}}}$, $i_{L_{1\mathrm{B}}}$, $i_{L_{2\mathrm{A}}}$ and $i_{L_{2\mathrm{B}}}$ are assumed to operate in continuous conduction mode (CCM), iii) the influence of load impedance is neglected in the steady-state analysis, and iv) the voltages of capacitors are assumed to be well smoothed and constant, which implies that the voltage ripples can be neglected due to the sufficiently large capacitance.

Fig. 3 illustrates a closed-loop control strategy incorporating A-DLC. This controller is comprised of dual closed-loops of output voltage and total current of the interleaved inductors.




| Mode | x | Main Switches | Sync. Rectifier |
|---|---|---|---|
| Buck | 1 | $Q^c_{1A}\ Q^c_{2A}\ Q^c_{1B}\ Q^c_{2B}$ | $Q^d_{1A}\ Q^d_{2A}\ Q^d_{1B}\ Q^d_{2B}$ |
| Boost | 0 | $Q^d_{1A}\ Q^d_{2A}\ Q^d_{1B}\ Q^d_{2B}$ | $Q^c_{1A}\ Q^c_{2A}\ Q^c_{1B}\ Q^c_{2B}$ |

Fig. 3. Schematic diagram of controller based on A-DLC.

TABLE I
RANGE OF DUTY CYCLES FOR BUCK AND BOOST MODES

| Switches | Buck mode | Boost mode |
|---|---|---|
| $Q^c_{1A}$ | $D^c_{1A} \le 0.5$ | $D^c_{1A} = 1 - D^d_{1A}$ |
| $Q^d_{1A}$ | $D^d_{1A} = 1 - D^c_{1A}$ | $0.5 \le D^d_{1A}$ |
| $Q^c_{1B}$ | $0 < D^c_{1B} < 1$ | $D^c_{1B} = 1 - D^d_{1B}$ |
| $Q^d_{1B}$ | $D^d_{1B} = 1 - D^c_{1B}$ | $0 < D^d_{1B} < 1$ |
| $Q^c_{2A}$ | $D^c_{2A} \le 0.5$ | $D^c_{2A} = 1 - D^d_{2A}$ |
| $Q^d_{2A}$ | $D^d_{2A} = 1 - D^c_{2A}$ | $0.5 \le D^d_{2A}$ |
| $Q^c_{2B}$ | $0 < D^c_{2B} < 1$ | $D^c_{2B} = 1 - D^d_{2B}$ |
| $Q^d_{2B}$ | $D^d_{2B} = 1 - D^c_{2B}$ | $0 < D^d_{2B} < 1$ |

Initially, the error between the sampled output voltage and the reference voltage undergoes external PI1 controller processing, which results in a reference current $i_{Lt,\mathrm{ref}}$. Subsequently, the total current $i_{Lt}$ of the four-phase inductors is detected and compared with the reference current. The internal PI2 controller is then employed to generate the control output $v_{\mathrm{con}}$, with its range constrained between 0 and 1. Then, the preliminary duty cycle $D^{\mathrm{c}}$ or $D^{\mathrm{d}}$ of the active switches is determined through the demultiplexer on the basis of the input and output voltages as well as operation mode.

In the case of buck mode as an example, the control signal $D^{\mathrm{c}}$ is compared with a unit triangle carrier to derive duty cycle signals $D^{\mathrm{c}}_{1\mathrm{A}}$ and $D^{\mathrm{c}}_{1\mathrm{B}}$. Subsequently, the signal $D^{\mathrm{c}}_{1\mathrm{A}}$ undergoes the A-DLC1 to obtain the ultimate duty cycle for the active switches $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$, $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}$, $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$, and $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}$. However, the signal $D^{\mathrm{c}}_{1\mathrm{B}}$ directly yields the duty cycles of the active switches $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}, \mathrm{Q}^{\mathrm{d}}_{1\mathrm{b}}, \mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$, and $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}$. Moreover, the switches $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}, \mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}, \mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}, \mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ operate with a phase difference of 90° in sequence, while the counter parts $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}, \mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}, \mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}$, and $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}$ operate in the synchronous rectification (SR) state. A similar control logic is applicable to the boost mode. The pulse generation and control rules for the above switches are presented in TABLE I.

### A. Buck Mode

The circuit configuration in the buck mode is shown in Fig. 4. The main switches $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$, $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$, $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$, $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ are driven with the phase-shift angle of 90° in sequence, while the counterpart switches $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}$, $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}$, $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$, $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}$ work as SR state to reduce the conduction power losses. Besides, the switch sets $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$ / $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}$, $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$ / $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$, $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$ / $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}$, and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ / $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}$ operate in complementary manner of gate driving, respectively. Furthermore, the charge pump capacitors $C_{1\mathrm{B}}$ and $C_{2\mathrm{B}}$ serve to step down the output voltage. The duty cycles of main switches are expressed as

$$\begin{cases} D^{\mathrm{c}}_{1\mathrm{A}} = D^{\mathrm{c}}_{2\mathrm{A}} = \begin{cases} D^{\mathrm{c}} \text{ when } D^{\mathrm{c}} < 0.5 \\ 0.5 \text{ when } D^{\mathrm{c}} \ge 0.5 \end{cases} \\ D^{\mathrm{c}}_{1\mathrm{B}} = D^{\mathrm{c}}_{2\mathrm{B}} = D^{\mathrm{c}}. \end{cases} \tag{1}$$

The typical operating waveforms of the main circuit for the buck mode are depicted in Fig. 5. Referring to these waveforms, the switching one cycle is divided into eight intervals as demonstrated in Fig. 6. The operating principle in the buck mode is described as follows when A-DLC1 is in active (Fig. 5(b)):

**[Mode 1b]** ($t_0 \le t < t_1$) The active switch $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$ which is operating in SR is turned OFF at $t = t_0$, and in a short interval the main switch $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$ in the positive dc rail is turned ON. Thus, the dc inductor $L_{1\mathrm{B}}$ begins to store the magnetic energy and

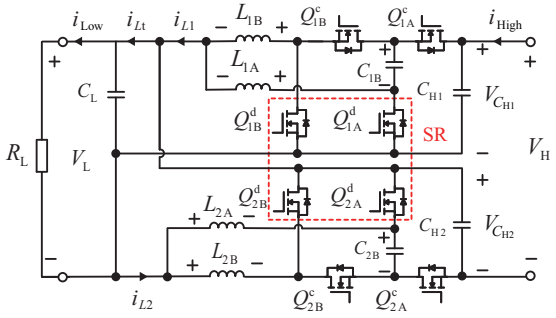



Fig. 4. Circuit configuration of F4P-ICPBDC in the buck mode.

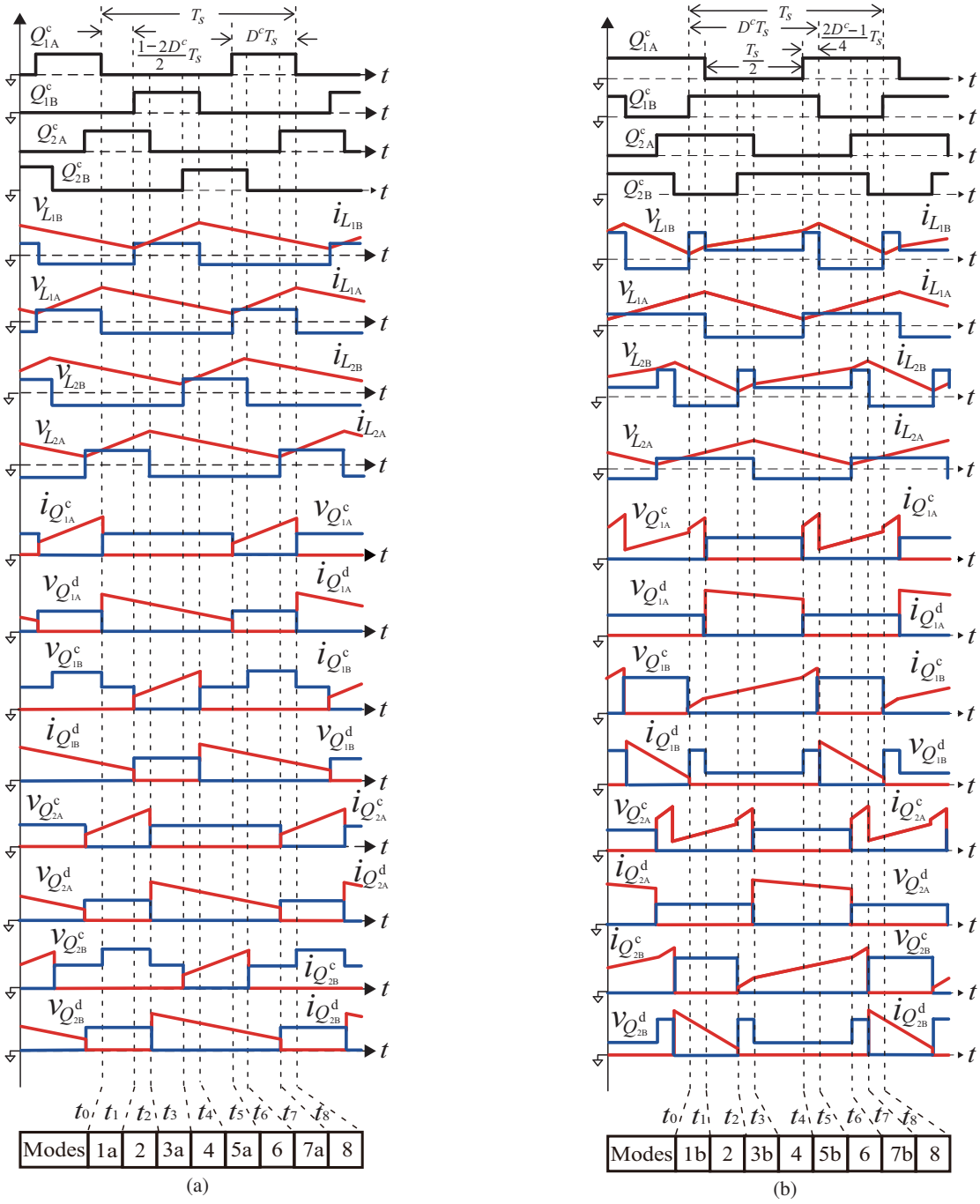



Fig. 5. Typical waveforms of F4P-ICPBDC in a buck mode, (a) $D^{\mathrm{c}} < 0.5$, and (b) $D^{\mathrm{c}} \geq 0.5$ .

its current $i_{L_{1\mathrm{B}}}$ linearly increases.

**[Mode 2]** ($t_1 \leq t < t_2$) The main switch $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$ in the positive dc rail is turned OFF at $t = t_1$, and in a short time interval $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}$ is turned ON by SR. Accordingly, the dc inductor current $i_{L_{1\mathrm{B}}}$ increases its positive gradient due to $V_{C_{1\mathrm{B}}} > V_{\mathrm{L}}$, while $i_{L_{2\mathrm{B}}}$ keeps discharging.

**[Mode 3b]** ($t_2 \leq t < t_3$) The SR switch $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}$ is turned OFF at $t = t_2$, after which $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ in the negative dc rail is turned ON. Thus, the magnetic energy in the dc inductor $L_{2\mathrm{B}}$ is stored, thereby $i_{L_{2\mathrm{B}}}$ begins to increase linearly.

**[Mode 4]** ($t_3 \leq t < t_4$) The main switch $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$ in the negative dc rail is turned OFF at $t = t_3$, after which $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}$ is turned ON by SR. Then, the dc inductor current $i_{L_{2\mathrm{B}}}$ keeps to increase linearly due to $V_{C_{2\mathrm{B}}} > V_{\mathrm{L}}$.

**[Mode 5b]** ($t_4 \leq t < t_5$) The SR switch $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}$ is turned OFF at $t = t_4$, and in a short interval the switch $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$ in the positive dc rail is turned ON. Accordingly, the dc inductor current $i_{L_{1\mathrm{A}}}$ changes to increase linearly .

**[Mode 6]** ($t_5 \leq t < t_6$) The main switch $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$ in the positive dc rail is turned OFF at $t = t_5$, after which $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$ is turned ON by SR.

**[Mode 7b]** ($t_6 \leq t < t_7$) The SR switch $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}$ is turned OFF

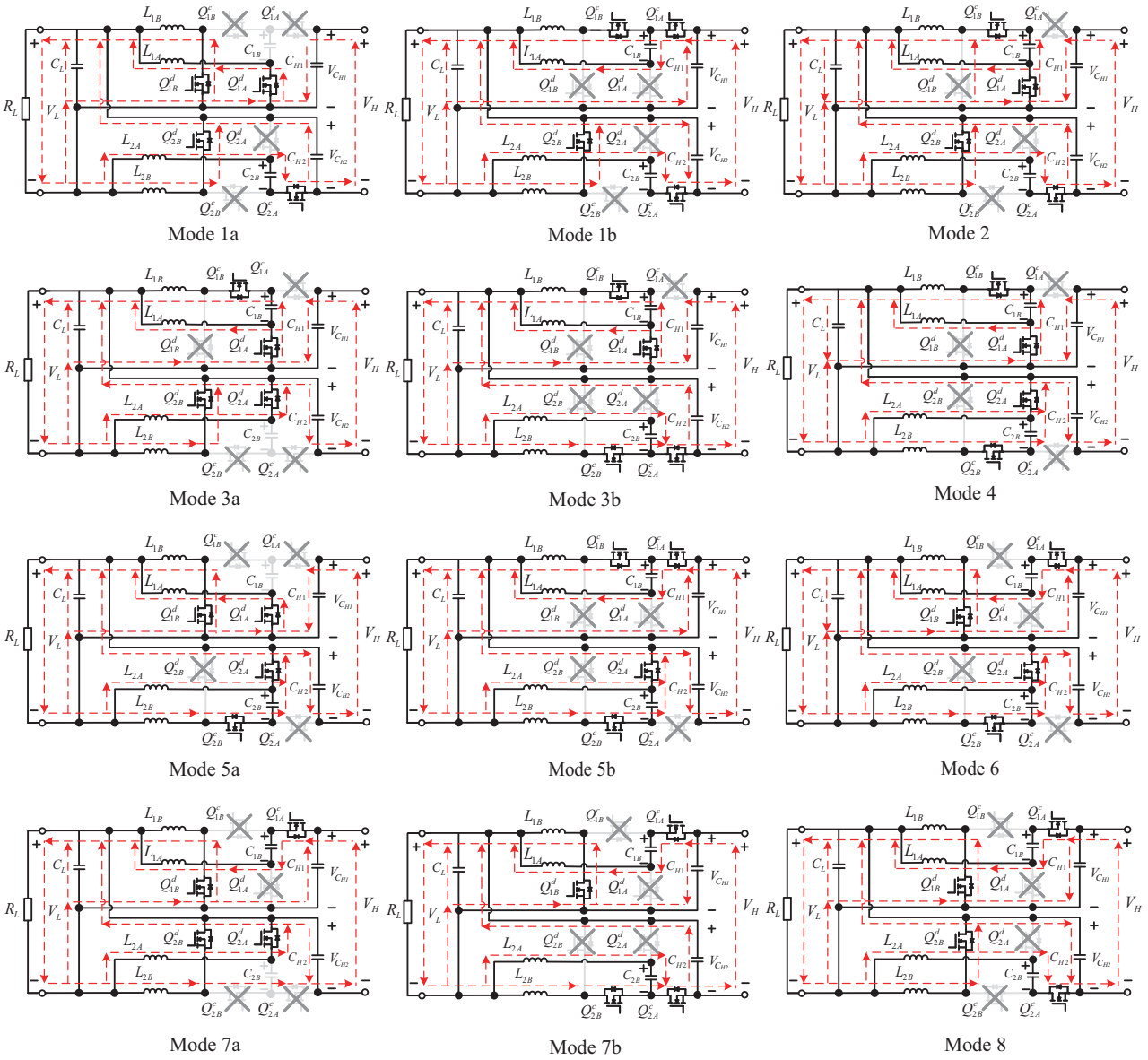



Fig. 6. Mode transitions and equivalent circuits during the switching one cycle in a buck mode.

at $t = t_6$, after which the active switch $\mathrm{Q^c_{2A}}$ on the negative dc rail is turned ON. Then, the magnetic energy is stored at $L_{2A}$, whereby the dc inductor current $i_{L_{2A}}$ begins to linearly increase.

**[Mode 8]** ($t_7 \leq t < t_8$) The active switch $\mathrm{Q^c_{2B}}$ on the negative dc rail is turned OFF at $t = t_7$, and in the short interval the counterpart $\mathrm{Q^d_{2B}}$ is turned ON by SR. Then, the dc inductor current $i_{L_{2B}}$ starts to decline linearly.

### *B. Boost Mode*

The circuit configuration of F4P-ICPBDC in the boost mode is shown in Fig. 7. The main switches $\mathrm{Q^d_{1A}}, \mathrm{Q^d_{2A}}, \mathrm{Q^d_{1B}}, \mathrm{Q^d_{2B}}$ are driven with the phase-shift angle of 90° in sequence, meanwhile the active switches $\mathrm{Q^c_{1A}}, \mathrm{Q^c_{2A}}, \mathrm{Q^c_{1B}}, \mathrm{Q^c_{2B}}$ work as SR state to improve the conversion efficiency. The sets of switches $\mathrm{Q^c_{1A}}$ / $\mathrm{Q^d_{1A}}$, $\mathrm{Q^c_{1B}}$ / $\mathrm{Q^d_{1B}}$, $\mathrm{Q^c_{2A}}$ / $\mathrm{Q^d_{2A}}$ and $\mathrm{Q^c_{2B}}$ / $\mathrm{Q^d_{2B}}$ operate in complementary manner, respectively. The charge pump capacitors $C_{1B}$ and $C_{2B}$ serve to step up the voltage

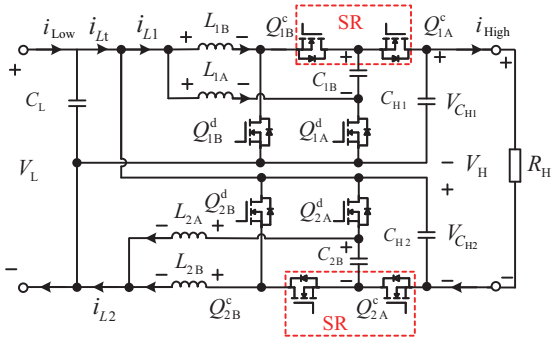



Fig. 7. Circuit configuration of F4P-ICPBDC in the boost mode.

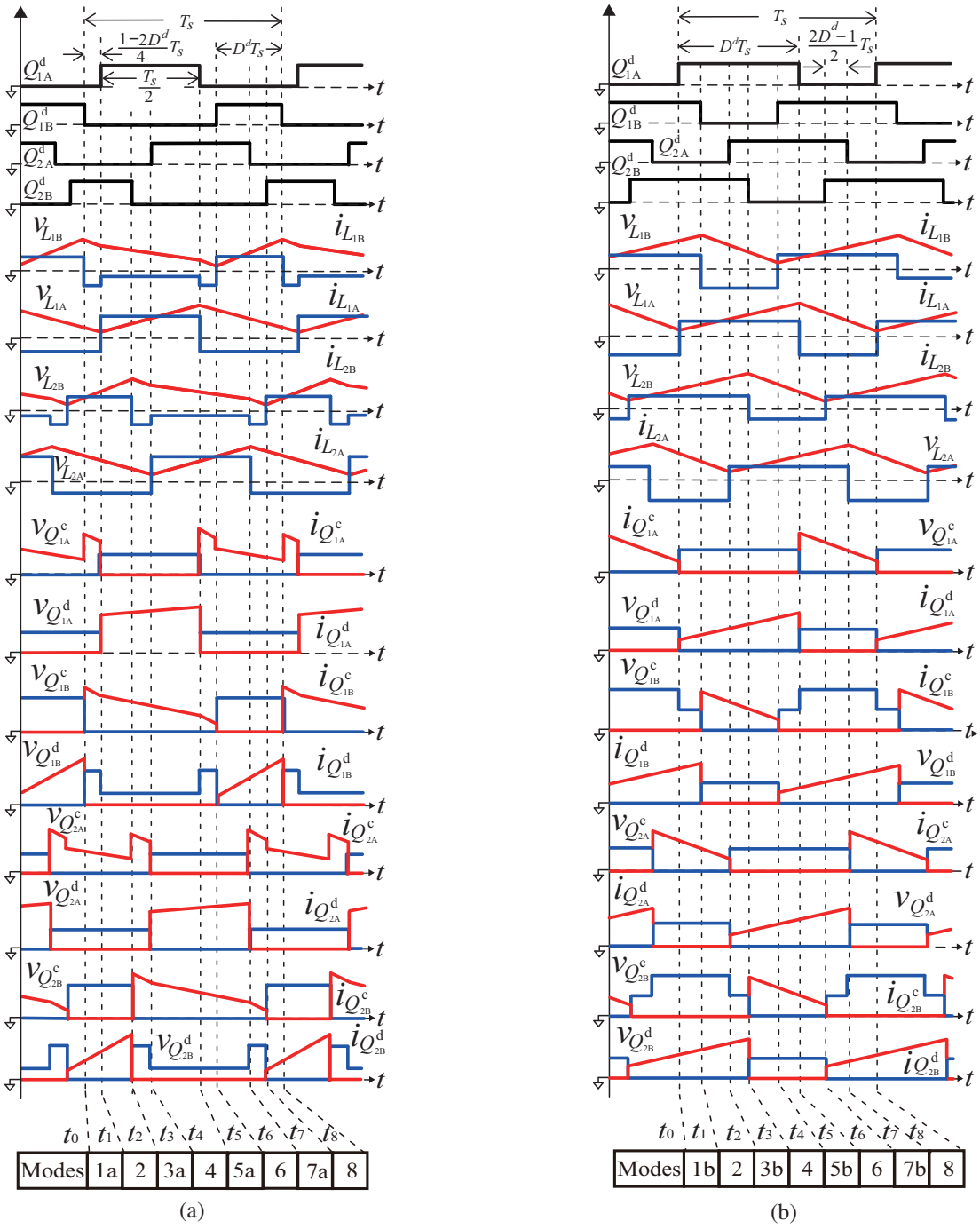
from $V_{\mathrm{L}}$ to $V_{\mathrm{H}}$. The duty cycles of main switches are expressed as

$$\begin{cases} D^{\mathrm{d}}_{1\mathrm{A}} = D^{\mathrm{d}}_{2\mathrm{A}} = \begin{cases} 0.5 \text{ when } D^{\mathrm{d}} \le 0.5 \\ D^{\mathrm{d}} \text{ when } D^{\mathrm{d}} > 0.5 \end{cases} \\ D^{\mathrm{d}}_{1\mathrm{B}} = D^{\mathrm{d}}_{2\mathrm{B}} = D^{\mathrm{d}}. \end{cases} \tag{2}$$

The typical gate signals and voltage and current waveforms for the boost mode are depicted in Fig. 8. Referring to these waveforms, the switching one cycle is divided into eight intervals as demonstrated in Fig. 9. The operating principle in the boost mode is described as follows when A-DLC2 is active (Fig. 8(a)):

**[Mode 1a]** ($t_0 \le t < t_1$) The main switch $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$ is turned OFF at $t = t_0$, after which $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$ in the positive dc rail is turned ON by SR. Then, the magnetic energy of $L_{1\mathrm{B}}$ begins to be released to the high voltage side $V_{\mathrm{H}}$, whereby the current $i_{L_{1\mathrm{B}}}$ decline linearly. The circuit operation is returned to Mode 2 at $t = t_1$.

**[Mode 2]** ($t_1 \le t < t_2$) The SR switch $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$ in the positive dc rail is turned OFF at $t = t_1$, after which the counterpart




(a) (b)

Fig. 8. Typical waveforms of F4P-ICPBDC in a boost mode, (a) $D^{\mathrm{d}} \le 0.5$, (b) $D^{\mathrm{d}} > 0.5$ .

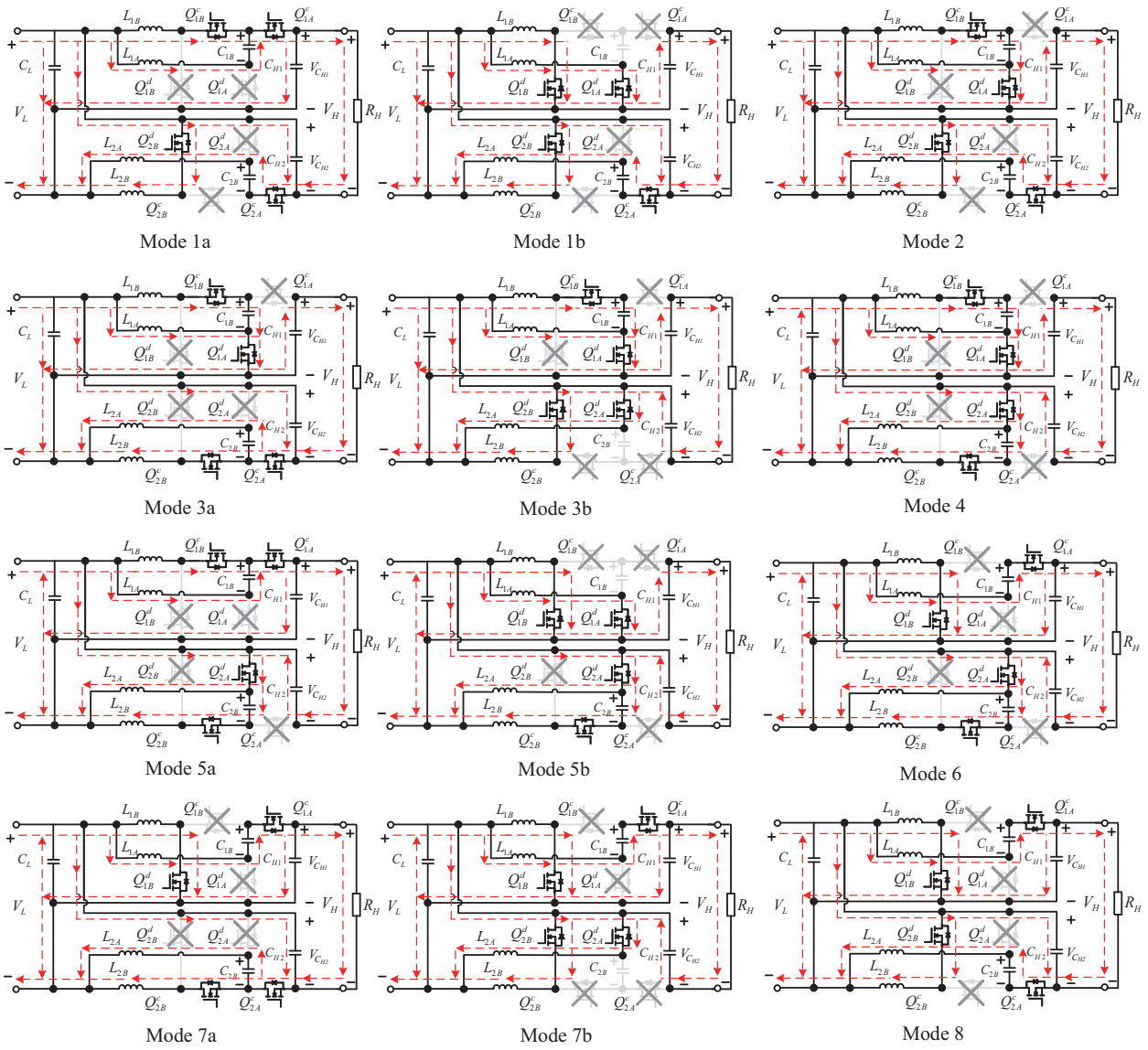



Fig. 9. Mode transitions and equivalent circuits during the switching one cycle in a boost mode.

main switch $Q^{d}_{1A}$ is turned ON. Then dc inductor currents $i_{L_{1A}}$ increases gradually.

**[Mode 3a]** ($t_2 \leq t < t_3$) The main switch $Q^{d}_{2B}$ is turned OFF at $t = t_2$, and $Q^{c}_{2B}$ on the negative dc rail is turned ON by SR. Then, the magnetic energy in $L_{2B}$ begins to be released to the high voltage side and $i_{L_{2B}}$ decline linearly.

**[Mode 4]** ($t_3 \leq t < t_4$) The SR switch $Q^{c}_{2A}$ in the negative dc rail is turned OFF at $t = t_3$, and the main switch $Q^{d}_{2A}$ is turned ON. The dc inductor $L_{2A}$ begins to store magnetic energy via $C_{\mathrm{L}}$, thereby $i_{L_{2A}}$ rises linearly.

**[Mode 5a]** ($t_4 \leq t < t_5$) The main switch $Q^{d}_{1A}$ is turned OFF at $t = t_4$, after which $Q^{c}_{1A}$ in the positive dc rail is turned ON by SR. Then, the magnetic energy in $L_{1A}$ is released to the output side $V_{\mathrm{H}}$ by discharging of $C_{1B}$, and $i_{L_{1A}}$ begins to decline with a certain slope.

**[Mode 6]** ($t_5 \leq t < t_6$) The SR switch $Q^{c}_{1B}$ in the positive dc rail is turned OFF at $t = t_5$, and in the short interval the main $Q^{d}_{1B}$ is turned ON. Accordingly, the magnetic energy in $L_{1B}$ begins to store, as a result $i_{L_{1B}}$ starts to increase linearly.

**[Mode 7a]** ($t_6 \leq t < t_7$) The main switch $Q^{d}_{2A}$ is turned OFF at $t = t_6$, and $Q^{c}_{2A}$ in the negative dc rail is turned ON by SR. Then, the magnetic energy in $L_{2A}$ is released to the high voltage side, whereby $i_{L_{2A}}$ decreases with a certain slope.

**[Mode 8]** ($t_7 \leq t < t_8$) The SR switch $Q^{c}_{2B}$ in the negative dc rail is turned OFF at $t = t_7$, followed by the turn ON of the main switch $Q^{d}_{2B}$. Accordingly, the dc inductor $L_{2B}$ starts to store the magnetic energy, whereby the dc inductor current $i_{L_{2B}}$ begins to increase linearly.

## III. Steady-State Analysis

### A. Inductor Current Self-Balancing with A-DLC

*1) Buck Mode:* It is assumed here that the duty cycles of the main switches $Q^{c}_{1A}$ and $Q^{c}_{2A}$ are represented by $D^{c}_{A}$ while those of $Q^{c}_{1B}$ and $Q^{c}_{2B}$ are represented by $D^{c}_{B}$ , with both $D^{c}_{A}$

and $D_{\mathrm{B}}^{\mathrm{c}}$ equal to $D^{\mathrm{c}}$. By applying the ampere-second balance principle on capacitors $C_{1\mathrm{B}}$, $C_{2\mathrm{B}}$, $C_{\mathrm{H1}}$, $C_{\mathrm{H2}}$, and $C_{\mathrm{L}}$ for the buck mode, the dc components of the current through $L_{1\mathrm{A}}$, $L_{1\mathrm{B}}$, $L_{2\mathrm{A}}$, and $L_{2\mathrm{B}}$ can be expressed theoretically as

$$I_{L_{1\mathrm{A}}} = I_{L_{2\mathrm{A}}} = \begin{cases} \dfrac{I_{\mathrm{Low}} + I_{\mathrm{High}}}{4} & \text{when } D^{\mathrm{c}} < 0.5 \\ \dfrac{D_{\mathrm{A}}^{\mathrm{c}}(I_{\mathrm{Low}} + I_{\mathrm{High}})}{2} & \text{when } D^{\mathrm{c}} \geq 0.5 \end{cases} \tag{3}$$

$$I_{L_{1\mathrm{B}}} = I_{L_{2\mathrm{B}}} = \begin{cases} \dfrac{I_{\mathrm{Low}} + I_{\mathrm{High}}}{4} & \text{when } D^{\mathrm{c}} < 0.5 \\ \dfrac{(1 - D_{\mathrm{A}}^{\mathrm{c}})(I_{\mathrm{Low}} + I_{\mathrm{High}})}{2} & \text{when } D^{\mathrm{c}} \geq 0.5. \end{cases} \tag{4}$$

where, $I_{\mathrm{Low}}$ and $I_{\mathrm{High}}$ represent the low-voltage side load current, and the high-voltage side source current, respectively. It can be observed from (3) and (4) that condition in (1) should be satisfied in order to achieve balance of the inductor currents within the full range of duty cycle. At this point, the average inductor current can be represented as follows:

$$\begin{aligned} I_{L_{1\mathrm{A}}} &= I_{L_{1\mathrm{B}}} = I_{L_{2\mathrm{A}}} = I_{L_{2\mathrm{B}}} \\ &= I_{L_{\mathrm{A,B}}} = \frac{I_{\mathrm{Low}} + I_{\mathrm{High}}}{4} = \frac{V_{\mathrm{L}}}{R_{\mathrm{L}}(4 - D^{\mathrm{c}})}. \end{aligned} \tag{5}$$

*2) Boost Mode:* It is assumed here that the duty cycles of main switches $\mathrm{Q}_{1\mathrm{A}}^{\mathrm{d}}$ and $\mathrm{Q}_{2\mathrm{A}}^{\mathrm{d}}$ are represented by $D_{\mathrm{A}}^{\mathrm{d}}$ while those of $\mathrm{Q}_{1\mathrm{B}}^{\mathrm{d}}$ and $\mathrm{Q}_{2\mathrm{B}}^{\mathrm{d}}$ are expressed by $D_{\mathrm{B}}^{\mathrm{d}}$ , where $D_{\mathrm{A}}^{\mathrm{d}}$ and $D_{\mathrm{B}}^{\mathrm{d}}$ are identical with $D^{\mathrm{d}}$. In a similar manner, applying the ampere-second balance into $C_{1\mathrm{B}}$, $C_{2\mathrm{B}}$, $C_{\mathrm{H1}}$, $C_{\mathrm{H2}}$ and $C_{\mathrm{L}}$ for the boost mode yield the dc components of dc inductors $L_{1\mathrm{A}}$, $L_{1\mathrm{B}}$, $L_{2\mathrm{A}}$, $L_{2\mathrm{B}}$ as expressed by

$$I_{L_{1\mathrm{A}}} = I_{L_{2\mathrm{A}}} = \begin{cases} \dfrac{(1 - D_{\mathrm{A}}^{\mathrm{d}})(I_{\mathrm{Low}} + I_{\mathrm{High}})}{2} & \text{when } D^{\mathrm{d}} \leq 0.5 \\ \dfrac{I_{\mathrm{Low}} + I_{\mathrm{High}}}{4} & \text{when } D^{\mathrm{d}} > 0.5 \end{cases} \tag{6}$$

$$I_{L_{1\mathrm{B}}} = I_{L_{2\mathrm{B}}} = \begin{cases} \dfrac{D_{\mathrm{A}}^{\mathrm{d}}(I_{\mathrm{Low}} + I_{\mathrm{High}})}{2} & \text{when } D^{\mathrm{d}} \leq 0.5 \\ \dfrac{I_{\mathrm{Low}} + I_{\mathrm{High}}}{4} & \text{when } D^{\mathrm{d}} > 0.5. \end{cases} \tag{7}$$

where, $I_{\mathrm{Low}}$ and $I_{\mathrm{High}}$ represent the low-voltage side source current and the high-voltage side load current, respectively. In the similar way, it can be observed from (6) and (7) that condition in (2) should be satisfied so as to achieve balance of the inductor currents within the full range of duty cycle. At this point, the average inductor current can be represented as follows:

$$\begin{aligned} I_{L_{1\mathrm{A}}} &= I_{L_{1\mathrm{B}}} = I_{L_{2\mathrm{A}}} = I_{L_{2\mathrm{B}}} = I_{L_{\mathrm{A,B}}} \\ &= \frac{I_{\mathrm{Low}} + I_{\mathrm{High}}}{4} = \frac{V_{\mathrm{H}}}{R_{\mathrm{H}}(1 - D^{\mathrm{d}})}. \end{aligned} \tag{8}$$

Therefore, it can be known from (5) and (8) that the dc inductor currents are naturally balance with the aid of A-DLCs.

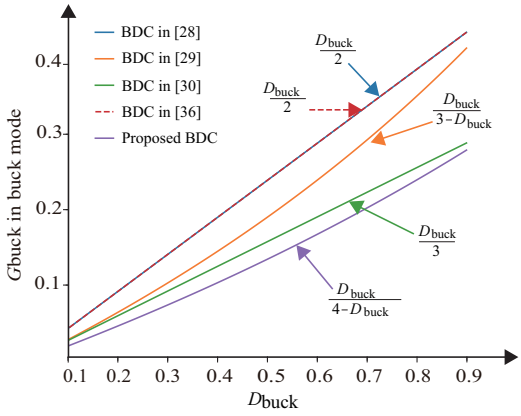



Fig. 10. Theoretical curves of dc voltage ratio in the buck mode.

### B. Voltage Conversion Ratio in Steady-State

*1) Buck Mode:* By applying the voltage-second balance principle into $L_{1\mathrm{A}}, L_{1\mathrm{B}}, L_{2\mathrm{A}}$, and $L_{2\mathrm{B}}$ based on (44) and (45) introduced in the APPENDIX, the voltage conversion ratio can be derived as

$$G_{\mathrm{buck}} = \frac{V_{\mathrm{L}}}{V_{\mathrm{H}}} = \begin{cases} \dfrac{D^{\mathrm{c}}}{4 - D^{\mathrm{c}}} & \text{when } D^{\mathrm{c}} \leq 0.5 \\ \dfrac{D_{\mathrm{A}}^{\mathrm{c}} D_{\mathrm{B}}^{\mathrm{c}}}{2 - D_{\mathrm{A}}^{\mathrm{c}} D_{\mathrm{B}}^{\mathrm{c}}} = \dfrac{D^{\mathrm{c}}}{4 - D^{\mathrm{c}}} & \text{when } D^{\mathrm{c}} > 0.5. \end{cases} \tag{9}$$

*2) Boost Mode:* Similarly, applying the voltage-second balance principle to $L_{1\mathrm{A}}, L_{1\mathrm{B}}, L_{2\mathrm{A}}$, and $L_{2\mathrm{B}}$ based on (46) and (47) in the APPENDIX, the voltage conversion ratio can be expressed as

$$G_{\mathrm{boost}} = \frac{V_{\mathrm{H}}}{V_{\mathrm{L}}} = \begin{cases} \dfrac{1 + D_{\mathrm{A}}^{\mathrm{d}} + D_{\mathrm{B}}^{\mathrm{d}} - D_{\mathrm{A}}^{\mathrm{d}} D_{\mathrm{B}}^{\mathrm{d}}}{(1 - D_{\mathrm{A}}^{\mathrm{d}})(1 - D_{\mathrm{B}}^{\mathrm{d}})} = \dfrac{3 + D^{\mathrm{d}}}{1 - D^{\mathrm{d}}} & \text{when } D^{\mathrm{d}} < 0.5 \\ \dfrac{3 + D^{\mathrm{d}}}{1 - D^{\mathrm{d}}} & \text{when } D^{\mathrm{d}} \geq 0.5. \end{cases} \tag{10}$$

According to (9) and (10), the voltage conversion ratios of the proposed and existing BDCs in the literatures [28]–[30], [36] are illustrated in Figs. 10 and 11. It is evident that the available voltage conversion ratios of the proposed BDC is much wider than those of other BDCs both in the buck and boost modes. The voltage conversion ratio $G_{\mathrm{buck}}$ attains in the range between $0.053$ and $0.25$ for $0.2 < D^{\mathrm{c}} < 0.8$ in the buck mode. The voltage ratio $G_{\mathrm{boost}}$ covers the range from $4$ to $19$ for $0.2 < D^{\mathrm{d}} < 0.8$ in the boost mode. Thus, it is revealed from Figs. 10 and 11 that the proposed BDC topology is advantageous over the others in terms of dc voltage ratio.

### C. Analysis of Voltage Stresses on Power Devices

*1) Buck Mode:* Applying the ampere-second balance principle to $C_{1\mathrm{B}}$, $C_{2\mathrm{B}}$, $C_{\mathrm{H1}}$ and $C_{\mathrm{H2}}$ based on (44) and (45) in-

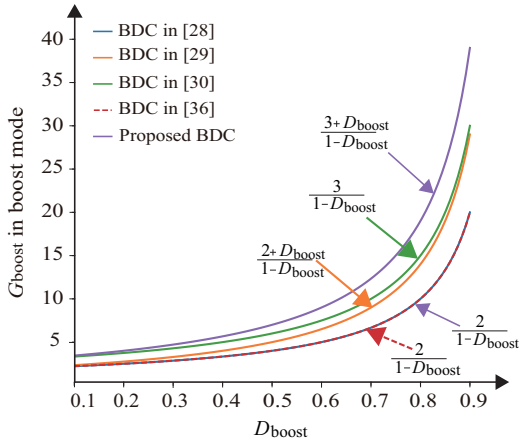



Fig. 11. Theoretical curves of dc voltage ratio in the boost mode.

troduced in the APPENDIX, the voltage across the capacitors can be determined as

$$V_{C_{1B}} = V_{C_{2B}} = \begin{cases} \dfrac{V_H}{4 - D^c} & \text{when } D^c < 0.5 \\ \dfrac{2(1 - D^c)V_H}{4 - D^c} & \text{when } D^c \geq 0.5 \end{cases} \tag{11}$$

$$V_{C_{H1}} = V_{C_{H2}} = \frac{2V_H}{4 - D^c} = \frac{V_H + V_L}{2}. \tag{12}$$

By employing (11) and (12) into the state equations for the buck mode, the voltage stresses of active switches can be derived as:

$$\begin{cases} \begin{cases} V_{Q^c_{1A}} = V_{Q^d_{1A}} = V_{Q^c_{2A}} = V_{Q^d_{2A}} \\ \quad = V_{Q^d_{1B}} = V_{Q^d_{2B}} = \dfrac{V_H}{4 - D^c} \\ V_{Q^c_{1B}} = V_{Q^c_{2B}} = \dfrac{2V_H}{4 - D^c} = \dfrac{V_H + V_L}{2} \end{cases} & \text{when } D^c < 0.5 \\ \begin{cases} V_{Q^c_{1A}} = V_{Q^d_{1A}} = V_{Q^c_{2A}} \\ \quad = V_{Q^d_{2A}} = \dfrac{2D^c V_H}{4 - D^c} \\ V_{Q^c_{1B}} = V_{Q^c_{2B}} = V_{Q^d_{1B}} \\ \quad = V_{Q^d_{2B}} = \dfrac{2V_H}{4 - D^c} = \dfrac{V_H + V_L}{2}. \end{cases} & \text{when } D^c \geq 0.5 \end{cases} \tag{13}$$

The maximum voltage stresses of the power devices are displayed for the buck mode in TABLE II.

*2) Boost Mode:* In the similar way, by applying the ampere-second balance principle to $C_{1B}$ and $C_{2B}$, $C_{H1}$ and $C_{H2}$ based on (46) and (47) of the APPENDIX, the capacitors voltages can be determined as

$$V_{C_{1B}} = V_{C_{2B}} = \begin{cases} \dfrac{2D^d V_L}{1 - D^d} & \text{when } D^d \leq 0.5 \\ \dfrac{V_L}{1 - D^d} & \text{when } D^d > 0.5 \end{cases} \tag{14}$$

$$V_{C_{H1}} = V_{C_{H2}} = \frac{2V_L}{1 - D^d} = \frac{V_H + V_L}{2}. \tag{15}$$

TABLE II
VOLTAGE STRESSES OF ACTIVE SWITCHES IN BUCK MODE

| Duty Cycle | | $0 < D^c < 0.5$ | $0.5 \leq D^c < 1$ |
|---|---|---|---|
| Voltage Stresses | $Q^c_{1A}, Q^c_{2A}$ | $\frac{V_H}{4 - D^c}$ | $\frac{2D^c V_H}{4 - D^c}$ |
| | $Q^c_{1B}, Q^c_{2B}$ | $\frac{2V_H}{4 - D^c}$ | $\frac{2V_H}{4 - D^c}$ |
| | $Q^d_{1A}, Q^d_{2A}$ | $\frac{V_H}{4 - D^c}$ | $\frac{2D^c V_H}{4 - D^c}$ |
| | $Q^d_{1B}, Q^d_{2B}$ | $\frac{V_H}{4 - D^c}$ | $\frac{2V_H}{4 - D^c}$ |

TABLE III
VOLTAGE STRESSES OF ACTIVE SWITCHES IN BOOST MODE

| Duty Cycle | | $0 < D^d \leq 0.5$ | $0.5 < D^d < 1$ |
|---|---|---|---|
| Voltage Stresses | $Q^c_{1A}, Q^c_{2A}$ | $2V_L$ | $\frac{V_L}{1 - D^d}$ |
| | $Q^c_{1B}, Q^c_{2B}$ | $\frac{2V_L}{1 - D^d}$ | $\frac{2V_L}{1 - D^d}$ |
| | $Q^d_{1A}, Q^d_{2A}$ | $2V_L$ | $\frac{V_L}{1 - D^d}$ |
| | $Q^d_{1B}, Q^d_{2B}$ | $\frac{2V_L}{1 - D^d}$ | $\frac{V_L}{1 - D^d}$ |

By substituting (14) and (15) for the state equations, the voltage stresses of active switches in the boost mode can be derived as

$$\begin{cases} \begin{cases} V_{Q^c_{1A}} = V_{Q^d_{1A}} = V_{Q^c_{2A}} \\ \quad = V_{Q^d_{2A}} = 2V_L \\ V_{Q^c_{1B}} = V_{Q^d_{1B}} = V_{Q^c_{2B}} = V_{Q^d_{2B}} \\ \quad = \dfrac{2V_L}{1 - D^d} = \dfrac{V_H + V_L}{2} \end{cases} & \text{when } D^d \leq 0.5 \\ \begin{cases} V_{Q^c_{1A}} = V_{Q^d_{1A}} = V_{Q^c_{2A}} = V_{Q^d_{2A}} \\ \quad = V_{Q^d_{1B}} = V_{Q^d_{2B}} = \dfrac{V_L}{1 - D^d} \\ V_{Q^c_{1B}} = V_{Q^c_{2B}} \\ \quad = \dfrac{2V_L}{1 - D^d} = \dfrac{V_H + V_L}{2}. \end{cases} & \text{when } D^d > 0.5 \end{cases} \tag{16}$$

The maximum stress of the power devices is comprehensively presented for the boost mode in TABLE III.

### D. Analysis of Inductor Current Ripples

*1) Buck Mode:* Taking the duty cycle range of $0 < D^c < 0.5$ into account, the current ripples of $L_{1A}$, $L_{1B}$, $L_{2A}$ and $L_{2B}$ can be derived in the buck mode as:

$$\begin{aligned} \Delta i_{L_{1A}} &= \Delta i_{L_{2A}} = \Delta i_{L_{1B}} = \Delta i_{L_{2B}} \\ &= \Delta i_{L_{A,B}} = \frac{(1 - D^c)V_L}{L f_s}. \end{aligned} \tag{17}$$

By combining (5) and (17), the current ripple rate can be derived as follows

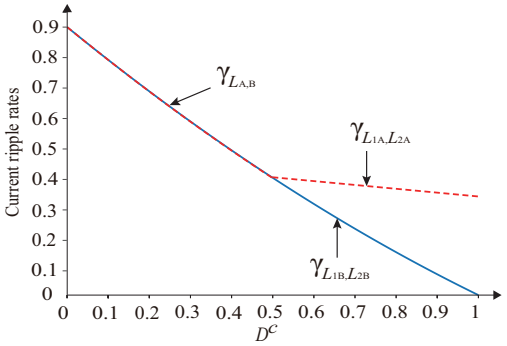



Fig. 12. Inductor current ripple rates versus duty cycle in the buck mode.

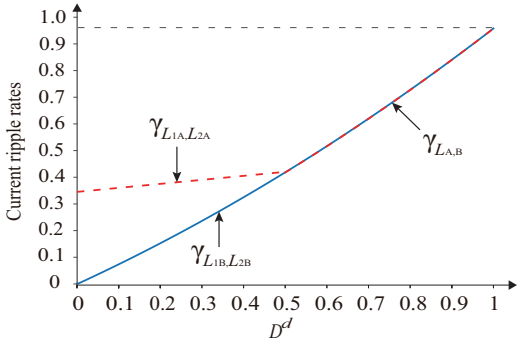



Fig. 13. Inductor current ripple rates versus duty cycle in the boost mode.

$$\gamma_{L_{1A},L_{2A}} = \gamma_{L_{1B},L_{2B}} = \gamma_{L_{A,B}} = \frac{\Delta i_{L_{A,B}}}{2I_{L_{A,B}}} = \frac{(1-D^c)(4-D^c)R_L}{2Lf_s}. \quad (18)$$

In the similar way, the current ripples of $L_{1A}$, $L_{1B}$, $L_{2A}$ and $L_{2B}$ within the range of $0.5 \leq D^c < 1$ can be described as follows:

$$\Delta i_{L_{1A}} = \Delta i_{L_{2A}} = \Delta i_{L_A} = \frac{V_L}{2Lf_s} \quad (19)$$

$$\Delta i_{L_{1B}} = \Delta i_{L_{2B}} = \Delta i_{L_B} = \frac{(1-D^c)V_L}{Lf_s}. \quad (20)$$

Employing (5) to (19) and (20) respectively, the current ripple rates can be expressed as

$$\gamma_{L_{1A},L_{2A}} = \frac{\Delta i_{L_A}}{2I_{L_{A,B}}} = \frac{(4-D^c)R_L}{4Lf_s} \quad (21)$$

$$\gamma_{L_{1B},L_{2B}} = \frac{\Delta i_{L_B}}{2I_{L_{A,B}}} = \frac{(1-D^c)(4-D^c)R_L}{2Lf_s}. \quad (22)$$

The characteristics of current ripple rates in $L_{1A}$, $L_{1B}$, $L_{2A}$ and $L_{2B}$ versus $D^c$ are portrayed in Fig. 12 with a set of numerical values: $L_{1A} = L_{1B} = L_{2A} = L_{2B} = 219\,\mu$H, the switching frequency $f_s = 50\,$kHz, $V_H = 400\,$V, and $V_L = 72\,$V. Since the rated power is set as $1\,$kW, the nominal load resistance is given as $R_L = 5.184\,\Omega$. As the duty cycle increases, the ripple rates of the inductor current tends to decline. Within the range of $0.5 < D^c < 1$, the current ripples in the inductors $L_{1B}$ and $L_{2B}$ are smaller than those of $L_{1A}$ and $L_{2A}$ due to the effect of topology:($C_{1B}$ and $C_{2B}$).

*2) Boost Mode:* The current ripples of $L_{1A}$, $L_{1B}$, $L_{2A}$, and $L_{2B}$ within the range of $0 < D^d \leq 0.5$ can be defined as

$$\Delta i_{L_{1A}} = \Delta i_{L_{2A}} = \Delta i_{L_A} = \frac{V_L}{2Lf_s} \quad (23)$$

$$\Delta i_{L_{1B}} = \Delta i_{L_{2B}} = \Delta i_{L_B} = \frac{D^d V_L}{Lf_s}. \quad (24)$$

Substituting (8) for (23) and (24) respectively, the current ripple rates can be derived as follows:

$$\gamma_{L_{1A},L_{2A}} = \frac{\Delta i_{L_A}}{2I_{L_{A,B}}} = \frac{(1-D^d)^2 R_H}{4(3+D^d)Lf_s} \quad (25)$$

$$\gamma_{L_{1B},L_{2B}} = \frac{\Delta i_{L_B}}{2I_{L_{A,B}}} = \frac{D^d(1-D^d)^2 R_H}{2(3+D^d)Lf_s}. \quad (26)$$

The current ripples of $L_{1A}$, $L_{1B}$, $L_{2A}$, and $L_{2B}$ in the range of $0.5 < D^d < 1$ can also be described as

$$\Delta i_{L_{1A}} = \Delta i_{L_{2A}} = \Delta i_{L_{1B}} = \Delta i_{L_{2B}} = \Delta i_{L_{A,B}} = \frac{D^d V_L}{Lf_s}. \quad (27)$$

Accordingly, combination (8) and (27) yields the current ripple rate as

$$\gamma_{L_{1A},L_{2A}} = \gamma_{L_{1B},L_{2B}} = \gamma_{L_{A,B}} = \frac{\Delta i_{L_{A,B}}}{2I_{L_{A,B}}} = \frac{D^d(1-D^d)^2 R_H}{2(3+D^d)Lf_s}. \quad (28)$$

The characteristics of current ripple rates in $L_{1A}$, $L_{1B}$, $L_{2A}$ and $L_{2B}$ versus $D^d$ are shown in Fig. 13 with the same parameters as the buck mode mentioned above, except for the load resistance. In the boost mode, where the output power is likewise fixed at $1\,$kW, the load varies with the output voltage as expressed by

$$R_H = \frac{{V_H}^2}{P_o} = \frac{5.184(3+D^d)^2}{(1-D^d)^2}. \quad (29)$$

As the duty cycle increases, the ripple rates of the inductor currents exhibit increment trend. In the similar way, the current ripple rates in $L_{1B}$ and $L_{2B}$ within the range of $0 < D^d < 0.5$ are smaller than those of $L_{1A}$ and $L_{2A}$, due to the effect of topology. It is worth noting that the inductor current ripple rate is not only related to the duty cycle but also to the inductance value, operating frequency, and load resistance.

### *E. Robustness of Average Inductor Current*

Fig. 14 showcases the simulation results illustrating the tolerance of the four-phase inductor variations for the average inductor current. As an example, the inductances of $L_{1A}$, $L_{1B}$, $L_{2A}$, and $L_{2B}$ are set to $263\,\mu$H (1.2 times the nominal value), $219\,\mu$H, $175\,\mu$H (0.8 times the nominal value) and $219\,\mu$H (the nominal value), respectively. The simulation results prove that the implementation of the A-DLC ensures the balance of the average inductor current in CCM, despite up to a $20\,\%$ fluctuation in the inductance values. Consequently, the proposed BDC topology demonstrates remarkable robustness to variations of the dc inductors.

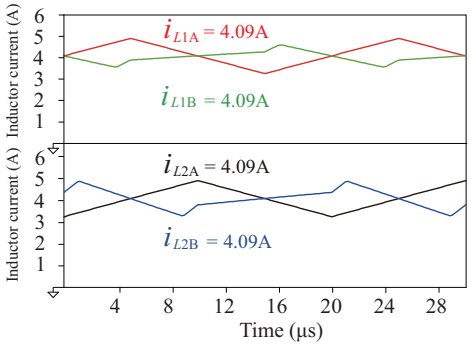



Fig. 14. Tolerances on the average inductor current for the dc inductor variations (400 V to 72 V, 1 kW).

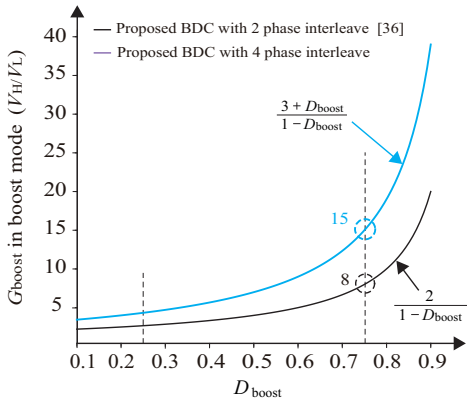



Fig. 15. Voltage conversion ratios versus duty cycle in the boost mode.

## IV. Design Consideration in Main Circuit

### A. Selection of Interleaving Phase Numbers

Fig. 15 illustrates the relationship between voltage conversion ratio and duty cycle for both the two- and four-phase interleaved topologies in the boost mode. It can be observed that employing the four-phase interleaved topology can significantly enhance the voltage conversion ratio. Typically, the duty cycle of a buck/boost converter exists between $0.2$ and $0.8$ while occasionally between $0.3$ and $0.7$. Considering the ripple rates of the inductor currents in the boost mode as depicted in Fig. 13, it is reasonable to operate the converter's duty cycle between $0.25$ and $0.75$ to ensure that the inductor current operates in CCM and to maintain sufficient margin. When the duty cycle is at $0.75$, the voltage ratio for the two-phase interleaved topology is $8$, while it is $15$ for the four-phase interleaved topology.

Aiming to attain the voltage conversion from $72\,\mathrm{V}$ to $400\,\mathrm{V}$–$800\,\mathrm{V}$, a voltage ratio higher than $11.1$ should be accomplished. In addition, further increasing the voltage ratio is necessary to maintain a $800\,\mathrm{V}$ output in consideration of presence of the loads. Moreover, when the input voltage in application scenarios is lower than $72\,\mathrm{V}$ such as $30\,\mathrm{V}$ as depicted in [30] and [33], a higher voltage ratio is required to achieve an output of $800\,\mathrm{V}$. It is obvious from the viewpoints of voltage ratio that a four-phase interleaved topology is more suitable for the wide range of voltage ratio.

### B. Selection of Active Switches

According to (13) and (16), the maximum voltage stress on the active switches is half the sum of the low-side and high-side voltages, in both buck and boost modes. Furthermore, it can be observed from the waveforms in Figs. 5 and 8 that the maximum current flowing through the active switches is two times the average inductor current. Therefore, the active switch should meet the following requirements as denoted by

$$\begin{cases} v_{\mathrm{ds}} > \dfrac{V_{\mathrm{H}}+V_{\mathrm{L}}}{2} \\ i_{\mathrm{ds}} > \begin{cases} (2+\dfrac{4D^{\mathrm{c}}-2}{D^{\mathrm{c}}}\gamma_{L_{1\mathrm{A}},L_{2\mathrm{A}}})I_{L_{\mathrm{A,B}}} & \text{when } D^{\mathrm{d}} \le 0.5 \\ \left(1+\gamma_{L_{\mathrm{A,B}}}\right) I_{L_{\mathrm{A,B}}} & \text{when } D^{d} > 0.5. \end{cases} \end{cases} \tag{30}$$

Considering to the scenario of $800\,\mathrm{V}$ in the high-voltage side, which is shared by two active switches, MOSFETs rated at $650\,\mathrm{V}$ and above are considered suitable for the active switches in the proposed BDC. In particular, the $650\,\mathrm{V}$ is the optimal choice from the viewpoints of low ON-resistance and low gate charging capacitance.

### C. Determination of Operating Frequency

The maximum operating frequency of SiC-MOSFETs can reach up to several hundred kHz in the latest trend of the wide band-gap power devices, and increasing the operating frequency under the same power leads to substantial reduction of the volume of magnetic components. The main switches are commutated in a hard-switching state (e.g., $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$, $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$,$\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$, and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ in buck mode) at the current stage of this research, while the remaining switches operate soft commutations and behave SR. Hence, the switching frequency over a hundred kHz may induce significant amounts of switching losses in the main switches. Therefore, the operating frequency is selected as $50\,\mathrm{kHz}$ for the proposed BDC from the practical point of view.

### D. Design of Inductors

The inductance values of $L_{1\mathrm{A}}$, $L_{1\mathrm{B}}$, $L_{2\mathrm{A}}$ and $L_{2\mathrm{B}}$ can be obtained using the following equations:

$$\begin{cases} L_{1\mathrm{A}} = L_{2\mathrm{A}} = \dfrac{V_{\mathrm{L}}D^{\mathrm{d}}}{2\gamma_{L_{1\mathrm{A}},L_{2\mathrm{A}}}I_{L_{\mathrm{A,B}}}f_{\mathrm{s}}} \\ L_{1\mathrm{B}} = L_{2\mathrm{B}} = \dfrac{V_{\mathrm{L}}D^{\mathrm{d}}}{2\gamma_{L_{1\mathrm{B}},L_{2\mathrm{B}}}I_{L_{\mathrm{A,B}}}f_{\mathrm{s}}}. \end{cases} \tag{31}$$

In order to ensure that the inductor currents operate in CCM, the values of $\gamma_{L_{1\mathrm{A}},L_{2\mathrm{A}}}$ and $\gamma_{L_{1\mathrm{B}},L_{2\mathrm{B}}}$ must be less than 1. In addition, the selected inductors should be able to accommodate the maximum current according to the following requirements.

$$\begin{cases} i_{L_{1\mathrm{A}}} = i_{L_{2\mathrm{A}}} > (1+\gamma_{L_{1\mathrm{A}},L_{2\mathrm{A}}})I_{L_{\mathrm{A,B}}} \\ i_{L_{1\mathrm{B}}} = i_{L_{2\mathrm{B}}} > (1+\gamma_{L_{1\mathrm{B}},L_{2\mathrm{B}}})I_{L_{\mathrm{A,B}}}. \end{cases} \tag{32}$$

### E. Design of Capacitors

Assuming $L_{1A}$, $L_{2A}$, $L_{1B}$, and $L_{2B}$ have the same values, the ripple current on the low voltage side in the four-phase interleaved topology can be approximately expressed as

$$\Delta I_{\mathrm{Low}} = \begin{cases} \dfrac{(0.5-D^{\mathrm{d}})V_{\mathrm{H}}}{(3+D^{\mathrm{d}})Lf_{\mathrm{s}}} & 0 < D^{\mathrm{d}} \le 0.5 \\ \dfrac{(D^{\mathrm{d}}-0.5)(3-4D^{\mathrm{d}})V_{\mathrm{H}}}{(3+D^{\mathrm{d}})Lf_{\mathrm{s}}} & 0.5 < D^{\mathrm{d}} \le 0.75 \\ \dfrac{(1-D^{\mathrm{d}})(4D^{\mathrm{d}}-3)V_{\mathrm{H}}}{(3+D^{\mathrm{d}})Lf_{\mathrm{s}}} & 0.75 < D^{\mathrm{d}} < 1. \end{cases} \tag{33}$$

The maximum charge increment stored in $C_{\mathrm{L}}$ during one cycle in the buck mode is as

$$\Delta \mathrm{Q} = \frac{\Delta I_{\mathrm{Low}}}{8f_{\mathrm{s}}}. \tag{34}$$

Therefore, the minimum capacitance value of $C_{\mathrm{L}}$ can be determined as

$$C_{\mathrm{L}} = \frac{\Delta I_{\mathrm{Low}}}{8\Delta V_{C_{\mathrm{L}}} f_{\mathrm{s}}}. \tag{35}$$

The charge-pump capacitors $C_{1\mathrm{B}}$ and $C_{2\mathrm{B}}$ can also be calculated as

$$C_{1\mathrm{B}} \ge \mathrm{MIN}\left(\frac{I_{L_{1\mathrm{B}}}}{2\Delta V_{C_{1\mathrm{B}}} f_{\mathrm{s}}}, \frac{(1-D^{\mathrm{d}})I_{L_{1\mathrm{B}}}}{\Delta V_{C_{1\mathrm{B}}} f_{\mathrm{s}}}\right) \tag{36}$$

$$C_{2\mathrm{B}} \ge \mathrm{MIN}\left(\frac{I_{L_{2\mathrm{B}}}}{2\Delta V_{C_{2\mathrm{B}}} f_{\mathrm{s}}}, \frac{(1-D^{\mathrm{d}})I_{L_{2\mathrm{B}}}}{\Delta V_{C_{2\mathrm{B}}} f_{\mathrm{s}}}\right). \tag{37}$$

Similarly, the filter capacitors of high-voltage side $C_{\mathrm{H1}}$ and $C_{\mathrm{H2}}$ can also be expressed as:

$$C_{\mathrm{H1}} \ge \mathrm{MAX}\left(\frac{I_{\mathrm{H}}}{2\Delta V_{C_{\mathrm{H1}}} f_{\mathrm{s}}}, \frac{D^{\mathrm{d}} I_{\mathrm{H}}}{\Delta V_{C_{\mathrm{H1}}} f_{\mathrm{s}}}\right) \tag{38}$$

$$C_{\mathrm{H2}} \ge \mathrm{MAX}\left(\frac{I_{\mathrm{H}}}{2\Delta V_{C_{\mathrm{H2}}} f_{\mathrm{s}}}, \frac{D^{\mathrm{d}} I_{\mathrm{H}}}{\Delta V_{C_{\mathrm{H2}}} f_{\mathrm{s}}}\right). \tag{39}$$

### F. ZVS Range

Referring to Figs. 5 and 6, it's evident that the minimum current through $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}$ equals that through $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$ and $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}$ for $0 < D^{\mathrm{c}} < 0.5$, while the minimum current flowing through $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}$ exceeds that through $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$ and $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}$ for $0.5 \le D^{\mathrm{c}} < 1$. Consequently, when $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$ and $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}$ meet the ZVS conditions, $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}$ naturally satisfy the ZVS conditions too. In order to ensure the successful completion of ZVS turn-on and turn-off commutations in the buck mode with the SR switches, the minimum energy stored in the dc inductors $L_{1\mathrm{B}}$ and $L_{2\mathrm{B}}$ should completely discharge $C_{\mathrm{oss}}$ in $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$, $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}$ and charge in $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$, $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ as described by

$$\begin{cases} L_{1\mathrm{B}}(i_{L_{1\mathrm{B}}})^2 > C_{\mathrm{oss}}(V_{\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B,ds}}})^2 + C_{\mathrm{oss}}(V_{\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B,ds}}})^2 \\ L_{2\mathrm{B}}(i_{L_{2\mathrm{B}}})^2 > C_{\mathrm{oss}}(V_{\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B,ds}}})^2 + C_{\mathrm{oss}}(V_{\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B,ds}}})^2. \end{cases} \tag{40}$$

where $C_{\mathrm{oss}}$ represents the output capacitance of the power MOSFETs.

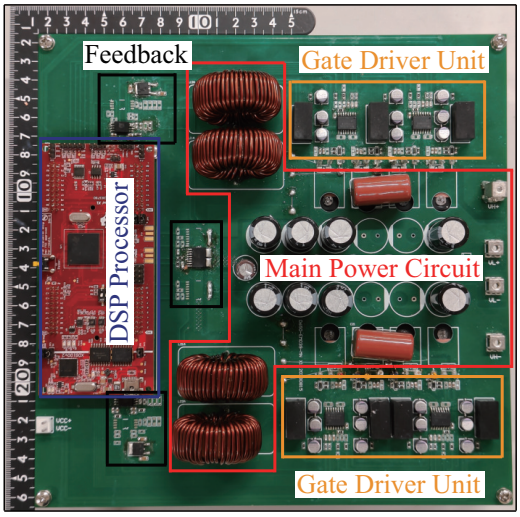



Fig. 16. Exterior appearance of 1 kW-50 kHz prototype.

Furthermore, by combining (5), (22) and (40), the critical load condition in the low-voltage side can be determined as

$$\left(\frac{(1-D^{\mathrm{c}})(4-D^{\mathrm{c}})}{2Lf_{\mathrm{s}}} + \frac{4(4-D^{\mathrm{c}})}{D^{\mathrm{c}}}\sqrt{\frac{C_{\mathrm{oss}}}{2L}}\right) R_{\mathrm{L}} = 1. \tag{41}$$

Referring to Figs. 8 and 9, the minimum current through $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$ exceeds that through $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$ and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ for $0 < D^{\mathrm{d}} \le 0.5$, while they are identical for $0.5 < D^{\mathrm{d}} < 1$. Therefore, once $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$ and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ meet the ZVS condition, $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$ naturally satisfy the ZVS conditions. In order to ensure the successful completion of ZVS in the boost mode, it is also necessary to satisfy the essential condition that the minimum energy stored in inductor $L_{1\mathrm{B}}$ and $L_{2\mathrm{B}}$ fully discharges $C_{\mathrm{oss}}$ in $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$, $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ and charge in $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$, $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}$ as described by

$$\begin{cases} L_{1\mathrm{B}}(i_{L_{1\mathrm{B}}})^2 > C_{\mathrm{oss}}(V_{\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B,ds}}})^2 + C_{\mathrm{oss}}(V_{\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B,ds}}})^2 \\ L_{2\mathrm{B}}(i_{L_{2\mathrm{B}}})^2 > C_{\mathrm{oss}}(V_{\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B,ds}}})^2 + C_{\mathrm{oss}}(V_{\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B,ds}}})^2. \end{cases} \tag{42}$$

Furthermore, by combining (8), (26) and (42), the critical load condition in the high-voltage side can be expressed as

$$\left(\frac{D^{\mathrm{d}}(1-D^{\mathrm{d}})^2}{2(3+D^{\mathrm{d}})Lf_{\mathrm{s}}} + \frac{4(1-D^{\mathrm{d}})}{3+D^{\mathrm{d}}}\sqrt{\frac{C_{\mathrm{oss}}}{2L}}\right) R_{\mathrm{H}} = 1. \tag{43}$$

## V. Experimental Verification

A performance of the F4P-ICPBDC is investigated by experiment of 1 kW-50 kHz prototype. The exterior appearance of the prototype is portrayed in Fig. 16, and the specifications are listed in TABLE IV, respectively. All the active switches are implemented with SiC-MOSFETs (IMW65R027M1H, 650 V, 47 A, 27 mΩ, 244 pF), all of which are driven by isolated gate drivers (UCC21520,Texas Instruments). The power controller is comprised by a DSP board development kit (LAUNCHXL-F28379D, Texas Instruments) with TMS320F28379D microcontroller.

TABLE IV
SPECIFICATIONS OF THE F4P-ICPBDC CONVERTER

| Item | Symbol | Value [unit] |
|---|---|---|
| High-side voltage | $V_{\mathrm{H}}$ | $400-800$ [V] |
| Low-side voltage | $V_{\mathrm{L}}$ | 72 [V] |
| Output power rating | $P_{\mathrm{o}}$ | 1 [kW] |
| Switching frequency | $f_{\mathrm{s}}$ | 50 [kHz] |
| DC inductors | $L_{1\mathrm{A}}, L_{1\mathrm{B}},$ | 219 [$\mu$H]/15A |
| (HHBC24N-2R0A0219V) | $L_{2\mathrm{A}}, L_{2\mathrm{B}}$ | (Fe-Si) |
| High-side capacitors | $C_{\mathrm{H1}}, C_{\mathrm{H2}}$ | 272 [$\mu$F]/500V |
| Low-side capacitor | $C_{\mathrm{L}}$ | 600 [$\mu$F]/100V |
| Charge pump capacitors | $C_{1\mathrm{B}}, C_{2\mathrm{B}}$ | 10 [$\mu$F] /450V |
| Power MOSFETs | $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$–$\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}$ | IMW65R027M1H |
| DSP controller chip | | TMS320F28379D |
| Voltage sampling chip | | AMC1311BDWR |
| Current sampling chip | | CZ3A02 |

### A. Steady-State Performances in the Buck Mode

*1) 400 V to 72 V:* Fig. 17 provides a detailed depiction of key experimental waveforms in a buck mode, where the dc input voltage $V_{\mathrm{H}}$ and the load resistance $R_{\mathrm{L}}$ are set as 400 V and 5.184 Ω, respectively. It can be observed in Fig. 17(a) that the sequential operation of the main switches $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$, $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$, $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$, and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ attain with a phase shift angle of 90°. The duty cycles for $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$, $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$ are consistently fixed at 0.5, while those for $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$ and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ are set at 0.63. The current waveforms of the dc inductors are shown in Fig. 17(b). The average currents for $L_{1\mathrm{A}}$, $L_{1\mathrm{B}}$, $L_{2\mathrm{A}}$, and $L_{2\mathrm{B}}$, are measured as $I_{L_{1\mathrm{A}}} = 3.98\,\mathrm{A}$, $I_{L_{1\mathrm{B}}} = 4.01\,\mathrm{A}$, $I_{L_{2\mathrm{A}}} = 4.02\,\mathrm{A}$, and $I_{L_{2\mathrm{B}}} = 3.97\,\mathrm{A}$ respectively, thus a well-balanced average inductor current can be realized in the proposed BDC with A-DLC1. Moreover, the current ripples for $i_{L_{1\mathrm{A}}}$, $i_{L_{1\mathrm{B}}}$, $i_{L_{2\mathrm{A}}}$, and $i_{L_{2\mathrm{B}}}$ are observed as $\Delta I_{L_{1\mathrm{A}}} = 3.19\,\mathrm{A}$, $\Delta I_{L_{1\mathrm{B}}} = 2.49\,\mathrm{A}$, $\Delta I_{L_{2\mathrm{A}}} = 3.26\,\mathrm{A}$, and $\Delta I_{L_{2\mathrm{B}}} = 2.47\,\mathrm{A}$, respectively, which have good agreement with (19) and (20). The current ripple rates for these inductors are found to be 0.40, 0.31, 0.41, and 0.31, respectively, corresponding to the theoretical values in (21) and (22). These experimental results clarify the validity of the current ripple analysis for duty cycles in the range of $0.5 \le D^{\mathrm{c}} < 1$.

Fig. 17(c) shows that the current ripple rates for $i_{L1}$, and $i_{L2}$ are further reduced to 0.16 and 0.15, respectively due to the interleaved switching patterns. Moreover, the total current of the interleaved inductors, $i_{Lt}$ has small current ripple rate, allowing for a reduction in the use of filtering capacitors. Fig. 17(d) presents the steady-state voltages across the capacitors. The measured values are, $V_{C_{1\mathrm{B}}} = 94.5\,\mathrm{V}$, $V_{C_{2\mathrm{B}}} = 94.5\,\mathrm{V}$, $V_{C_{\mathrm{H1}}} = 236.2\,\mathrm{V}$, $V_{C_{\mathrm{H2}}} = 233.7\,\mathrm{V}$, and

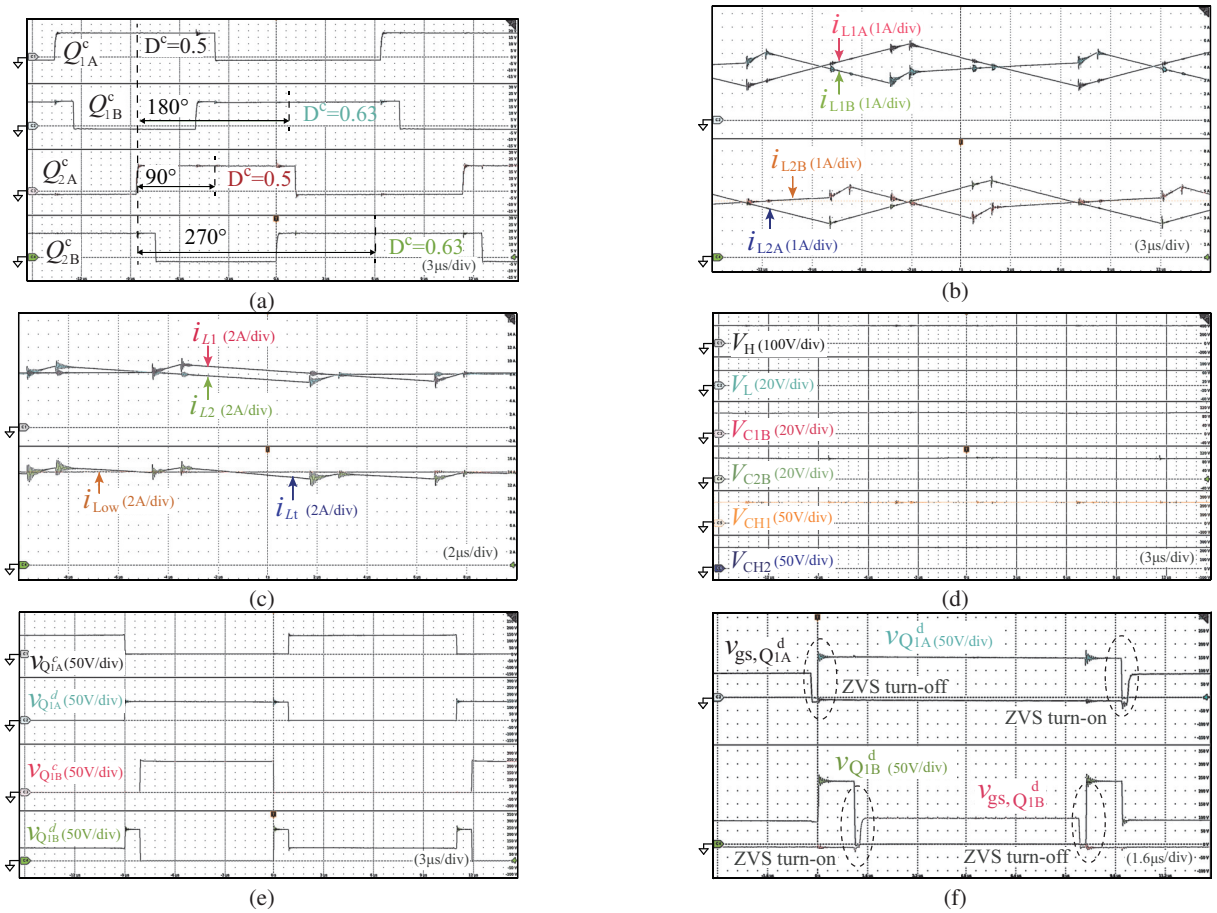



Fig. 17. Observed waveforms in a buck mode with $V_{\mathrm{H}} = 400\,\mathrm{V}$ and $R_{\mathrm{L}} = 5.184\,\Omega$ for $V_{\mathrm{L}} = 72\,\mathrm{V}$: (a) gate signals, (b) dc inductor currents, (c) high and low-side unit dc inductor currents and the output currents, (d) capacitor voltages, (e) power switch voltage stresses, and (f) synchronous rectifier voltages.

$V_{\rm H} = 400\,{\rm V}$, corresponding well with (11) and (12). Additionally, the output voltage is controlled as $V_{\rm L} = 72\,{\rm V}$ in accordance with the command value, whereby the validity of (9) is revealed.

Fig. 17(e) illustrates the steady-state voltage stresses on switches $\rm Q^c_{1A}$, $\rm Q^d_{1A}$, $\rm Q^c_{1B}$, and $\rm Q^d_{1B}$, whereby $V_{\rm Q^c_{1A}} = 141.3\,{\rm V}$, $V_{\rm Q^d_{1A}} = 142.1\,{\rm V}$, $V_{\rm Q^c_{1B}} = 236.1\,{\rm V}$ and $V_{\rm Q^d_{1B}} = 235.8\,{\rm V}$ are lower than the high side voltage $V_{\rm H} = 400\,{\rm V}$. It should be remarked herein some voltage stresses are even lower than half of $V_{\rm H}$. The black dash-circles in Fig. 17(f) reveal the successful achievement of both ZVS turn-ON and turn-OFF on the counterpart switches $\rm Q^d_{1A}$, $\rm Q^d_{1B}$ under the condition of SR. By substituting the relevant parameters, the critical load resistance for achieving ZVS in the buck mode can be determined to be $R_{\rm L} = 13.7\,\Omega$. It is worthwhile noting that due to the hard-switching operation of the main switches, rapid discharge of the parasitic capacitance $\rm C_{oss}$ inherently occurs at the turn-on transitions, which leads to the voltage oscillations. Consequently, the voltage oscillations induced by the turn-on of the main switches will inevitably provoke voltage oscillations upon the turn-off of SR switches.

*2) 800 V to 72 V:* Fig. 18 presents the key experimental waveforms in a buck mode, where the dc input voltage $V_{\rm H}$ and the load resistance $R_{\rm L}$ are set at $800\,{\rm V}$ and $5.184\,\Omega$, respectively. It can be observed in Fig. 18(a) that the sequential operations of the main switches $\rm Q^c_{1A}$, $\rm Q^c_{2A}$, $\rm Q^c_{1B}$, and $\rm Q^c_{2B}$ exhibit a phase shift of $90\,^\circ$. In this condition, the A-DLC1 is inactive and the duty cycle for all the main switches is consistently set at 0.34. Fig. 18(b) displays the current waveforms of the dc inductors. The average currents for $L_{1\rm A}$, $L_{1\rm B}$, $L_{2\rm A}$, and $L_{2\rm B}$ are measured as $I_{L_{1\rm A}} = 3.73\,{\rm A}$, $I_{L_{1\rm B}} = 3.69\,{\rm A}$, $I_{L_{2\rm A}} = 3.77\,{\rm A}$, and $I_{L_{2\rm B}} = 3.72\,{\rm A}$, respectively. These values also demonstrate a well-balanced average inductor current. Additionally, the current ripples for $i_{L_{1\rm A}}$, $i_{L_{1\rm B}}$, $i_{L_{2\rm A}}$, and $i_{L_{2\rm B}}$ are $\Delta I_{L_{1\rm A}} = 4.12\,{\rm A}$, $\Delta I_{L_{1\rm B}} = 4.07\,{\rm A}$, $\Delta I_{L_{2\rm A}} = 4.18\,{\rm A}$, and $\Delta I_{L_{2\rm B}} = 4.15\,{\rm A}$, respectively, which has good agreement with (17). The current ripple rates for these inductors are found to be 0.55, 0.55, 0.55, and 0.56, respectively, corresponding to the theoretical values in (18). Hence, the validity of the current ripple analysis for duty cycles is clarified in the range of $0 < D^{\rm c} < 0.5$.

Due to the adoption of interleaved switching topologies, the current ripple rates for $i_{L1}$, and $i_{L2}$ are further reduced to 0.14 and 0.15, respectively as shown in Fig. 18(c). Similarly, the total current of the interleaved inductors, $i_{Lt}$ has small current ripple rate, which allows for a reduction in the use

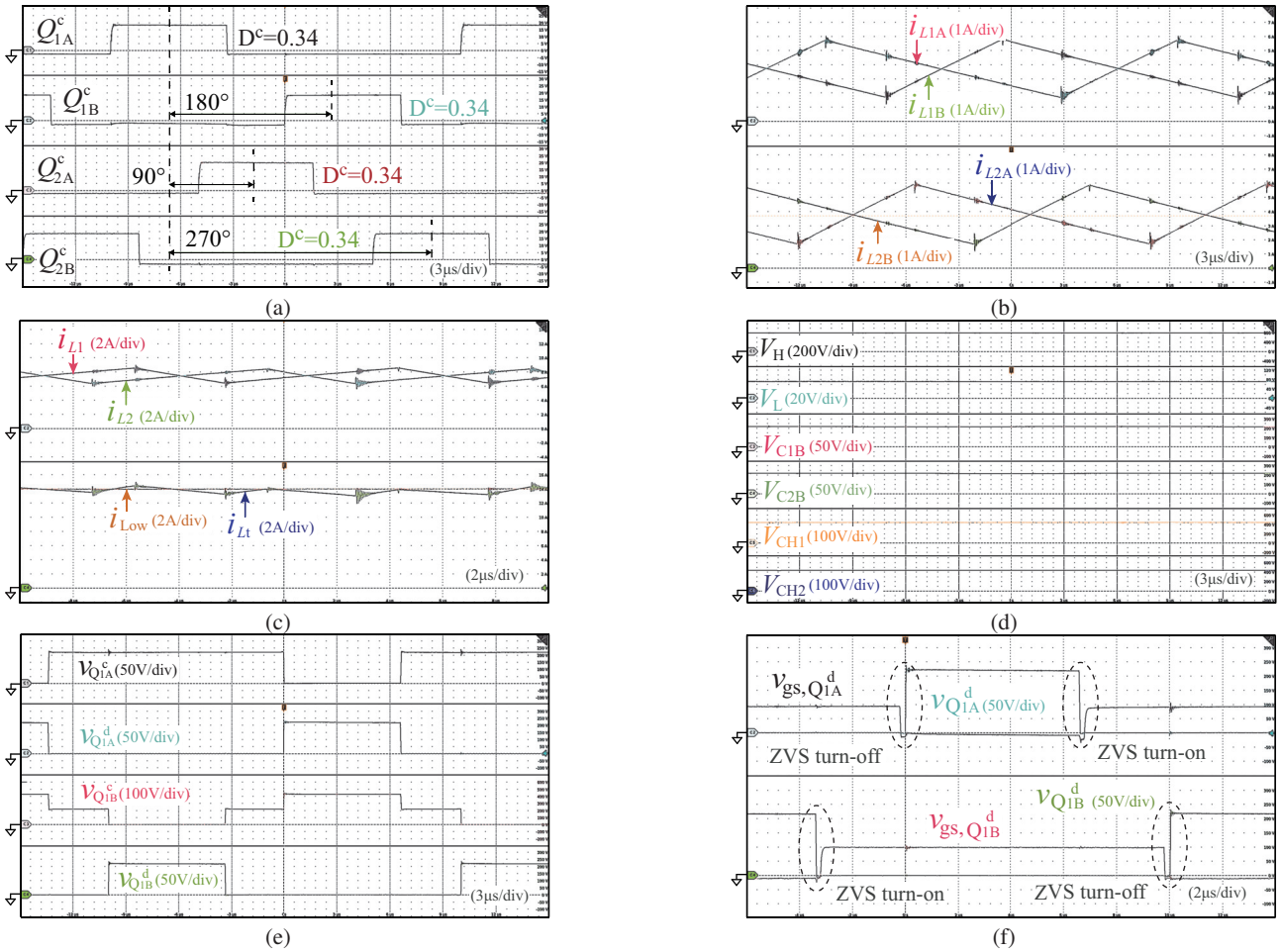



Fig. 18. Observed waveforms in a buck mode with $V_{\rm H} = 800\,{\rm V}$ and $R_{\rm L} = 5.184\,\Omega$ for $V_{\rm L} = 72\,{\rm V}$: (a) gate signals, (b) dc inductor currents, (c) high and low-side unit dc inductor currents and the output currents, (d) capacitor voltages, (e) power switch voltage stresses, and (f) synchronous rectifier voltages.

of filtering capacitors. Fig. 18(d) shows that the steady-state voltages across the capacitors are $V_{C_{1B}} = 216.9\,\mathrm{V}$, $V_{C_{2B}} = 217.8\,\mathrm{V}$, $V_{C_{H1}} = 439.2\,\mathrm{V}$, $V_{C_{H2}} = 436.9\,\mathrm{V}$, and $V_H = 800\,\mathrm{V}$, corresponding well with the theoretical values (11) and (12).

Fig. 18(e) illustrates the steady-state turn-off voltage stresses on switches $Q^c_{1A}$, $Q^d_{1A}$, $Q^c_{1B}$, and $Q^d_{1B}$. The observed values $V_{Q^c_{1A}} = 222.1\,\mathrm{V}$, $V_{Q^d_{1A}} = 221.0\,\mathrm{V}$, $V_{Q^c_{1B}} = 431.3\,\mathrm{V}$ and $V_{Q^d_{1B}} = 220.3\,\mathrm{V}$ are lower than the high voltage $V_H = 800\,\mathrm{V}$. Additionally, the black dash-circles in Fig. 18(f) reveal the successful achievement of both ZVS turn-ON and ZVS turn-OFF commutations on the counterpart switches $Q^d_{1A}$, $Q^d_{1B}$ under the condition of SR.

### B. Steady-State Performances in the Boost Mode

*1) 72 V to 400 V:* Fig. 19 illustrates the key experimental waveforms in the boost mode, where the dc input voltage $V_L$ and the load resistance $R_H$ are set to 72 V and 160 Ω, respectively. It can be observed in Fig. 19(a) that the main switches $Q^d_{1A}$, $Q^d_{2A}$, $Q^d_{1B}$, and $Q^d_{2B}$ are driven in the sequential manner with a phase shift angle of 90°. The duty cycles for $Q^d_{1A}$, $Q^d_{2A}$ are consistently fixed at 0.5, while those for $Q^d_{1B}$ and $Q^d_{2B}$ are set at 0.41. The current waveforms of the dc inductors are depicted in Fig. 19(b). The average currents through $L_{1A}$, $L_{1B}$, $L_{2A}$, and $L_{2B}$, are obtained as $I_{L_{1A}} = 4.04\,\mathrm{A}$, $I_{L_{1B}} = 4.10\,\mathrm{A}$, $I_{L_{2A}} = 4.07\,\mathrm{A}$, and $I_{L_{2B}} = 4.11\,\mathrm{A}$, respectively, which implies that a well-balanced average inductor current can be achieved in the proposed converter with the A-DLC2. The current ripples for $i_{L_{1A}}$, $i_{L_{1B}}$, $i_{L_{2A}}$, and $i_{L_{2B}}$ are $\Delta I_{L_{1A}} = 3.12\,\mathrm{A}$, $\Delta I_{L_{1B}} = 2.61\,\mathrm{A}$, $\Delta I_{L_{2A}} = 3.10\,\mathrm{A}$, and $\Delta I_{L_{2B}} = 2.67\,\mathrm{A}$, respectively, which has good agreement with (23) and (24). The current ripple rates for these inductors are found to be 0.39, 0.32, 0.38, and 0.32, respectively, corresponding to the theoretical analyses in (25) and (26). Thus, the validity of the current ripple analysis for duty cycles in the range of $0 < D^d \leq 0.5$ is verified herein.

As shown in Fig. 19(c), the current ripple rates for $i_{L1}$, and $i_{L2}$ are further reduced to 0.13 and 0.14, respectively due to the adoption of interleaved switching patterns. Fig. 19(d) presents the steady-state voltages across the capacitors. The measured values $V_{C_{1B}} = 94.7\,\mathrm{V}$, $V_{C_{2B}} = 93.9\,\mathrm{V}$, $V_{C_{H1}} = 235.9\,\mathrm{V}$, $V_{C_{H2}} = 232.7\,\mathrm{V}$, and $V_L = 72\,\mathrm{V}$ correspond well with (14) and (15). Additionally, the output voltage is recorded as $V_H = 400\,\mathrm{V}$, whereby the validity of (10) is revealed.

Fig. 19(e) illustrates the voltage stresses on switches $Q^c_{1A}$, $Q^d_{1A}$, $Q^c_{1B}$, and $Q^d_{1B}$. The observed steady-state turn-off values $V_{Q^c_{1A}} = 143.5\,\mathrm{V}$, $V_{Q^d_{1A}} = 140.8\,\mathrm{V}$, $V_{Q^c_{1B}} = 238.2\,\mathrm{V}$ and

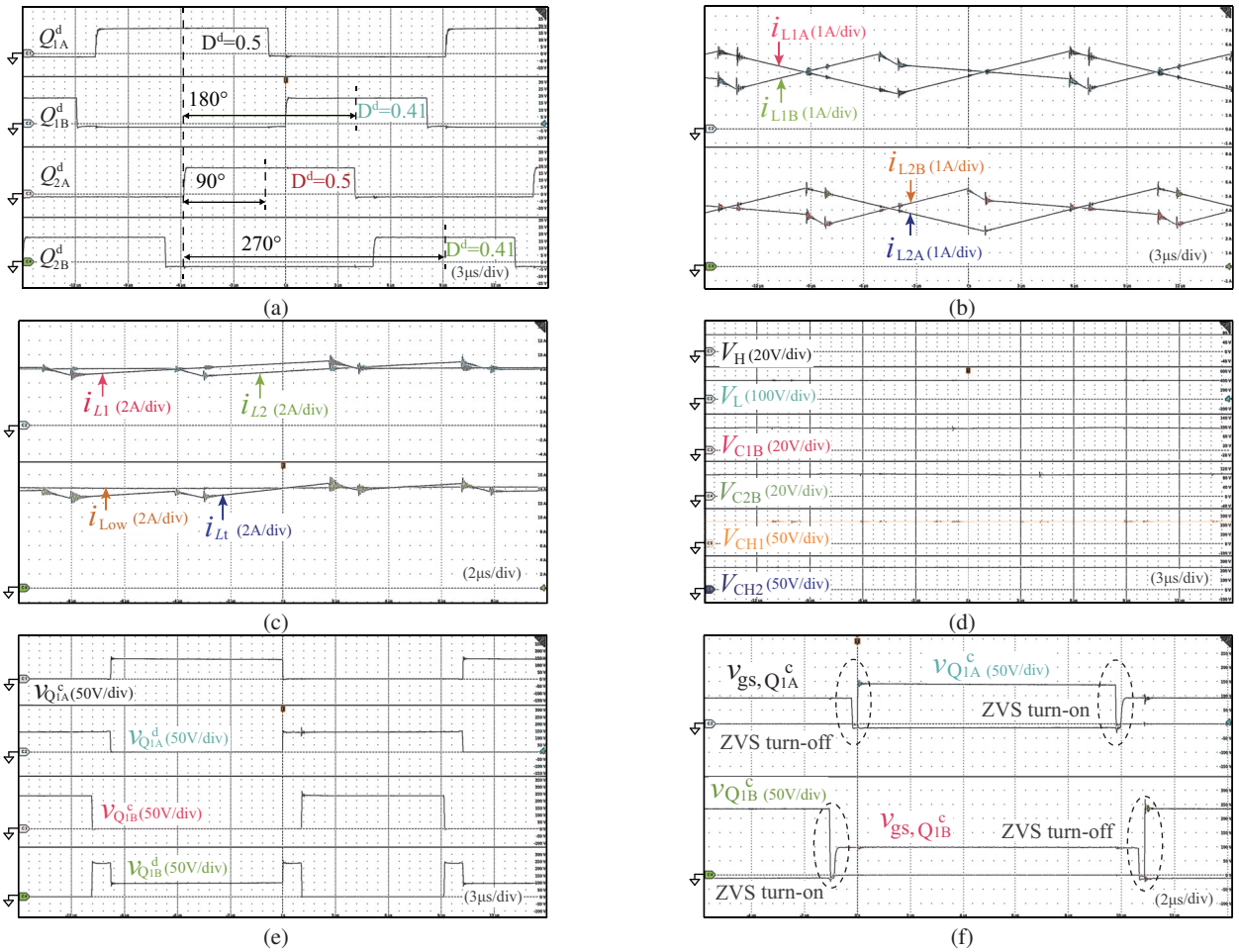



Fig. 19. Observed waveforms in a boost mode with $V_L = 72\,\mathrm{V}$ and $R_H = 160\,\Omega$ for $V_H = 400\,\mathrm{V}$: (a) gate signals, (b) dc inductor currents, (c) high and low-side unit dc inductor currents and the input currents, (d) capacitor voltages, (e) power switch voltage stresses, and (f) synchronous rectifier voltages.

$V_{Q^d_{1B}} = 237.6\,\text{V}$ are lower than $V_H = 400\,\text{V}$. It should be remarked herein that some voltage stresses are even lower than half of $V_H$. Furthermore, the black dash-circles in Fig. 19(f) reveal the successful achievement of both the ZVS turn-ON and ZVS turn-OFF commutations on the counterpart switches $Q^c_{1A}$, $Q^c_{1B}$ under the condition of SR. Accordingly, the critical resistance of ZVS in the boost mode can be determined as $R_H = 411.5\,\Omega$ for the output voltage of 400 V.

*2) 72 V to 800 V:* Fig. 20 displays the critical experimental waveforms in a boost mode, where the dc input voltage $V_L$ and the load resistance $R_H$ are set at 72 V and 640 Ω, respectively. It can be observed in Fig. 20(a) that the sequential operations of the main switches $Q^d_{1A}$, $Q^d_{2A}$, $Q^d_{1B}$, and $Q^d_{2B}$ exhibit a phase shift of 90°. During this period, the A-DLC2 is inactive and the duty cycle for all the main switches is set at 0.68. The current waveforms of the inductors are shown in Fig. 20(b). The average currents for $L_{1A}$, $L_{1B}$, $L_{2A}$, and $L_{2B}$, are measured as $I_{L_{1A}} = 3.79\,\text{A}$, $I_{L_{1B}} = 3.86\,\text{A}$, $I_{L_{2A}} = 3.81\,\text{A}$, and $I_{L_{2B}} = 3.83\,\text{A}$, respectively. Thus, the average inductor currents are well-balanced in the proposed BDC. The current ripples for $i_{L_{1A}}$, $i_{L_{1B}}$, $i_{L_{2A}}$, and $i_{L_{2B}}$ are $\Delta I_{L_{1A}} = 4.13\,\text{A}$, $\Delta I_{L_{1B}} = 4.10\,\text{A}$, $\Delta I_{L_{2A}} = 4.14\,\text{A}$, and $\Delta I_{L_{2B}} = 4.17\,\text{A}$, respectively, which has good agreement with (27). The current ripple rates for these inductors are found as 0.54, 0.53, 0.54 and 0.55, respectively, which agree well with the theoretical values in (28). These results validate the precision of the current ripple analysis for duty cycles in the range of $0.5 < D^d < 1$.

Due to the interleaved switching patterns, the current ripple rates for $i_{L1}$, and $i_{L2}$ are further reduced to 0.14 and 0.15, respectively as shown in Fig. 20(c). Fig. 20(d) shows that the steady-state voltages across the capacitors are $V_{C_{1B}} = 217.5\,\text{V}$, $V_{C_{2B}} = 218.8\,\text{V}$, $V_{C_{H1}} = 438.3\,\text{V}$, $V_{C_{H2}} = 436.8\,\text{V}$, and $V_L = 72\,\text{V}$, corresponding well with (14) and (15). The output voltage is obtained as $V_H = 800\,\text{V}$.

Fig. 20(e) illustrates the voltage stresses on $Q^c_{1A}$, $Q^d_{1A}$, $Q^c_{1B}$, and $Q^d_{1B}$. The steady-state turn-off voltages are observed as $V_{Q^c_{1A}} = 223.9\,\text{V}$, $V_{Q^d_{1A}} = 225.7\,\text{V}$, $V_{Q^c_{1B}} = 436.8\,\text{V}$ and $V_{Q^d_{1B}} = 222.4\,\text{V}$. It should be remarked herein that voltage stresses of a few power devices are even lower than half of $V_H$. Additionally, the successful achievements of both the ZVS turn-ON and ZVS turn-OFF commutations on the counterpart switches $Q^c_{1A}$, $Q^c_{1B}$ are observed under the condition of SR in Fig. 20(f). The critical resistance of ZVS for the output voltage of 800 V can be determined as $R_H = 890.5\,\Omega$.

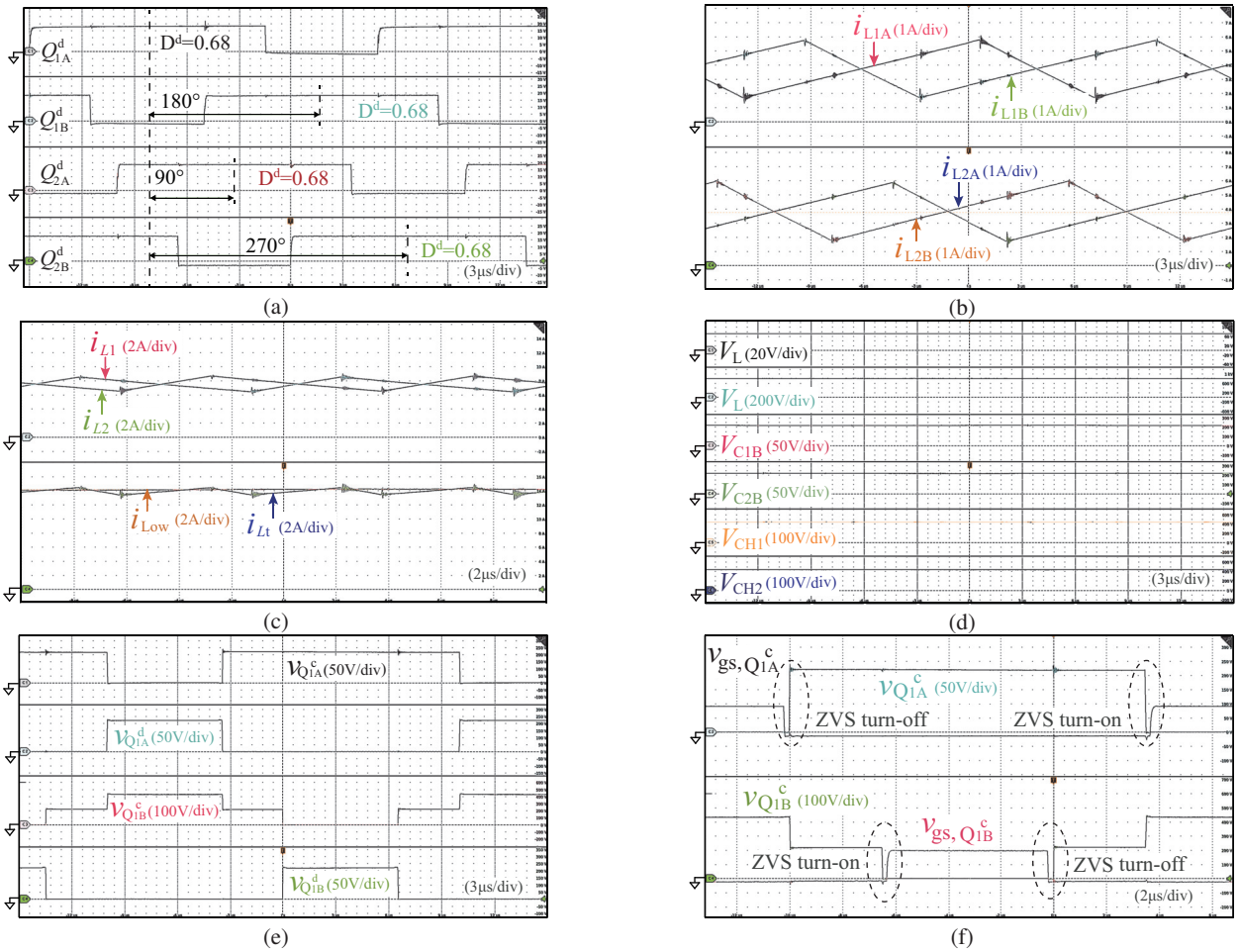



Fig. 20. Observed waveforms in a boost mode with $V_L = 72\,\text{V}$ and $R_H = 640\,\Omega$ for $V_H = 800\,\text{V}$: (a) gate signals, (b) dc inductor currents, (c) high and low-side unit dc inductor currents and the input currents, (d) capacitor voltages, (e) power switch voltage stresses, and (f) synchronous rectifier voltages.

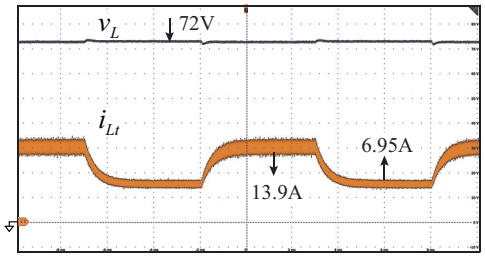



Fig. 21. Transient waveforms of the inductor current and output voltage in the buck mode,(10 V/div, 5 A/div, 2 ms/div).

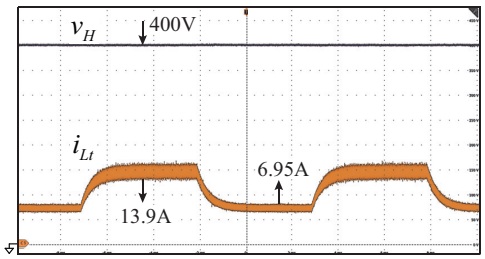



Fig. 22. Transient waveforms of the inductor current and output voltage in the boost mode (50 V/div, 5 A/div, 2 ms/div).

### C. Dynamic Performances

Fig. 21 illustrates the waveforms of inductor current $i_{Lt}$ and output voltage $V_{\mathrm{L}}$ in a buck mode where the input voltage is fixed at $V_{\mathrm{H}} = 400\,\mathrm{V}$ but the load resistance periodically exchanges between $5.18\,\Omega$ for 1 kW to $10.36\,\Omega$ (500 W). It is evident from the transitional performances that $V_{\mathrm{L}}$ is regulated at 72 V regardless of the load variations

In a similar way, Fig. 22 depicts the waveforms of inductor current $i_{Lt}$ and output voltage in the boost mode, when the input voltage is $V_{\mathrm{H}} = 72\,\mathrm{V}$, and the load resistance periodically varies from $160\,\Omega$ (1 kW) to $320\,\Omega$ (500 W). It is evident from the dynamical waveforms that the output voltage $V_{\mathrm{H}}$ is well controlled at 400 V while the load resistance exchanges between the two sets of values.

### D. Power Conversion Efficiencies

The actual efficiencies of the F4P-ICPBDC with the A-DLC is evaluated for the buck / boost modes by the closed-loop controller scheme with two sets of $V_{\mathrm{H}}$: 400 V and 800 V. As displayed in Fig. 23, the maximum efficiencies are recorded as 98.3 % and 96.9 % for $V_{\mathrm{H}} = 400\,\mathrm{V}$ and 800 V respectively in the buck mode. The maximum efficiencies are 97.6 % and 96.9 % respectively for $V_{\mathrm{H}} = 400\,\mathrm{V}$ and 800 V in the boost mode, as indicated in Fig. 24. Therefore, the high efficiencies of the proposed F4P-ICPBDC are actually verified in both the power flows. In particular, over 98 % efficiency attains in the 60 %–100 % load ratios of the buck mode (400 V to 72 V).

### E. Comparison with Existing BDCs

In order to reveal the performance of the proposed BDC, a comprehensive comparison with the existing BDC topologies from the literatures [27]–[36], are summarized in TABLE V

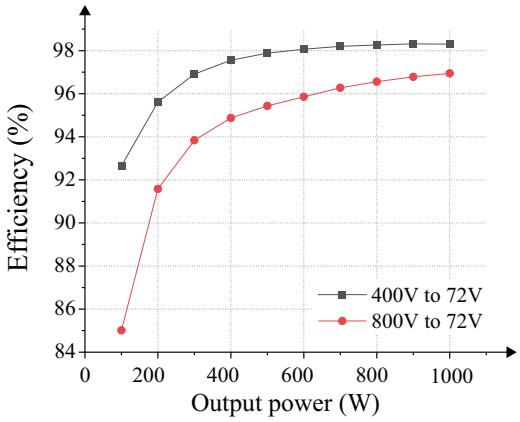



Fig. 23. Actual efficiencies in a buck mode (measured by YOKOGAWA WT1800 power analyzer).

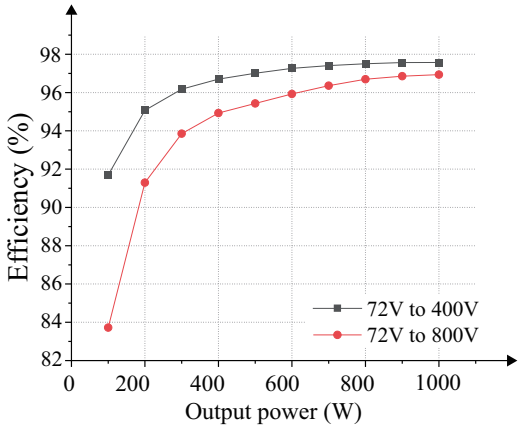



Fig. 24. Actual efficiencies in a boost mode (measured by YOKOGAWA WT1800 power analyzer).

as well as the descriptions in Section I. The higher voltage ratio and higher efficiency can attain by the proposed BDC while the counts of the magnetic components are relatively high. The passive components can be reduced by adopting the magnetic integration of the dc inductors. Employment of SiC-MOSFETs is dedicated to achieving the high efficiency despite eight active switches in the four-phase structure.

The characteristics of SiC-MOSFETs, i.e. faster switching speeds and the lower ON-resistance contribute to reduction of switching losses and promotion of overall efficiency of converter even with hard switching. Besides, the efficiency is further optimized by the proposed BDC, due to Zero-Voltage Switching (ZVS) achievable in the SR switches. In addition, 800 V dc voltage in the input or output side is shared by two active switches in the proposed BDC. Accordingly, 650 V-class SiC-MOSFET is irreplaceable for the F4P-ICPBDC topology.

## VI. Conclusions

The F4P-ICPBDC topology has been proposed in this article, and its operating principle and the excellent performance have been demonstrated in addition to the sound amount

TABLE V
COMPARISON OF DIFFERENT NON-ISOLATED BIDIRECTIONAL DC-DC CONVERTERS

| Ref. | Peak Efficiency | | Voltage ratio | | Components | Specifications | Maximum device voltage stress | | $I_L$ balance |
|---|---|---|---|---|---|---|---|---|---|
| | Boost | Buck | Boost | Buck | | | Capacitors | MOSFETs | |
| [27] | 97.5% | 94.3% | $\frac{1}{(1-D_{\text{boost}})^2}$ | $D_{\text{buck}}^2$ | L:2; C:3 SW:4 | 25V/250V 160W/Si 30kHz/PWM | $U_{\text{high}}$ | $\frac{(2-D_{\text{boost}})U_{\text{high}}}{1-D_{\text{boost}}}$ | D = 0.5 |
| [28] | 95.2% | 95.3% | $\frac{2}{1-D_{\text{boost}}}$ | $\frac{D_{\text{buck}}}{2}$ | L:2; C:4 SW:5 | 50-120V/400V 1kW/Si 20kHz/PWM | $\frac{U_{\text{high}}}{2}$ | $\frac{U_{\text{high}}}{2}$ | Full duty |
| [29] | 96.4% | 96.7% | $\frac{2+D_{\text{boost}}}{1-D_{\text{boost}}}$ | $\frac{D_{\text{buck}}}{3-D_{\text{buck}}}$ | L:3; C:5 SW:5 | 40-120V/400V 1kW/Si 50kHz/PWM | $U_{\text{high}}$ | $\frac{2(U_{\text{high}}+U_{\text{low}})}{3}$ | Full duty |
| [30] | 95.8% | 95.9% | $\frac{3}{1-D_{\text{boost}}}$ | $\frac{D_{\text{buck}}}{3}$ | L:3; C:6 SW:8 | 30-100V/400V 800W/Si 20kHz/PWM | $U_{\text{high}}$ | $\frac{U_{\text{high}}}{3}$ | —— |
| [31] | 96.5% | 96.5% | $\frac{N+2}{N(1-D_{\text{boost}})}$ | —— | L:2; CL:1; C:4 SW:6 | 40-60V/400V 1kW/Si 50kHz/PWM | $\frac{NU_{\text{high}}}{N+2}$ | $\frac{2U_{\text{high}}}{N+2}$ | Full duty |
| [32] | 96.1% | 96.6% | $\frac{2N+2}{1-D_{\text{boost}}}$ | $\frac{D_{\text{buck}}}{2N+2}$ | CL:3; C:6 SW:6 | 48V/380V 250W/Si 50kHz/PWM | $U_{\text{high}}$ | —— | Full duty |
| [33] | 96% | 96% | $\frac{2N+2}{1-D_{\text{boost}}}$ | $\frac{D_{\text{buck}}}{2N+2}$ | CL:2; C:6 SW:8 | 30-40V/400V 1kW/Si 50kHz/PWM | $U_{\text{high}}$ | $\frac{NU_{\text{high}}}{N+1}$ | Full duty |
| [34] | 95.7% | 95.4% | $\frac{4N}{4D_{\text{boost}}+1}+2$ | —— | BT:2; L:2; C:3 SW:8 | 40-60V/400V 1kW/Si 50kHz/PWM | —— | —— | Full duty |
| [35] | 96.8% | 96.8% | $\frac{N+2}{N(1-D_{\text{boost}})}$ | —— | L:2; CL:1; C:6 SW:8; D:2 | 40-60V/400V 1kW/Si 50kHz/PWM | $U_{\text{high}}$ | $\frac{U_{\text{high}}}{N+2}$ | Full duty |
| [36] | 97.5% | 97.5% | $\frac{2}{1-D_{\text{boost}}}$ | $\frac{D_{\text{buck}}}{2}$ | L:2; C:3 SW:4 | 60V/200-380V 500W/SiC 50kHz/PWM | $U_{\text{high}}$ | $U_{\text{high}}$ | Full duty |
| Prop. | 97.6% | 98.3% | $\frac{3+D_{\text{boost}}}{1-D_{\text{boost}}}$ | $\frac{D_{\text{buck}}}{4-D_{\text{buck}}}$ | L:4; C:5 SW:8 | 72V/400-800V 1kW/SiC 50kHz/PWM | $\frac{U_{\text{high}}+U_{\text{low}}}{2}$ | $\frac{U_{\text{high}}+U_{\text{low}}}{2}$ | Full duty |

$N$: turns ratio; L: inductor; CL: coupled inductor; C: capacitor; BT: built-in transformer; SW: power switch; D: diode; —— : not reported

of stead-state analysis and design guideline of the circuit parameters. The essential performance of the proposed BDC have been investigated by experiments including the enhanced voltage ratio, high efficiency as well as the current balances in the dc inductors.

The wide buck/boost voltage ratios and full-range inherent current balancing properties can be attained by the proposed circuit topology and duty cycle control scheme. The asymmetrical DLC strategy has been demonstrated for an EV-DCMGs system with a wide range high-side voltage. A prototype with SiC-MOSFETs has been developed with a specification of $1\,\text{kW}$–$50\,\text{kHz}$ to reveal the actual performance of F4P-ICPBDC, whereby a wide voltage ratio range between the variable high-side voltage ($400$-$800\,\text{V}$) and the constant low-side voltage ($72\,\text{V}$) have been actually verified. The prototype can achieve maximum efficiencies above $98.3\,\%$. By comparing to the existing BDCs, the higher efficiency and higher voltage ratio can attain due to the SiC-MOSET based the F4P-ICPBDC topology.

Future research will include implementing soft switching for all main switches and adopting integrated inductors. Then, enhancing the operating frequency and increasing power density will be pursued for a wide variety of BDC applications.

## APPENDIX

The average models of the converter are derived by utilizing the state-space averaging method in order to facilitate the steady-state performance of the proposed BDC. In the buck mode, $C_{\text{H1}}$, $C_{\text{H2}}$, and $C_{\text{L}}$ are connected in series while in parallel with the high-voltage side dc source. Therefore, an equivalent series resistance (e.g., $r = 0.2\ \Omega$) for the dc source is considered to prevent invalid state variables. Referring to Fig. 5 (a) and Fig. 6, the state equations corresponding to each mode can be obtained when $D^{\text{c}} < 0.5$. By combining these state equations, the average model can be described in a matrix form as expressed by (44). Similarly, referring to Fig. 5 (b) and Fig. 6, the state equations corresponding to each mode can be obtained when $D^{\text{c}} \geq 0.5$. By combining these state equations, the average model can be derived in a matrix form as expressed by (45).

$$\frac{d}{dt}\begin{bmatrix} i_{L_{1A}}(t) \\ i_{L_{1B}}(t) \\ i_{L_{2A}}(t) \\ i_{L_{2B}}(t) \\ u_{C_{1B}}(t) \\ u_{C_{2B}}(t) \\ u_{C_{H1}}(t) \\ u_{C_{H2}}(t) \\ u_{C_L}(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{D^c}{L_{1A}} & 0 & \frac{D^c}{L_{1A}} & 0 & \frac{-1}{L_{1A}} \\ 0 & 0 & 0 & 0 & \frac{D^c}{L_{1B}} & 0 & 0 & 0 & \frac{-1}{L_{1B}} \\ 0 & 0 & 0 & 0 & 0 & \frac{-D^c}{L_{2A}} & 0 & \frac{D^c}{L_{2A}} & \frac{-1}{L_{2A}} \\ 0 & 0 & 0 & 0 & 0 & \frac{D^c}{L_{2B}} & 0 & 0 & \frac{-1}{L_{2B}} \\ \frac{D^c}{C_{1B}} & \frac{-D^c}{C_{1B}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{D^c}{C_{2B}} & \frac{-D^c}{C_{2B}} & 0 & 0 & 0 & 0 & 0 \\ \frac{-D^c}{C_{H1}} & 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_{H1}r} & \frac{-1}{C_{H1}r} & \frac{1}{C_{H1}r} \\ 0 & 0 & \frac{-D^c}{C_{H2}} & 0 & 0 & 0 & \frac{-1}{C_{H2}r} & \frac{-1}{C_{H2}r} & \frac{1}{C_{H2}r} \\ \frac{1}{C_L} & \frac{1}{C_L} & \frac{1}{C_L} & \frac{1}{C_L} & 0 & 0 & \frac{-1}{C_Lr} & \frac{-1}{C_Lr} & \frac{1}{C_Lr} - \frac{1}{R_LC_L} \end{bmatrix} \begin{bmatrix} i_{L_{1A}}(t) \\ i_{L_{1B}}(t) \\ i_{L_{2A}}(t) \\ i_{L_{2B}}(t) \\ u_{C_{1B}}(t) \\ u_{C_{2B}}(t) \\ u_{C_{H1}}(t) \\ u_{C_{H2}}(t) \\ u_{C_L}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ \frac{1}{C_{H1}r} \\ \frac{1}{C_{H2}r} \\ \frac{1}{C_Lr} \end{bmatrix} u_H(t) \quad (44)$$

$$\frac{d}{dt}\begin{bmatrix} i_{L_{1A}}(t) \\ i_{L_{1B}}(t) \\ i_{L_{2A}}(t) \\ i_{L_{2B}}(t) \\ u_{C_{1B}}(t) \\ u_{C_{2B}}(t) \\ u_{C_{H1}}(t) \\ u_{C_{H2}}(t) \\ u_{C_L}(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{-1}{2L_{1A}} & 0 & \frac{1}{2L_{1A}} & 0 & \frac{-1}{L_{1A}} \\ 0 & 0 & 0 & 0 & \frac{1}{2L_{1B}} & 0 & \frac{2D^c-1}{2L_{1B}} & 0 & \frac{-1}{L_{1B}} \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{2L_{2A}} & 0 & \frac{1}{2L_{2A}} & \frac{-1}{L_{2A}} \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{2L_{2B}} & 0 & \frac{2D^c-1}{2L_{2B}} & \frac{-1}{L_{2B}} \\ \frac{1}{2C_{1B}} & \frac{-1}{2C_{1B}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{2C_{2B}} & \frac{-1}{2C_{2B}} & 0 & 0 & 0 & 0 & 0 \\ \frac{-1}{2C_{H1}} & \frac{2D^c-1}{2C_{H1}} & 0 & 0 & 0 & 0 & \frac{-1}{C_{H1}r} & \frac{-1}{C_{H1}r} & \frac{1}{C_{H1}r} \\ 0 & 0 & \frac{-1}{2C_{H2}} & \frac{-2D^c-1}{2C_{H2}} & 0 & 0 & \frac{-1}{C_{H2}r} & \frac{-1}{C_{H2}r} & \frac{1}{C_{H2}r} \\ \frac{1}{C_L} & \frac{1}{C_L} & \frac{1}{C_L} & \frac{1}{C_L} & 0 & 0 & \frac{-1}{C_Lr} & \frac{-1}{C_Lr} & \frac{R_L-r}{C_LR_LC_Lr} \end{bmatrix} \begin{bmatrix} i_{L_{1A}}(t) \\ i_{L_{1B}}(t) \\ i_{L_{2A}}(t) \\ i_{L_{2B}}(t) \\ u_{C_{1B}}(t) \\ u_{C_{2B}}(t) \\ u_{C_{H1}}(t) \\ u_{C_{H2}}(t) \\ u_{C_L}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ \frac{1}{C_{H1}r} \\ \frac{1}{C_{H2}r} \\ \frac{1}{C_Lr} \end{bmatrix} u_H(t) \quad (45)$$

---

$$\begin{cases} \frac{d}{dt}\begin{bmatrix} i_{L_{1A}}(t) \\ i_{L_{1B}}(t) \\ i_{L_{2A}}(t) \\ i_{L_{2B}}(t) \\ u_{C_{1B}}(t) \\ u_{C_{2B}}(t) \\ u_{C_{H1}}(t) \\ u_{C_{H2}}(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{1}{2L_{1A}} & 0 & \frac{-1}{2L_{1A}} & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{2L_{1B}} & 0 & \frac{2D^d-1}{2L_{1B}} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{2L_{2A}} & 0 & \frac{-1}{2L_{2A}} \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{2L_{2B}} & 0 & \frac{2D^d-1}{2L_{2B}} \\ \frac{-1}{2C_{1B}} & \frac{1}{2C_{1B}} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{2C_{2B}} & \frac{1}{2C_{1B}} & 0 & 0 & 0 & 0 \\ \frac{1}{2C_{H1}} & \frac{1-2D^d}{2C_{H1}} & 0 & 0 & 0 & 0 & \frac{-1}{C_{H1}R_H} & \frac{-1}{C_{H1}R_H} \\ 0 & 0 & \frac{1}{2C_{H2}} & \frac{1-2D^d}{2C_{H2}} & 0 & 0 & \frac{-1}{C_{H2}R_H} & \frac{-1}{C_{H2}R_H} \end{bmatrix} \begin{bmatrix} i_{L_{1A}}(t) \\ i_{L_{1B}}(t) \\ i_{L_{2A}}(t) \\ i_{L_{2B}}(t) \\ u_{C_{1B}}(t) \\ u_{C_{2B}}(t) \\ u_{C_{H1}}(t) \\ u_{C_{H2}}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{1A}} \\ \frac{1}{L_{1B}} \\ \frac{1}{L_{2A}} \\ \frac{1}{L_{2B}} \\ 0 \\ 0 \\ 0 \\ \frac{1}{C_{H1}R_H} \\ \frac{1}{C_{H2}R_H} \end{bmatrix} u_L(t) \\ u_H = u_{C_{H1}} + u_{C_{H2}} - u_L \end{cases} \quad (46)$$

$$\begin{cases} \frac{d}{dt}\begin{bmatrix} i_{L_{1A}}(t) \\ i_{L_{1B}}(t) \\ i_{L_{2A}}(t) \\ i_{L_{2B}}(t) \\ u_{C_{1B}}(t) \\ u_{C_{2B}}(t) \\ u_{C_{H1}}(t) \\ u_{C_{H2}}(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{1-D^d}{L_{1A}} & 0 & \frac{D^d-1}{L_{1A}} & 0 \\ 0 & 0 & 0 & 0 & \frac{D^d-1}{L_{1B}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1-D^d}{L_{2A}} & 0 & \frac{D^d-1}{L_{2A}} \\ 0 & 0 & 0 & 0 & 0 & \frac{D^d-1}{L_{2B}} & 0 & 0 \\ \frac{D^d-1}{C_{1B}} & \frac{1-D^d}{C_{1B}} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{D^d-1}{C_{2B}} & \frac{1-D^d}{C_{1B}} & 0 & 0 & 0 & 0 \\ \frac{1-D^d}{C_{H1}} & 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_{H1}R_H} & \frac{-1}{C_{H1}R_H} \\ 0 & 0 & \frac{1-D^d}{C_{H2}} & 0 & 0 & 0 & \frac{-1}{C_{H2}R_H} & \frac{-1}{C_{H2}R_H} \end{bmatrix} \begin{bmatrix} i_{L_{1A}}(t) \\ i_{L_{1B}}(t) \\ i_{L_{2A}}(t) \\ i_{L_{2B}}(t) \\ u_{C_{1B}}(t) \\ u_{C_{2B}}(t) \\ u_{C_{H1}}(t) \\ u_{C_{H2}}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{1A}} \\ \frac{1}{L_{1B}} \\ \frac{1}{L_{2A}} \\ \frac{1}{L_{2B}} \\ 0 \\ 0 \\ 0 \\ \frac{1}{C_{H1}R_H} \\ \frac{1}{C_{H2}R_H} \end{bmatrix} u_L(t) \\ u_H = u_{C_{H1}} + u_{C_{H2}} - u_L \end{cases} \quad (47)$$

In the boost mode, the state equations corresponding to each mode can be derived when $D^{\mathrm{d}} \leq 0.5$ by referring to Fig. 8(a) and Fig. 9. By utilizing these state equations, the average model can be derived in matrix form as written by (46). Similarly, referring to Fig. 8(b) and Fig. 9, the state equations corresponding to each mode can be obtained when $D^{\mathrm{d}} > 0.5$. Then, based on these state equations, the average model can be derived in a matrix form as denoted by (47).

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**Shiqiang Liu** (S'23) was born in Henan, China in 1995. He received the B.S. degree in electrical engineering and automation from Shandong University of Technology, Zibo, China, in 2017, and the M.S. degree in electrical engineering from Dalian University of Technology, Dalian, China, in 2020. He is currently working toward the Ph.D degree in electrical engineering with the Faculty of Maritime Sciences, Kobe University, Kobe City, Japan. His research interests include bidirectional dc-dc converters, HEV/EV onboard chargers, Induction Heating (IH) systems, EV-connected dc-microgrids (EV-DCMGs) systems, and artificial intelligence applications in power electronics.

**Guiyi Dong** (S'22) received his B.S. degree from the School of Information and Electrical Engineering, Shandong Jianzhu University, Shandong, China. He obtained his M.S. degree from Gunma University, Gunma, Japan. He is currently working towards his Ph.D. degree at the Graduate School of Maritime Sciences, Kobe University, Kobe City, Hyogo, Japan. His research interests include resonant converters, high frequency inverters, bidirectional dc-dc converters, and bidirectional Wireless Power Transfer (WPT) device for vehicle-to-house (V2H) systems. His current research is focused on the development of high-frequency inverters for WPT and Induction Heating (IH) systems, with a particular emphasis on the application of direct AC-AC converters.

**Tomokazu Mishima** (S'00–M'04–SM'15) received the Ph.D. degree in electrical engineering from The University of Tokushima, Japan in 2004. Since 2010, he has been with Kobe University, Hyogo, Japan as an associate professor, and engages in the researches and developments of power electronics circuits and systems. Dr. Mishima has been appointed to the Center for Advanced Medical Engineering Research and Development (CAMED) in 2020, and the research center for Hydrogen Energy Technology (HyTec) in 2024, both of which are institutional organizations in Kobe University. His research interests include soft-switching dc–dc converters, resonant converters, and high frequency inverters for industrial, automotive, biomedical, renewable and sustainable energy applications.

Dr. Mishima is the recipients of 2022 IEEE Transactions on Power Electronics Second Place Prize Paper Award, Japan Nikkei Electronics Power Electronics Award in 2021, the best paper award in the 2009 IEEE International Conference on Power Electronics and Drive Systems (PEDS), and the best paper presentation award in 2012 Annual Conference of the IEEE Industrial Electronics Society (IECON). He serves as the associate editor of IEEE Transactions on Power Electronics since 2018, and the chairperson of the semiconductor power converter sector in IEEJ (The Institute of Electrical Engineering of Japan) Transactions on Industry Applications in 2023. He was also the chairperson of the IEEJ Investing Research & Development Committee on High-Frequency Switching Power Converters and Applied Power Supplies in 2019–2023.

Dr. Mishima is a senior member of IEEJ, and members of IEICE (The Institute of Electronics, Information and Communication Engineers) and JIPE (the Japan Institute of Power Electronics).

**Ching-Ming Lai** (S'06–M'10–SM'17) received the Ph.D. degree in electrical engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2010. From 2009 to 2012, he was a Senior Research and Development Engineer with Lite-On Technology Corporation, Taiwan. From 2014 to 2019, he was a Faculty Member with the Department of Vehicle Engineering, National Taipei University of Technology. Since 2019, he has joined the Department of Electrical Engineering at National Chung Hsing University (NCHU), Taiwan. He is currently the professor and the director of the Intelligent Electric Vehicle & Green Energy Center at NCHU. From February to August 2023, he was a Research Professor at Kobe University, Kobe, Japan. His research interests include electric vehicles (EVs), power electronics, green energy technologies, and intelligent transportation.

Dr. Lai received 2008 Young Author's Award for Practical Application from the Society of Instrument and Control Engineers (SICE), Japan, and the Best Paper Award at the 2013 IEEE International Conference on Power Electronics and Drive Systems (PEDS). He was a recipient of several distinguished awards, including the Dr. Shechtman Youth Researcher Award from Taipei Tech (2018), the Outstanding Youth Electrical Engineer Award from the Chinese Institute of Electrical Engineering (2018), the Outstanding Education Achievement Award from SAE-Taipei (2019), the Outstanding Youth Control Engineer Award from the Chinese Automatic Control Society (2019), the Outstanding Youth Engineer Award from the Chinese Institute of Engineers-Taichung Chapter (2020), the NCHU Outstanding Industry-Academia Collaboration Award (2021 2023). In 2023, he received the Ta-You Wu Memorial Award from National Science and Technology, Taiwan. In addition, according to Elsevier, he was listed in the World's Top 2 of Scientists (Field: Energy) by field in 2021, 2022, and 2023.

Dr. Lai was the Co-Chair of IEEE IFEEC-2021, the Tutorial Chair of IEEE IFEEC-2021, IEEE WiPDA-2019, and IEEE IFEEC-2015. He has been serving as an Editor for the IEEE TRANSACTIONS ON VEHICULAR TECHNOLOGY, since 2017, and an Associate Editor for IEEE ACCESS, since 2021.

Dr. Lai is Fellow of IET and Fellow of the Australian Institute of Energy.