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Asymmetrical Duty-Cycle Limit Control-Based Multi-Port Bidirectional DC–DC Converter for Distributed Energy Storage System Applications

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***Abstract*—This paper presents a novel multi-port bidirectional DC–DC converter (MP-BDC) by featuring a two-phase interleaved architecture at each low-voltage port to mitigate current ripple across the low-voltage side capacitors and inductors. The multi-port configuration is designed to enable the simultaneous utilization of energy storage systems (ESSs) with different voltage levels, while also achieving a wide voltage conversion ratio. In order to ensure the balanced average inductor current across the entire duty cycle range, a cost-effective asymmetric duty-cycle limit control (A-DLC) strategy is implemented, which demonstrates the robust performance against variations in the DC inductors. Moreover, the proposed converter is well-suited for integrating various renewable energy resources and hybrid energy storage systems. In addition, the low-voltage ports are configured to share a common ground with the high-voltage port, which helps reduce electromagnetic interference within the system. The operating principles, device stresses, current ripple characteristics, and design procedures in the proposed MP-BDC are comprehensively analyzed. The essential performances are demonstrated by a 2.5 kW–50 kHz prototype with dual low-voltage dc ports (72 V and 48 V) and a single high-voltage dc port (400–800 V) utilizing silicon carbide metal-oxide-field-effect-transistors (SiC-MOSFETs); The maximum efficiencies are measured as 98.04 % with a high-voltage port of 400 V and 98.46 % with a high-voltage port of 800 V, respectively. These results demonstrate the effectiveness of the proposed MP-BDC and highlight its potential for high-power applications, such as EV fast charging and renewable energy integration.**

***Index Terms*—Asymmetrical duty-cycle limit control (A-DLC), energy storage system (ESS), high voltage ratio, interleaved architecture, multi-port bidirectional DC–DC converter (MP-BDC), synchronous rectification (SR).**

I. Introduction

DEVELOPMENT of renewable energy generation has been accelerated in recent years as part of global efforts to mitigate the greenhouse effect and address energy shortages. In general, renewable energy sources are significantly influenced by natural environmental factors, leading to instability in power supply within microgrid systems. To stabilize the fluctuating power output from renewable energy generation systems, DC microgrids equipped with various energy storage systems (ESSs) such as batteries and supercapacitors, have emerged as a popular architecture for power generation [1]. In parallel, the potential use of electric vehicle (EV) batteries as mobile backup clean energy sources has garnered considerable attention [2], [3]. This approach enables the vehicle-to-grid (V2G) function, allowing power to be fed back to the DC microgrid or AC utility grid, which is particularly valuable during peak power demand periods. Additionally, EVs can act as a power source for vehicle-to-everything (V2X) applications in cases of grid interruptions [4]–[6].

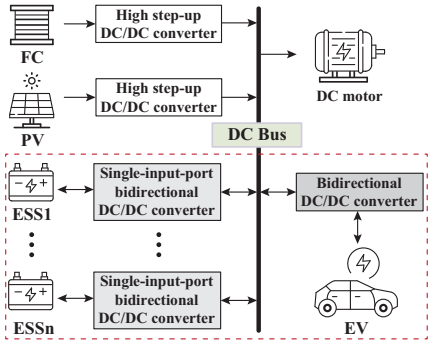

Fig. 1. Traditional single-input single-output (SISO) architecture with various energy storage systems in the DC microgrid.

Fig. 1 illustrates the widely adopted architecture of an EV-connected DC microgrid. In this configuration, the typical DC bus voltage is 400 V, while EV battery voltages generally range from 400 V to 800 V [7]. In contrast, the rated voltages of ESSs are typically in the range of tens of volts. Consequently, the bidirectional DC–DC converter (BDC) in this system is required to achieve a voltage gain of 10 to 20 times in both boost and buck modes. Meanwhile, fast charging capabilities have become a critical focus of research and development in order to address key requirements for EV advancement, including high power, high-power density, high reliability, and compatibility with next-generation high-voltage platforms [8]–[12]. However, BDCs are typically configured as single-input single-output (SISO) structures in the typical DC microgrids as depicted in Fig. 1. This necessitates the use of multiple converters to connect various ESSs to the DC bus, which increases the number of power devices and results in larger system size and higher costs. In order to overcome these challenges and enable a low-loss, compact converter design, this paper introduces a novel multi-port circuit architecture,

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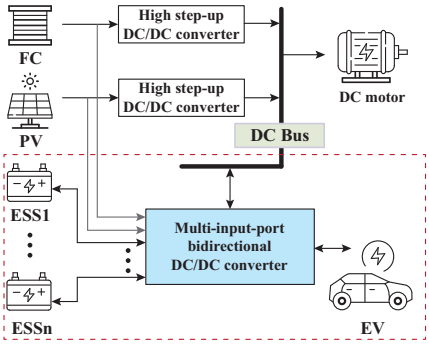


Fig. 2. Proposed multi-input single-output (MISO) architecture with various energy storage systems in the DC microgrid.

as shown in Fig. 2. This architecture allows multiple ESSs to be directly integrated into the DC microgrid system alongside EV connection through a single BDC. As a result, the number of converters required between the ESSs and the DC bus is reduced, and the additional converter between the DC bus and the EV can be eliminated. Moreover, photovoltaic (PV) and fuel cell (FC) systems can serve as low-voltage ESSs for the unidirectional boost operation of the converter, enabling full utilization of hybrid energy sources within the system. In this context, the development of multi-port BDCs with wide voltage conversion ratios and fast-charging potential is essential for DC microgrids. These converters are critical for achieving seamless power flow control between ESSs and EV batteries, facilitating both charging and discharging operations [13], [14].

The multi-port BDCs are generally categorized into two types: isolated and non-isolated [15], [16]. Isolated BDCs achieve substantial voltage conversion ratios by adjusting the windings turns ratio of a high-frequency transformer, the duty cycles, or the phase shift angles of switches. However, isolated multi-port BDCs based on architectures such as interleaved buck-boost [17]–[19], full-bridge, or dual-active-bridge [20]–[22] typically involve more than eight power switches, which potentially leads to increases in the system complexity and high cost. In order to address this, configurations using half-bridge circuits and voltage multipliers have been proposed as more efficient alternatives, offering reduced switch counts [23]. Nonetheless, the leakage inductance of the high-frequency transformer in isolated multi-port BDCs can cause significant voltage spikes across power devices, necessitating the use of soft-switching techniques, snubber circuits, or clamp circuits to recover the magnetic energy due to the leakage magnetic fluxes [24]. These methods, while effective, require complex control strategies or additional auxiliary components, further complicating control and potentially impacting overall efficiency.

In contrast, non-isolated BDCs feature compact structures with fewer components and are commonly proposed for renewable energy systems and EVs [25]–[27]. Traditional topologies, such as boost, buck-boost, Cuk, and SEPIC converters [28]–[32], are efficient and cost-effective for low-voltage applications. However, all of them suffer from limited voltage ratio and high voltage stress, making them unsuitable for EV-connected DC microgrids. In order to achieve higher voltage ratios, topologies based on voltage multiplier, multilevel, coupled inductors, and switched capacitors offer effective solutions. Voltage multiplier and multilevel converters can achieve high voltage ratios and reduce voltage stress on power devices, but they typically require additional components and complex control strategies, which may increase system size as well as cost [33]–[35]. Coupled inductor converters can achieve high voltage ratios through turns ratio adjustments but face challenges such as leakage inductance and parasitic oscillations [36], [37]. Multi-port converters with full soft-switching have been proposed in [38]–[40], utilizing snubber and active clamp circuits to mitigate the technical drawbacks as mentioned above. However, these approaches introduce additional components, increasing system complexity. Furthermore, the single coupled inductor design in [40] exhibited lower voltage gain and limited output power. Soft switching, as demonstrated in [41] and [42], can be achieved by leveraging the inherent synchronous rectification (SR) characteristics of the proposed topologies. However, adapting these designs for multiport operation remains a significant challenge. In contrast, switched capacitor converters, known for their simplicity and scalability, achieve high voltage ratios by transferring energy through distinct capacitor charging and discharging paths. These features make them a promising alternative for high-voltage applications [43]. A design combining PWM and phase-shift-switched capacitor operation, introduced in [44], reduces the switch count with a simplified structure. However, it is limited by a low voltage gain ratio (less than 5), restricting its applicability. In order to overcome this, a multi-port converter integrating a modified Z-source converter with a switched capacitor network is presented in [45], offering multiple operational modes. However, it is constrained by a narrow duty-cycle range (below 0.5) and imbalanced average inductor currents. In [46], a converter is developed to reduce normalized peak voltage stress across semiconductor devices, which improves reliability. However, this comes at the cost of increased numbers of semiconductor power devices and passive components, along with duty cycle limitations, which pose challenges from a practical implementation perspective. Multi-port converters proposed in [47]–[49] achieve higher voltage conversion ratios, however suffer from low output power and efficiency, limiting their potential in high-power EV fast-charging systems. An alternative topology in [50] incorporates three basic boost cells, enabling flexible operation across input ports. Nevertheless, its reliance on equal duty-cycle control hinders the ability to balance inductor currents across the whole range of duty cycle and necessitates large inductors, posing challenges for miniaturization and high-density integration.

To address the limitations of existing switched capacitor-based BDCs, this article proposes a novel multi-port bidirectional DC–DC converter (MP-BDC) integrated with an asymmetrical duty-cycle limit control (A-DLC) scheme. The key features in the proposed MP-BDC are summarized as:

1) The proposed interleaved BDC achieves an enhanced voltage conversion ratio, higher power output, and improved efficiency.

2) The A-DLC ensures natural self-balancing of inductor currents across the whole range of duty cycle in both buck and boost modes.
3) The low-voltage ports are designed to share a common ground with the high-voltage port, effectively reducing electromagnetic interference (EMI) within the system.
4) The proposed control method enables efficient power distribution and sharing among the low-voltage dc ports.
5) The proposed MP-BDC demonstrates strong potential for high-power fast charging of EVs and other multi-port applications within DC microgrids.

The remainder of this article is organized as follows: Section II elaborates on the topology derivations, control strategy, and operating mode transitions of the proposed multi-port bidirectional DC–DC converter. Section III focuses on analyzing the steady-state characteristics of the proposed MP-BDC based on its operating principles. The design guidelines for the key parameters of the proposed BDC are detailed in Section IV. In Section V, experimental results from a 2.5 kW-50 kHz scaled-down prototype using SiC-MOSFETs are presented, showcasing the converter's key performance metrics. Finally, Section VI summarizes the findings, evaluates the practical effectiveness of the proposed circuit topology and A-DLC control scheme, and highlights its potential for high-power fast charging and other high-power applications.

II. Proposed Topology and Control Strategy with A-DLC

A. Derivations of Circuit Topology

The derivation process of the proposed MP-BDC is demonstrated in Fig. 3. Fig. 3(a) presents the basic two-phase buck/boost converter with a switched capacitor, where V_{Low} and V_{High} represent the low-side and high-side voltages, respectively [51]. In this configuration, the gate signals of $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$ are interleaved clocking by 180° with an identical duty cycle, while $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$ operate complementary to $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$, respectively. This arrangement enables the voltage conversion ratio (VCR) to be doubled in a boost mode or halved in a buck mode compared to the conventional buck/boost converter. Although the interleaved structure effectively reduces the low-side current ripple, the converter shown in Fig. 3(a) still suffers from significant limitations: It is restricted to SISO operation, and the achievable VCR remains relatively low. These constraints hinder the full utilization of different ESSs in the DC microgrid. Moreover, with existing control methods, inductor current balance can only be achieved within a limited duty cycle range: less than 0.5 in a buck mode and greater than 0.5 in a boost mode. In order to overcome these limitations, a multi-port BDC can be synthesized based on the basic-level module through various configurations of input and output port connections [32], as illustrated in Fig. 3(b). The input and output ports can be arranged either in series or parallel with appropriate module configurations. The parallel connection, as shown in Fig. 3(b1) and Fig. 3(b3), offers the advantage of common grounding for the ports. On the other hand, the series connection, as illustrated in Fig. 3(b2) and Fig. 3(b4), enables the voltage of the ports

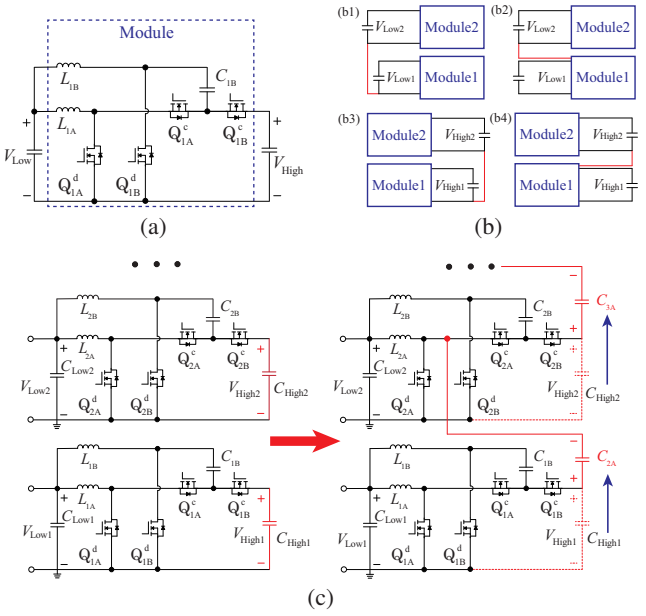


Fig. 3. Topology derivation of the proposed MP-BDC: (a) two phase buck/boost converter with a switched capacitor, (b) extensible connection types of multi-port converters [32], and (c) proposed scalable MP-BDC.

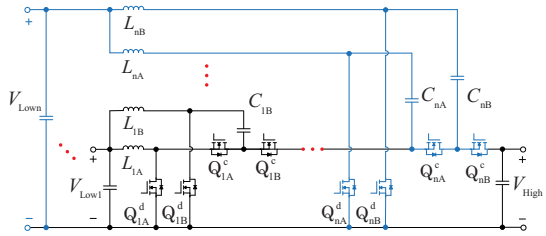


Fig. 4. Proposed MP-BDC topology with A-DLC.

to be stepped up. As depicted in Fig. 2, a configuration with multiple low-voltage ports and a single high-voltage port is critical. In order to leverage the advantages of both parallel and series connections, this study introduces a multi-port converter featuring parallel-connected low-voltage ports and series-connected high-voltage ports, as derived from the basic-level module shown in Fig. 3(a). The topology evolution of the proposed converter is shown in Fig. 3(c). In this design, the series connection on the high-voltage side is achieved by using the high-voltage capacitor of the preceding module as the switched capacitor for the subsequent module (e.g., $C_{\mathrm{High1}} \rightarrow C_{2\mathrm{A}}$, $C_{\mathrm{High2}} \rightarrow C_{3\mathrm{A}}$, ...). Furthermore, to address the inductor current balance issue for each low-voltage port, an innovative asymmetric duty-cycle limit control strategy is implemented. In summary, the proposed topology and duty cycle control scheme allow the converter to achieve multi-port operation, a high voltage conversion ratio, and full-range inherent inductor current balancing simultaneously.

B. Composition of the Proposed Topology

The proposed MP-BDC, featuring n low-voltage dc ports along with a single high-voltage dc port, is illustrated in Fig. 4. The converter consists of the following components:

- n sets of power semiconductor switches: ($\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$, $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}$, $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$, $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$) up to ($\mathrm{Q}^{\mathrm{c}}_{\mathrm{nA}}$, $\mathrm{Q}^{\mathrm{d}}_{\mathrm{nA}}$, $\mathrm{Q}^{\mathrm{c}}_{\mathrm{nB}}$, $\mathrm{Q}^{\mathrm{d}}_{\mathrm{nB}}$).

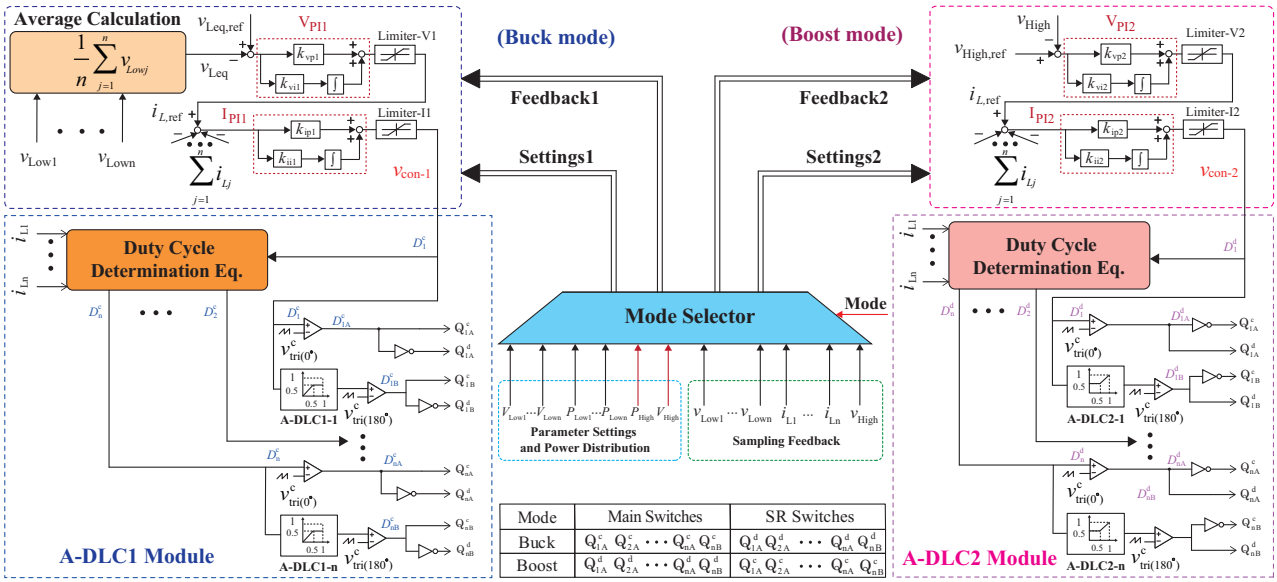


Fig. 5. Schematic diagram of controller based on A-DLC strategy.

- $2\mathrm{n}-1$ switched capacitors, including $C_{1\mathrm{B}}$, ($C_{2\mathrm{A}}$, $C_{2\mathrm{B}}$) up to (C_{nA}, C_{nB}).
- n groups of power inductors, ranging from ($L_{1\mathrm{A}}$, $L_{1\mathrm{B}}$) to (L_{nA}, L_{nB}).
- n low-voltage side filter capacitors: C_{Low1} through C_{Lown}.
- 1 high-voltage side filter capacitor: C_{High}.

C. Asymmetric Duty-cycle Limit Control Strategy

The closed-loop control strategy employing the A-DLC scheme is illustrated in Fig. 5. It features dual closed loops: an external loop for output voltage regulation and an internal loop for inductor current regulation. In a boost mode, the error between the sampled high-side output voltage and its reference is processed by the external $\mathrm{V_{PI2}}$ controller to generate the reference current $i_{\mathrm{L,ref}}$, after passing through the $\mathrm{Limiter-V2}$ block. In the subsequent stage, the total current from the two-phase inductors in each low-voltage unit is then summed and compared with $i_{\mathrm{L,ref}}$. The resulting control signal $v_{\mathrm{con-2}}$, which corresponds to D_1^{d}, is generated through the internal $\mathrm{I_{PI2}}$ controller and $\mathrm{Limiter-I2}$, and is constrained within the range of 0 to 1. The preliminary duty cycle D_1^{d} for the first module is determined based on input/output voltages and power distribution. Using the duty cycle equation (which has a similar form to (10) for dual low-voltage ports), the relationship between duty cycles and current distribution is derived, leading to D_2^{d} to $D_{\mathrm{n}}^{\mathrm{d}}$. Then, the control signal $D_{\mathrm{k}}^{\mathrm{d}}$, (where k ranges from 1 to n), is compared with a unit triangle carrier to generate the duty cycle signals $D_{\mathrm{kA}}^{\mathrm{d}}$, which directly determines the duty cycles of the active switches $D_{\mathrm{kA}}^{\mathrm{c}}$ and $D_{\mathrm{kA}}^{\mathrm{d}}$. In contrast, the signal $D_{\mathrm{kB}}^{\mathrm{d}}$, derived via the $\mathrm{A-DLC2-k}$ stage, sets the cycles for $\mathrm{Q_{kB}^c}$ and $\mathrm{Q_{kB}^d}$. Additionally, all $\mathrm{Q_{kA}^d}$ switches operate without phase shift, while $\mathrm{Q_{kB}^d}$ switches have a 180° phase difference. Their counterparts, $\mathrm{Q_{kA}^c}$ and $\mathrm{Q_{kB}^c}$, receive complementary gate signals corresponding to $\mathrm{Q_{kA}^d}$ and $\mathrm{Q_{kB}^d}$, operating in the SR state.

In the similar way, the sampled voltages from low-voltage ports are averaged in the buck mode to obtain the equivalent low-voltage input $\mathrm{V_{Leq}}$, which is defined in (29). The deviation between $\mathrm{V_{Leq}}$ and its reference value $\mathrm{V_{Leq,ref}}$ is processed by the $\mathrm{V_{PI1}}$ controller to generate $i_{\mathrm{L,ref}}$ after passing through $\mathrm{Limiter-V1}$ block. In the next step, the total current of the two-phase inductors in each low-voltage module is summed and compared with $i_{\mathrm{L,ref}}$. The control signal $v_{\mathrm{con-1}}$, which corresponds to D_1^{c}, is subsequently generated by the inner $\mathrm{I_{PI1}}$ controller and $\mathrm{Limiter-I1}$, where its range is limited to a value between 0 and 1. The initial duty cycle D_1^{c} is determined on the basis of input/output voltages and power distribution. Using the duty cycle determination equation (like (19) for dual low-voltage ports), the relationship between duty cycles and the current distribution on the low-voltage sides is established, yielding D_2^{c} to $D_{\mathrm{n}}^{\mathrm{c}}$. Furthermore, the control signal $D_{\mathrm{k}}^{\mathrm{c}}$ is compared with a unit triangular waveform to generate the duty cycle signals $D_{\mathrm{kA}}^{\mathrm{c}}$, which directly define the duty cycles for $\mathrm{Q_{kA}^c}$ and $\mathrm{Q_{kA}^d}$. Meanwhile, $D_{\mathrm{kB}}^{\mathrm{c}}$, derived via $\mathrm{A-DLC1-k}$ sets the duty cycles for $\mathrm{Q_{kB}^c}$ and $\mathrm{Q_{kB}^d}$. All $\mathrm{Q_{kA}^c}$ switches operate without any phase shift, while $\mathrm{Q_{kB}^c}$ switches operate with a 180° phase shift relative to $\mathrm{Q_{kA}^c}$. In addition, their complementary counterparts $\mathrm{Q_{kA}^d}$ and $\mathrm{Q_{kB}^d}$ operate in the SR mode.

D. Mode Transitions

The proposed converter operates as a multi-input single-output (MISO) structure in the boost mode. The circuit configuration with dual low-voltage inputs and a single high-voltage output is depicted in Fig. 6. The primary switches $\mathrm{Q_{1A}^d}$ and $\mathrm{Q_{2A}^d}$ operate without any phase shift, arranged in a center-oriented manner, while the switches $\mathrm{Q_{1B}^d}$ and $\mathrm{Q_{2B}^d}$ function with a phase offset of 180°. Their corresponding switches $\mathrm{Q_{1A}^c}$, $\mathrm{Q_{1B}^c}$, $\mathrm{Q_{2A}^c}$ and $\mathrm{Q_{2B}^c}$ operate in SR mode to minimize the power losses. Moreover, the pairs of switches $\mathrm{Q_{1A}^c}$ / $\mathrm{Q_{1A}^d}$, $\mathrm{Q_{1B}^c}$ / $\mathrm{Q_{1B}^d}$, $\mathrm{Q_{2A}^c}$ / $\mathrm{Q_{2A}^d}$, and $\mathrm{Q_{2B}^c}$ / $\mathrm{Q_{2B}^d}$ are driven in a complementary fashion. Furthermore, the switched capacitors $C_{1\mathrm{B}}$,

C_{2A} and C_{2B} are employed to step up the output voltage. The duty cycles of the primary switches are expressed as

$$\begin{cases} D_{1A}^{d} = D_{1}^{d} \\ D_{1B}^{d} = \begin{cases} 0.5 \text{ when } D_{1}^{d} \le 0.5 \\ D_{1}^{d} \text{ when } D_{1}^{d} > 0.5 \end{cases} \\ D_{2A}^{d} = D_{2}^{d} \\ D_{2B}^{d} = \begin{cases} 0.5 \text{ when } D_{2}^{d} \le 0.5 \\ D_{2}^{d} \text{ when } D_{2}^{d} > 0.5. \end{cases} \end{cases} \tag{1}$$

The representative operating waveforms of the main circuit in boost mode are illustrated in Fig. 7 and Fig. 8, respectively. Referring to the typical waveforms, the circuit comprises 12 operation modes as demonstrated in Fig. 9. The detailed operating principle in (III) Zone $B2$ of Fig. 7 is explained below when A-DLC2-2 is active (Zone $B2$ is delineated in Fig. 11):

[Mode j] ($t_0 \le t < t_1$) The SR switch Q_{1A}^{c} is turned OFF at $t = t_0$, and after a brief dead time interval, the switch Q_{1A}^{d} is turned ON. Accordingly, the DC inductor current $i_{L_{1A}}$ changes to increase linearly.

[Mode i] ($t_1 \le t < t_2$) The main switch Q_{2B}^{d} is switched OFF at $t = t_1$. Then, Q_{2B}^{c} is turned ON by SR. At this moment, the magnetic energy stored in L_{2A} and L_{2B} is combined and transferred to the high voltage side V_{H}, causing the currents $i_{L_{2A}}$ and $i_{L_{2B}}$ to decrease linearly. The circuit operation reverts to Mode f at $t = t_2$.

[Mode f] ($t_2 \le t < t_3$) The SR switch Q_{1B}^{d} is turned OFF at $t = t_2$, after which Q_{1B}^{c} is turned ON. Consequently, the magnetic energy stored in the DC inductor L_{1B} subsequently begins to transfer to the high voltage side V_{High}, causing the current $i_{L_{2B}}$ to decrease linearly.

[Mode g] ($t_3 \le t < t_4$) The SR switch Q_{2A}^{c} is turned OFF at $t = t_3$, after which, the main switch Q_{2A}^{d} is turned ON. As a result, the DC inductor current $i_{L_{2A}}$ begins to increase linearly. However, the $i_{L_{1B}}$ continues to decrease due to $V_{Low1} + V_{C_{1B}} < V_{C_{2A}}$.

[Mode f] ($t_4 \le t < t_5$) The main switch Q_{2A}^{d} is turned OFF at $t = t_4$, and shortly thereafter, the switch Q_{2A}^{c} is turned ON by the SR. Consequently, the DC inductor current $i_{L_{2A}}$ changes to decrease linearly, and the energy stored in L_{1B}, L_{2A} and L_{2B} is simultaneously released to the high-voltage side.

[Mode i] ($t_5 \le t < t_6$) The SR switch Q_{1B}^{c} is turned OFF at $t = t_5$, after which the main switch Q_{1B}^{d} is turned ON. Accordingly, the DC inductor current $i_{L_{1B}}$ changes to increase linearly.

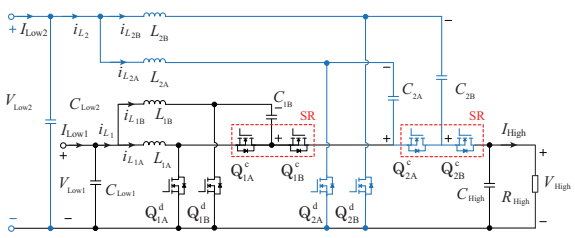


Fig. 6. Circuit configuration of MP-BDC in the boost mode.

[Mode j] ($t_6 \le t < t_7$) The SR switch Q_{2B}^{c} is turned OFF at $t = t_6$, after which the primary switch Q_{2B}^{d} is turned ON. Then, the magnetic energy is stored at L_{2B}, whereby the DC inductor current $i_{L_{2B}}$ begins to linearly increase. Additionally, L_{2A} begins to charge due to $V_{Low2} + V_{C_{2A}} > V_{C_{2B}}$.

[Mode d] ($t_7 \le t < t_8$) The main switch Q_{1A}^{d} is turned OFF at $t = t_7$, and in the short interval, the counterpart Q_{1A}^{c} is turned ON by the SR. As a result, the DC inductor current $i_{L_{1A}}$ starts to decline linearly, while $i_{L_{1B}}$, $i_{L_{2A}}$ and $i_{L_{2B}}$ continue to increase linearly.

In a similar way, the circuit configuration in the buck mode features a single-input multi-output (SIMO) structure. The circuit configuration with a single high-voltage input and dual low-voltage outputs, is depicted in Fig. 10. In this setup, the primary switches Q_{1A}^{c} and Q_{2A}^{c} operate without any phase shift, aligned in a center-oriented manner, while the switches Q_{1B}^{c} and Q_{2B}^{c} function with a phase offset of 180°. Their corresponding switches Q_{1A}^{d}, Q_{1B}^{d}, Q_{2A}^{d}, and Q_{2B}^{d} operate in SR mode to minimize power losses. Additionally, the pairs of switches Q_{1A}^{c}/Q_{1A}^{d}, Q_{1B}^{c}/Q_{1B}^{d}, Q_{2A}^{c}/Q_{2A}^{d} and Q_{2B}^{c}/Q_{2B}^{d} are driven in a complementary manner. Furthermore, the switched capacitors C_{1B}, C_{2A}, and C_{2B} are utilized to step down the output voltage. The duty cycles of the primary switches are expressed as

$$\begin{cases} D_{1A}^{c} = D_{1}^{c} \\ D_{1B}^{c} = \begin{cases} D_{1}^{c} \text{ when } D_{1}^{c} < 0.5 \\ 0.5 \text{ when } D_{1}^{c} \ge 0.5 \end{cases} \\ D_{2A}^{c} = D_{2}^{c} \\ D_{2B}^{c} = \begin{cases} D_{2}^{c} \text{ when } D_{2}^{c} < 0.5 \\ 0.5 \text{ when } D_{2}^{c} \ge 0.5. \end{cases} \end{cases} \tag{2}$$

The operating waveforms and mode transitions of the main circuit in the buck mode remains as same as those of the boost mode, while the power flow is reversed.

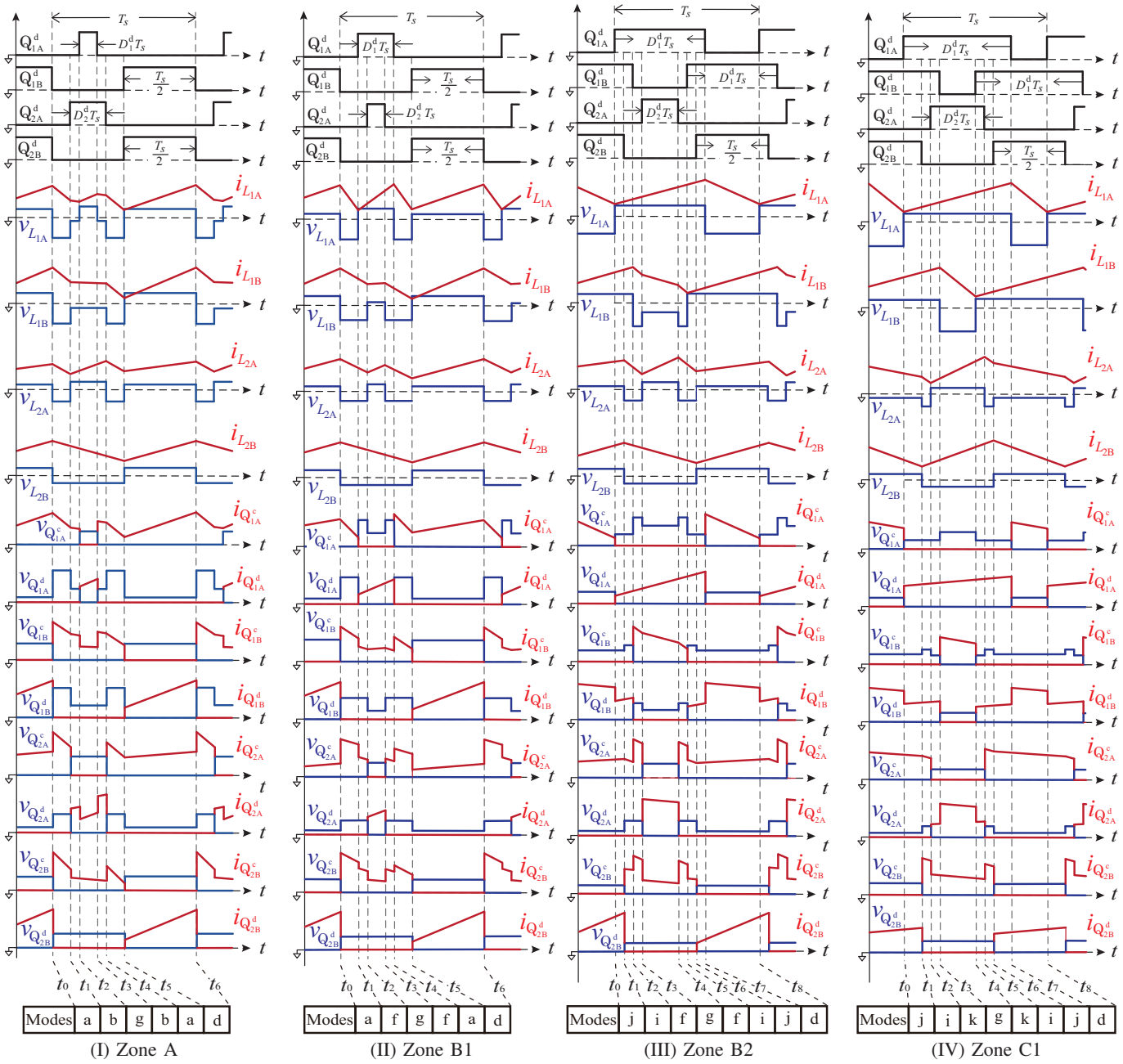
III. Steady-State Analysis

In order to simplify the analysis and design of the circuit parameters, the following operating conditions of the main circuit are assumed: i) all the active and passive components are considered ideal; ii) the DC inductor currents $i_{L_{1A}}$, $i_{L_{1B}}$, $i_{L_{2A}}$ and $i_{L_{2B}}$ are assumed to operate in continuous conduction mode (CCM); iii) the effect of load impedance is disregarded in the steady-state analysis; and iv) the voltages of capacitors are assumed to be well smoothed and constant, implying that voltage ripples are negligible due to sufficiently large capacitance.

A. Inductor Current Self-Balancing with A-DLC

1) Boost Mode: In this mode, based on the different actions of A-DLC2, the entire duty cycle range can be segmented into three main regions:A, B, and C. The ranges of zones A, B, and C in the boost mode are illustrated in Fig. 11, where l_1 through l_6 satisfy the following equations, which will be utilized in the subsequent analysis of inductor current ripples:

$$\left\{ l_1 : D_{1}^{d} = \frac{5 - \sqrt{17}}{4} \right. \tag{3a}$$



(I) Zone A (II) Zone B1 (III) Zone B2 (IV) Zone C1

Fig. 7. Typical waveforms of MP-BDC in the boost mode - Part I: (I) $0 < D_1^{\mathrm{d}} \le D_2^{\mathrm{d}} \le 0.5$, (II) $0 < D_2^{\mathrm{d}} \le D_1^{\mathrm{d}} \le 0.5$, (III) $0.5 \le D_1^{\mathrm{d}} < 1$, $0 < D_2^{\mathrm{d}} \le 0.5$ and $D_1^{\mathrm{d}} + D_2^{\mathrm{d}} \le 1$, (IV) $0.5 \le D_1^{\mathrm{d}} < 1$, $0 < D_2^{\mathrm{d}} \le 0.5$ and $D_1^{\mathrm{d}} + D_2^{\mathrm{d}} \ge 1$.

$$
\begin{cases}
l_2 : D_2^{\mathrm{d}} = \dfrac{1 + (2k-5)D_1^{\mathrm{d}} + 2\left(D_1^{\mathrm{d}}\right)^2}{1 + (4k-5)D_1^{\mathrm{d}} + 2\left(D_1^{\mathrm{d}}\right)^2} \\
l_3 : D_2^{\mathrm{d}} = \dfrac{1 - 5D_1^{\mathrm{d}} + 2\left(D_1^{\mathrm{d}}\right)^2}{1 - 2k + (4k-5)D_1^{\mathrm{d}} + 2\left(D_1^{\mathrm{d}}\right)^2} \\
l_4 : 4k(1-D_1^{\mathrm{d}})\left(D_2^{\mathrm{d}}\right)^2 + (2D_1^{\mathrm{d}} - k - 1)D_2^{\mathrm{d}} \\
\qquad\qquad - 2D_1^{\mathrm{d}} + 1 = 0 \\
l_5 : (2k + 1 - 2D_1^{\mathrm{d}})\left(D_2^{\mathrm{d}}\right)^2 + (2\left(D_1^{\mathrm{d}}\right)^2 + (2k-1) \\
\qquad D_1^{\mathrm{d}} - 2k)D_2^{\mathrm{d}} - 2\left(D_1^{\mathrm{d}}\right)^2 + 3D_1^{\mathrm{d}} - 1 = 0 \\
l_6 : D_2^{\mathrm{d}} = \dfrac{5 - \sqrt{17}}{4}.
\end{cases}
\tag{3b}
$$

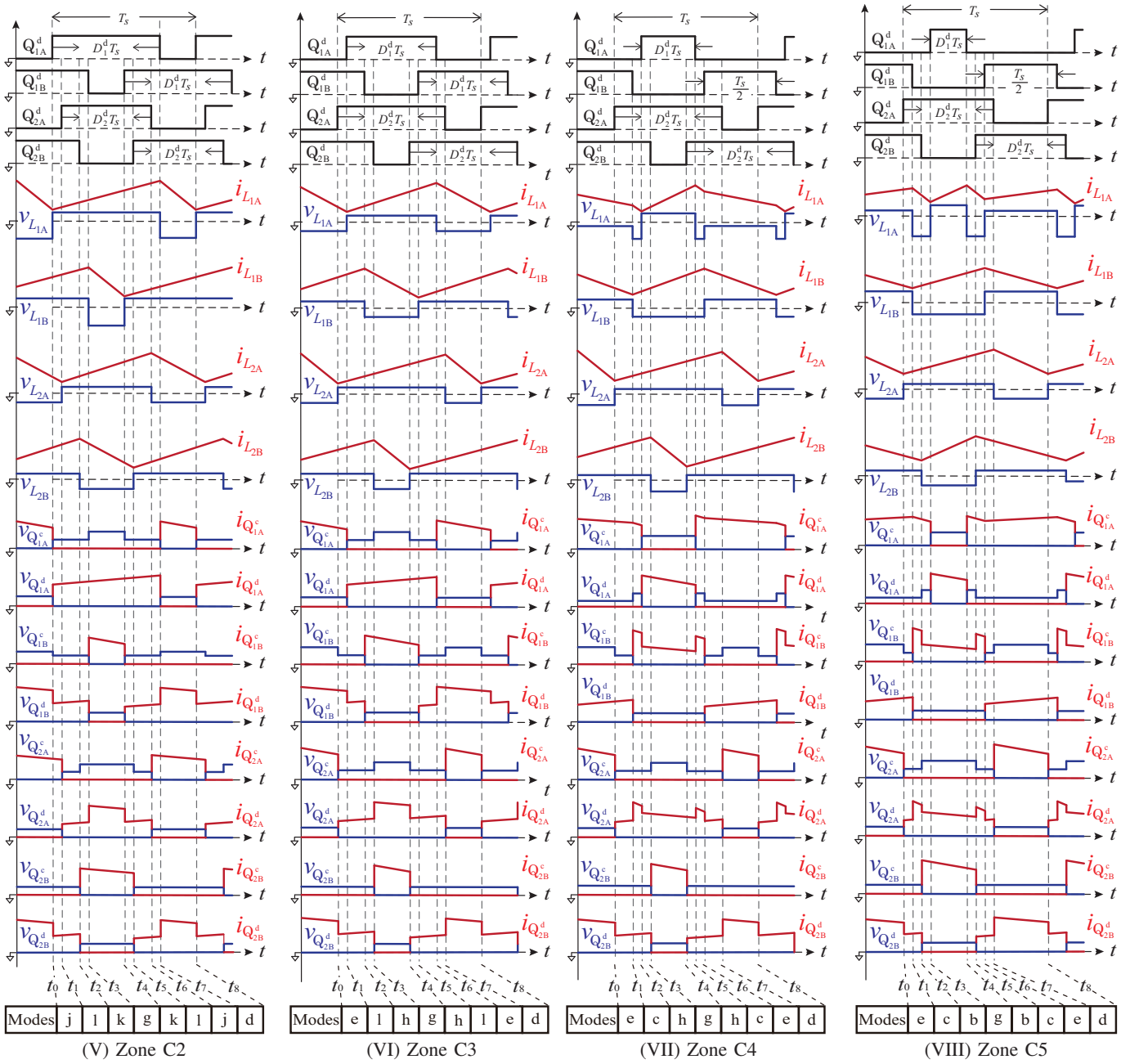
Where $k\,(0 < k < 1)$ represents the ratio of the V_{Low2} to the V_{Low1}.

In zone A of Fig. 11, the ampere-second balance applied to the capacitors $C_{1\mathrm{B}}$, $C_{2\mathrm{A}}$ and $C_{2\mathrm{B}}$ can be determined as

$$
\begin{cases}
-I_{\mathrm{L_{1A}}} + I_{\mathrm{L_{1B}}} = 0 \\
-I_{\mathrm{L_{1B}}}(2D_2^{\mathrm{d}} - D_1^{\mathrm{d}}) + I_{\mathrm{L_{2A}}}(1 - D_2^{\mathrm{d}}) = 0 \\
-I_{\mathrm{L_{2A}}} + I_{\mathrm{L_{2B}}} = 0.
\end{cases}
\tag{4}
$$

By rearranging (4), the relationship between the average currents of different low-voltage sides can be expressed as

$$
I_{\mathrm{Low1}}(2D_2^{\mathrm{d}} - D_1^{\mathrm{d}}) = I_{\mathrm{Low2}}(1 - D_2^{\mathrm{d}}). \tag{5}
$$



(V) Zone C2 (VI) Zone C3 (VII) Zone C4 (VIII) Zone C5

Fig. 8. Typical waveforms of MP-BDC in the boost mode - Part II: (V) $0.5 \leq D_1^{\mathrm{d}} < 1$, $0.5 \leq D_2^{\mathrm{d}} < 1$, and $D_2^{\mathrm{d}} \leq D_1^{\mathrm{d}}$, (VI) $0.5 \leq D_1^{\mathrm{d}} < 1$, $0.5 \leq D_2^{\mathrm{d}} < 1$, and $D_1^{\mathrm{d}} \leq D_2^{\mathrm{d}}$, (VII) $0 < D_1^{\mathrm{d}} \leq 0.5$, $0.5 \leq D_2^{\mathrm{d}} < 1$, and $D_1^{\mathrm{d}} + D_2^{\mathrm{d}} \geq 1$, (VIII) $0 < D_1^{\mathrm{d}} \leq 0.5$, $0.5 \leq D_2^{\mathrm{d}} < 1$, and $D_1^{\mathrm{d}} + D_2^{\mathrm{d}} \leq 1$.

Subsequently in zone B of Fig. 11, the ampere-second balance applied to the capacitors $C_{1\mathrm{B}}$, $C_{2\mathrm{A}}$ and $C_{2\mathrm{B}}$ can be given as

$$\begin{cases} -I_{\mathrm{L_{1A}}} + I_{\mathrm{L_{1B}}} = 0 \\ -I_{\mathrm{L_{1B}}} D_2^{\mathrm{d}} + I_{\mathrm{L_{2A}}}(1 - D_2^{\mathrm{d}}) = 0 \\ -I_{\mathrm{L_{2A}}} + I_{\mathrm{L_{2B}}} = 0. \end{cases} \tag{6}$$

Rearranging (6) yields the relationship between the average inductor currents

$$I_{\mathrm{Low1}} D_2^{\mathrm{d}} = I_{\mathrm{Low2}}(1 - D_2^{\mathrm{d}}). \tag{7}$$

Finally, in zone C of Fig. 11, the ampere-second balance applied to the capacitors $C_{1\mathrm{B}}$, $C_{2\mathrm{A}}$ and $C_{2\mathrm{B}}$ is described as follows

$$\begin{cases} -I_{\mathrm{L_{1A}}} + I_{\mathrm{L_{1B}}} = 0 \\ -I_{\mathrm{L_{1B}}}(1 - D_1^{\mathrm{d}}) + I_{\mathrm{L_{2A}}}(1 - D_2^{\mathrm{d}}) = 0 \\ -I_{\mathrm{L_{2A}}} + I_{\mathrm{L_{2B}}} = 0. \end{cases} \tag{8}$$

Rearranging (8) provides the relationship between the average inductor currents as

$$I_{\mathrm{Low1}}(1 - D_1^{\mathrm{d}}) = I_{\mathrm{Low2}}(1 - D_2^{\mathrm{d}}). \tag{9}$$

By combining (5), (7) and (9), the relationship between the average currents on different low-voltage sides can be

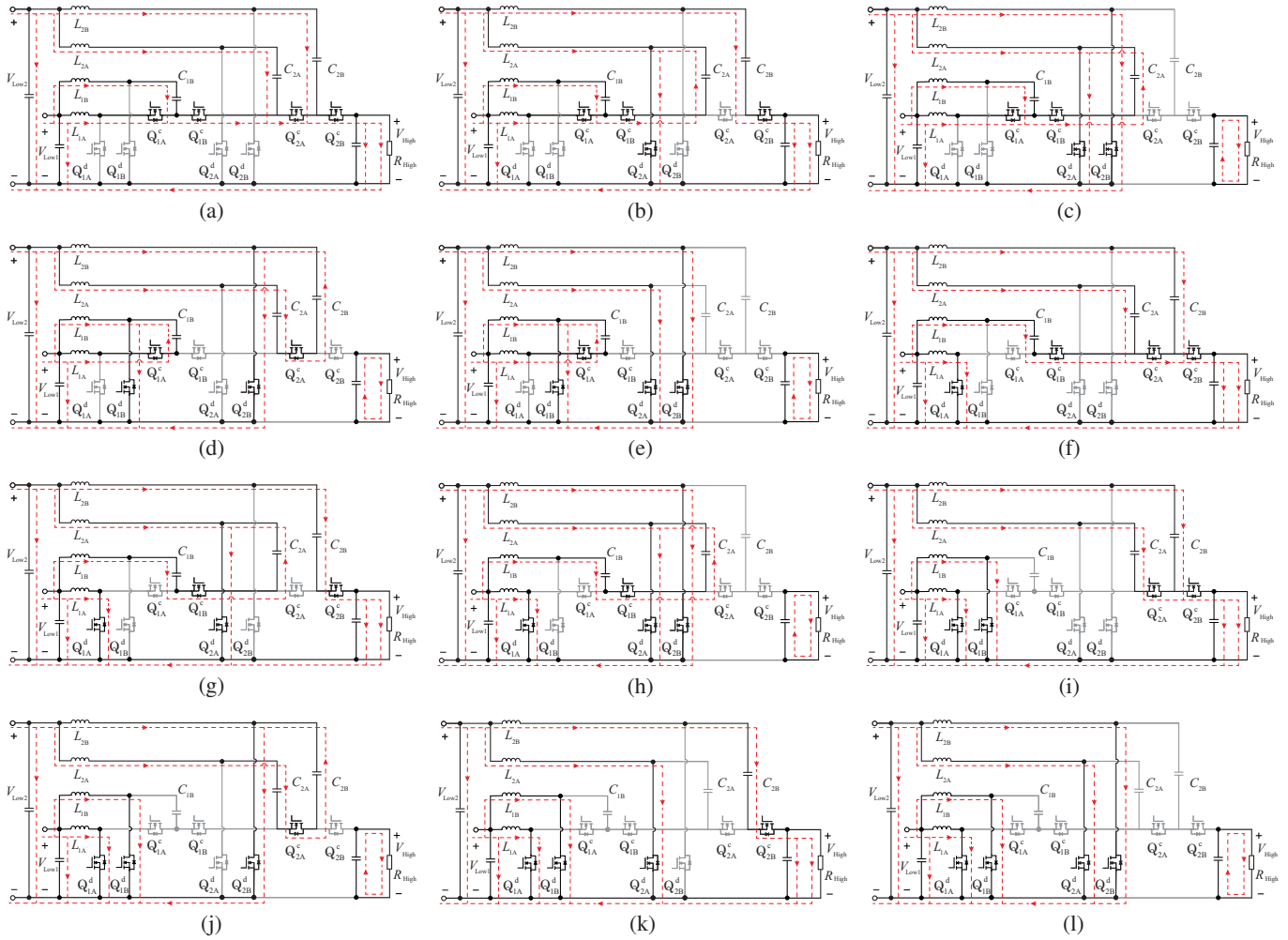


Fig. 9. Mode transitions and equivalent circuits in a boost mode during the switching one cycle.

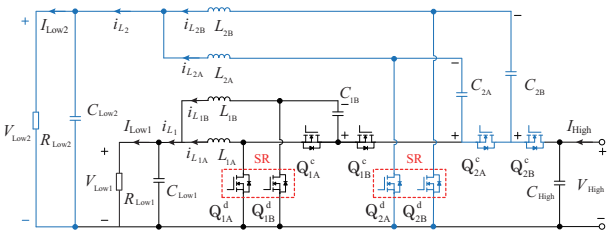


Fig. 10. Circuit configuration of MP-BDC in the buck mode.

summarized as

$$\begin{cases} I_{\mathrm{Low1}}(2D_2^{\mathrm{d}} - D_1^{\mathrm{d}}) = I_{\mathrm{Low2}}(1 - D_2^{\mathrm{d}}) \\ \qquad\qquad\qquad\qquad \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in A \\ I_{\mathrm{Low1}} D_2^{\mathrm{d}} = I_{\mathrm{Low2}}(1 - D_2^{\mathrm{d}}) \quad \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in B \\ I_{\mathrm{Low1}}(1 - D_1^{\mathrm{d}}) = I_{\mathrm{Low2}}(1 - D_2^{\mathrm{d}}) \quad \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in C. \end{cases} \tag{10}$$

It is evident that the inductor currents at each low-voltage side port are equal across the entire range of duty cycle with the assistance of A-DLC2. Moreover, when D_1^{d} and D_2^{d} satisfy equations L_{a} and L_{c}, all the inductor currents become equal, enabling effective power sharing among the low-voltage ports. Here, L_{a} and L_{c} can be expressed as

$$\begin{cases} L_{\mathrm{a}} : 1 + D_1^{\mathrm{d}} - 3D_2^{\mathrm{d}} = 0 \\ L_{\mathrm{c}} : D_1^{\mathrm{d}} - D_2^{\mathrm{d}} = 0. \end{cases} \tag{11}$$

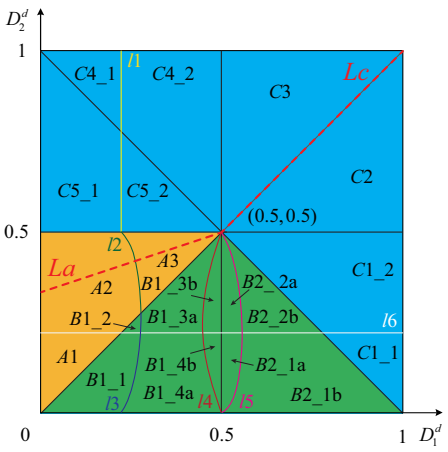


Fig. 11. Range of zones A, B, and C in the boost mode, ($A = A_1 \cup A_2 \cup A_3, B1\_3 = B1\_3a \cup B1\_3b, B1\_4 = B1\_4a \cup B1\_4b, B2\_1 = B2\_1a \cup B2\_1b, B2\_2 = B2\_2a \cup B2\_2b, B1 = B1\_1 \cup B1\_2 \cup B1\_3 \cup B1\_4, B2 = B2\_1 \cup B2\_2, B = B1 \cup B2, C1 = C1\_1 \cup C1\_2, C4 = C4\_1 \cup C4\_2, C5 = C5\_1 \cup C5\_2, C = C1 \cup C2 \cup C3 \cup C4 \cup C5$).

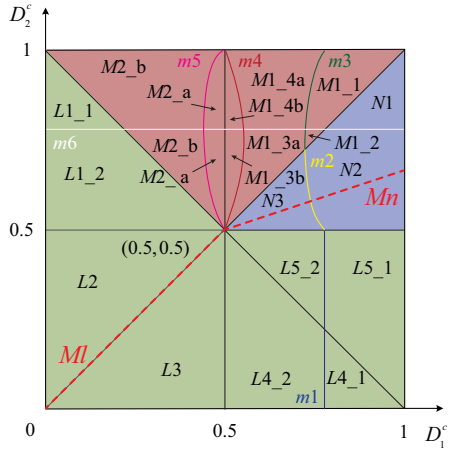


Fig. 12. Range of zones L, M, and N in the buck mode, ($L1 = L1\_1 \cup L1\_2, L4 = L4\_1 \cup L4\_2, L5 = L5\_1 \cup L5\_2, L = L1 \cup L2 \cup L3 \cup L4 \cup L5, M1\_3 = M1\_3a \cup M1\_3b, M1\_4 = M1\_4a \cup M1\_4b, M2\_1 = M2\_1a \cup M2\_1b, M2\_2 = M2\_2a \cup B2\_2b, M1 = M1\_1 \cup M1\_2 \cup M1\_3 \cup M1\_4, M2 = M2\_1 \cup M2\_2, M = M1 \cup M2, N = N_1 \cup N_2 \cup N_3$).

2) Buck Mode: Similarly, in the buck mode, depending on the distinctive section of A-DLC1, the full duty cycle range can be divided into three sections: L, M, and N. The ranges for zones L, M, and N in the buck mode are depicted in Fig. 12, where m_1 through m_6 fulfill the following equations.

$$\begin{cases} m_1 : D_1^{\mathrm{c}} = \dfrac{\sqrt{17}-1}{4} \\ m_2 : D_2^{\mathrm{c}} = \dfrac{2k-2+(1-2k)D_1^{\mathrm{c}}+2\left(D_1^{\mathrm{c}}\right)^2}{4k-2+(1-4k)D_1^{\mathrm{c}}+2\left(D_1^{\mathrm{c}}\right)^2} \\ m_3 : D_2^{\mathrm{c}} = \dfrac{-2+D_1^{\mathrm{c}}+2\left(D_1^{\mathrm{c}}\right)^2}{2k-2+(1-4k)D_1^{\mathrm{c}}+2\left(D_1^{\mathrm{c}}\right)^2} \\ m_4 : 4kD_1^{\mathrm{c}}\left(D_2^{\mathrm{c}}\right)^2-((8k-2)D_1^{\mathrm{c}}-k+1)D_2^{\mathrm{c}} \\ \qquad\qquad +k(4D_1^{\mathrm{c}}-1)=0 \\ m_5 : (2k-1+2D_1^{\mathrm{c}})\left(D_2^{\mathrm{c}}\right)^2-(2\left(D_1^{\mathrm{c}}\right)^2+(1-2k) \\ \qquad D_1^{\mathrm{c}}+4k-1)D_2^{\mathrm{c}}+2k(1-D_1^{\mathrm{c}})=0 \\ m_6 : D_2^{\mathrm{c}} = \dfrac{\sqrt{17}-1}{4}. \end{cases} \tag{12}$$

In zone L of Fig. 12, the ampere-second balance applied to capacitors $C_{1\mathrm{B}}$, $C_{2\mathrm{A}}$ and $C_{2\mathrm{B}}$ is derived as

$$\begin{cases} -I_{\mathrm{L_{1A}}}+I_{\mathrm{L_{1B}}}=0 \\ -I_{\mathrm{L_{1B}}}D_1^{\mathrm{c}}+I_{\mathrm{L_{2A}}}D_2^{\mathrm{c}}=0 \\ -I_{\mathrm{L_{2A}}}+I_{\mathrm{L_{2B}}}=0. \end{cases} \tag{13}$$

Rearranging (13) yields the relationship between the average currents of the inductors as

$$I_{\mathrm{Low1}}D_1^{\mathrm{c}} = I_{\mathrm{Low2}}D_2^{\mathrm{c}}. \tag{14}$$

Subsequently, in zone M of Fig. 12, the ampere-second balance applied to the capacitors $C_{1\mathrm{B}}$, $C_{2\mathrm{A}}$ and $C_{2\mathrm{B}}$ can be established as

$$\begin{cases} -I_{\mathrm{L_{1A}}}+I_{\mathrm{L_{1B}}}=0 \\ -I_{\mathrm{L_{1B}}}(1-D_2^{\mathrm{c}})+I_{\mathrm{L_{2A}}}D_2^{\mathrm{c}}=0 \\ -I_{\mathrm{L_{2A}}}+I_{\mathrm{L_{2B}}}=0. \end{cases} \tag{15}$$

By reconfiguring (15), the relationship between the average inductor currents can be expressed as

$$I_{\mathrm{Low1}}(1-D_2^{\mathrm{c}}) = I_{\mathrm{Low2}}D_2^{\mathrm{c}}. \tag{16}$$

Finally, in zone N of Fig. 12, the ampere-second balance applied to the capacitors $C_{1\mathrm{B}}$, $C_{2\mathrm{A}}$ and $C_{2\mathrm{B}}$ can be represented as

$$\begin{cases} -I_{\mathrm{L_{1A}}}+I_{\mathrm{L_{1B}}}=0 \\ -I_{\mathrm{L_{1B}}}(1+D_1^{\mathrm{c}}-2D_2^{\mathrm{c}})+I_{\mathrm{L_{2A}}}D_2^{\mathrm{c}}=0 \\ -I_{\mathrm{L_{2A}}}+I_{\mathrm{L_{2B}}}=0. \end{cases} \tag{17}$$

By reorganizing (17), the relationship between the average inductor currents is expressed as

$$I_{\mathrm{Low1}}(1+D_1^{\mathrm{c}}-2D_2^{\mathrm{c}}) = I_{\mathrm{Low2}}D_2^{\mathrm{c}}. \tag{18}$$

The correlation between the average currents on different low-voltage sides can be outlined as

$$\begin{cases} I_{\mathrm{Low1}}D_1^{\mathrm{c}} = I_{\mathrm{Low2}}D_2^{\mathrm{c}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in L \\ I_{\mathrm{Low1}}(1-D_2^{\mathrm{c}}) = I_{\mathrm{Low2}}D_2^{\mathrm{c}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in M \\ I_{\mathrm{Low1}}(1+D_1^{\mathrm{c}}-2D_2^{\mathrm{c}}) = I_{\mathrm{Low2}}D_2^{\mathrm{c}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in N. \end{cases} \tag{19}$$

It is also clear that the inductor currents at each port on the low-voltage side are uniform across the entire duty cycle range with the help of A-DLC1. Moreover, when D_1^{c} and D_2^{c} satisfy equations M_{l} and M_{n}, the equilibrium of all the inductor currents can likewise be achieved. Here, M_{l} and M_{n} can be expressed as

$$\begin{cases} M_{\mathrm{l}} : D_1^{\mathrm{c}} - D_2^{\mathrm{c}} = 0 \\ M_{\mathrm{n}} : 1+D_1^{\mathrm{c}} - 3D_2^{\mathrm{c}} = 0. \end{cases} \tag{20}$$

Consequently, it can be concluded that, whether in the boost or buck mode, the DC inductor currents are automatically balanced with the help of A-DLC.

B. Voltage Conversion Ratio in Steady-State

1) Boost Mode: In zone A of Fig. 11, the voltage-second balance applied to the inductors $L_{1\mathrm{A}}$, $L_{1\mathrm{B}}$, $L_{2\mathrm{A}}$ and $L_{2\mathrm{B}}$ are described as

$$\begin{cases} L_{1\mathrm{A}} : 2V_{\mathrm{Low1}} - V_{\mathrm{C_{1B}}} - 2V_{\mathrm{C_{2A}}}(D_2^{\mathrm{d}} - D_1^{\mathrm{d}}) \\ \qquad\qquad - V_{\mathrm{High}}(1-2D_2^{\mathrm{d}}) = 0 \\ L_{1\mathrm{B}} : 2V_{\mathrm{Low1}} + V_{\mathrm{C_{1B}}} - 2V_{\mathrm{C_{2A}}}D_2^{\mathrm{d}} - V_{\mathrm{High}}(1-2D_2^{\mathrm{d}}) = 0 \\ L_{2\mathrm{A}} : 2V_{\mathrm{Low2}} + 2V_{\mathrm{C_{2A}}}(1-D_2^{\mathrm{d}}) - V_{\mathrm{C_{2B}}} \\ \qquad\qquad - V_{\mathrm{High}}(1-2D_2^{\mathrm{d}}) = 0 \\ L_{2\mathrm{B}} : 2V_{\mathrm{Low2}} + V_{\mathrm{C_{2B}}} - V_{\mathrm{High}} = 0. \end{cases} \tag{21}$$

Simplifying (21) gives birth to a set of equations as

$$\begin{cases} V_{\mathrm{C_{1B}}} = PD_1^{\mathrm{d}} + Q\dfrac{D_1^{\mathrm{d}}(2D_2^{\mathrm{d}}-1)}{(1-D_1^{\mathrm{d}})} \\ V_{\mathrm{C_{2A}}} = P + Q\dfrac{(2D_2^{\mathrm{d}}-1)}{(1-D_1^{\mathrm{d}})} \\ V_{\mathrm{C_{2B}}} = P + Q\dfrac{(3D_2^{\mathrm{d}}-D_1^{\mathrm{d}}D_2^{\mathrm{d}}-1)}{(1-D_1^{\mathrm{d}})} \\ V_{\mathrm{High}} = P + Q\dfrac{(2D_2^{\mathrm{d}}-D_1^{\mathrm{d}})}{(1-D_1^{\mathrm{d}})}. \end{cases} \tag{22}$$

The definitions of P and Q are as follows, representing the primary influence of the low-voltage inputs on the high-voltage output:

$$P = \frac{2V_{\mathrm{Low1}}}{(1-D_1^{\mathrm{d}})} \tag{23}$$

$$Q = \frac{2V_{\mathrm{Low2}}}{(1-D_2^{\mathrm{d}})}. \tag{24}$$

In zone B of Fig. 11, the voltage-second balance applied to the inductors $L_{1\mathrm{A}}$, $L_{1\mathrm{B}}$, $L_{2\mathrm{A}}$ and $L_{2\mathrm{B}}$ can be determined as

$$\begin{cases} L_{1\mathrm{A}}: \begin{cases} 2V_{\mathrm{Low1}} - V_{\mathrm{C_{1B}}} - V_{\mathrm{High}}(1-2D_1^{\mathrm{d}}) = 0 \\ \qquad\qquad\qquad\qquad \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in B1 \\ V_{\mathrm{Low1}} - V_{\mathrm{C_{1B}}}(1-D_1^{\mathrm{d}}) = 0 \quad \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in B2 \end{cases} \\ L_{1\mathrm{B}}: 2V_{\mathrm{Low1}} - V_{\mathrm{C_{2A}}}D_2^{\mathrm{d}} - V_{\mathrm{High}}(1-D_1^{\mathrm{d}} - D_2^{\mathrm{d}}) = 0 \\ L_{2\mathrm{A}}: 2V_{\mathrm{Low2}} + 2V_{\mathrm{C_{2A}}}(1-D_2^{\mathrm{d}}) - V_{\mathrm{C_{2B}}} \\ \qquad\qquad - V_{\mathrm{High}}(1-2D_2^{\mathrm{d}}) = 0 \\ L_{2\mathrm{B}}: 2V_{\mathrm{Low2}} + V_{\mathrm{C_{2B}}} - V_{\mathrm{High}} = 0. \end{cases} \tag{25}$$

By simplifying (25), a set of equations can be obtained as

$$\begin{cases} V_{\mathrm{C_{1B}}} = \begin{cases} PD_1^{\mathrm{d}} + Q\dfrac{D_2^{\mathrm{d}}(2D_1^{\mathrm{d}}-1)}{1-D_1^{\mathrm{d}}} & \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in B1 \\ \dfrac{P}{2} & \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in B2 \end{cases} \\ V_{\mathrm{C_{2A}}} = P + Q\dfrac{(D_1^{\mathrm{d}} + D_2^{\mathrm{d}} - 1)}{1-D_1^{\mathrm{d}}} \\ V_{\mathrm{C_{2B}}} = P + Q\dfrac{(D_1^{\mathrm{d}} + 2D_2^{\mathrm{d}} - D_1^{\mathrm{d}}D_2^{\mathrm{d}} - 1)}{(1-D_1^{\mathrm{d}})} \\ V_{\mathrm{High}} = P + Q\dfrac{D_2^{\mathrm{d}}}{(1-D_1^{\mathrm{d}})}. \end{cases} \tag{26}$$

Finally, in zone C of Fig. 11, the voltage-second balance applied to the inductors $L_{1\mathrm{A}}$, $L_{1\mathrm{B}}$, $L_{2\mathrm{A}}$ and $L_{2\mathrm{B}}$ can be expressed as

$$\begin{cases} L_{1\mathrm{A}}: \begin{cases} V_{\mathrm{Low1}} - V_{\mathrm{C_{1B}}}(1-D_1^{\mathrm{d}}) = 0 \\ \qquad\qquad \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in C1 \cup C2 \cup C3 \\ 2V_{\mathrm{Low1}} - V_{\mathrm{C_{1B}}} - V_{\mathrm{C_{2A}}}(1-2D_1^{\mathrm{d}}) = 0 \\ \qquad\qquad \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in C4 \cup C5 \end{cases} \\ L_{1\mathrm{B}}: \begin{cases} V_{\mathrm{Low1}} + V_{\mathrm{C_{1B}}}(1-D_1^{\mathrm{d}}) - V_{\mathrm{C_{2A}}}(1-D_1^{\mathrm{d}}) = 0 \\ \qquad\qquad \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in C1 \cup C2 \cup C3 \\ 2V_{\mathrm{Low1}} + V_{\mathrm{C_{1B}}} - V_{\mathrm{C_{2A}}} = 0 \\ \qquad\qquad \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in C4 \cup C5 \end{cases} \\ L_{2\mathrm{A}}: \begin{cases} 2V_{\mathrm{Low2}} + 2V_{\mathrm{C_{2A}}}(1-D_2^{\mathrm{d}}) - V_{\mathrm{C_{2B}}} \\ \qquad\qquad - V_{\mathrm{High}}(1-2D_2^{\mathrm{d}}) = 0 \\ \qquad\qquad \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in C1 \\ V_{\mathrm{Low2}} + V_{\mathrm{C_{2A}}}(1-D_2^{\mathrm{d}}) - V_{\mathrm{C_{2B}}}(1-D_2^{\mathrm{d}}) = 0 \\ \qquad\qquad \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in C2 \cup C3 \cup C4 \cup C5 \end{cases} \\ L_{2\mathrm{B}}: \begin{cases} 2V_{\mathrm{Low2}} + V_{\mathrm{C_{2B}}} - V_{\mathrm{High}} = 0 \ \text{ when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in C1 \\ V_{\mathrm{Low2}} + V_{\mathrm{C_{2B}}}(1-D_2^{\mathrm{d}}) - V_{\mathrm{High}}(1-D_2^{\mathrm{d}}) = 0 \\ \qquad\qquad \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in C2 \cup C3 \cup C4 \cup C5. \end{cases} \end{cases} \tag{27}$$

By simplifying (27), the following equations can be formulated as

$$\begin{cases} V_{\mathrm{C_{1B}}} = \begin{cases} \dfrac{P}{2} & \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in C1 \cup C2 \cup C3 \\ PD_1^{\mathrm{d}} & \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in C4 \cup C5 \end{cases} \\ V_{\mathrm{C_{2A}}} = P \\ V_{\mathrm{C_{2B}}} = \begin{cases} P + QD_2^{\mathrm{d}} & \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in C1 \\ P + \dfrac{Q}{2} & \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in C2 \cup C3 \cup C4 \cup C5 \end{cases} \\ V_{\mathrm{High}} = P + Q. \end{cases} \tag{28}$$

For the sake of simplicity in the analysis, the equivalent low-side voltage can be defined as

$$V_{\mathrm{Leq}} = \frac{V_{\mathrm{Low1}} + V_{\mathrm{Low2}}}{2}. \tag{29}$$

When D_1^{d} and D_2^{d} satisfy equations L_{a} and L_{c}, replacing V_{Low1} and V_{Low2} with V_{Leq} can achieve the same effect of VCR. The equivalent normalized voltages of V_{Low1} and V_{Low2} are respectively expressed as

$$M_1 = \frac{V_{\mathrm{Low1}}}{V_{\mathrm{Leq}}} = \frac{2V_{\mathrm{Low1}}}{V_{\mathrm{Low1}} + V_{\mathrm{Low2}}} \tag{30}$$

$$M_2 = \frac{V_{\mathrm{Low2}}}{V_{\mathrm{Leq}}} = \frac{2V_{\mathrm{Low2}}}{V_{\mathrm{Low1}} + V_{\mathrm{Low2}}}. \tag{31}$$

By combining (22), (26), (28) - (31), the overall voltage conversion ratio in the boost mode can be summarized as

$$G_{\mathrm{boost}} = \frac{V_{\mathrm{High}}}{V_{\mathrm{Leq}}} = \begin{cases} \dfrac{2M_1(1-D_2^{\mathrm{d}}) + 2M_2(2D_2^{\mathrm{d}} - D_1^{\mathrm{d}})}{(1-D_1^{\mathrm{d}})(1-D_2^{\mathrm{d}})} \\ \qquad\qquad \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in A \\ \dfrac{2M_1(1-D_2^{\mathrm{d}}) + 2M_2D_2^{\mathrm{d}}}{(1-D_1^{\mathrm{d}})(1-D_2^{\mathrm{d}})} \\ \qquad\qquad \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in B \\ \dfrac{2M_1(1-D_2^{\mathrm{d}}) + 2M_2(1-D_1^{\mathrm{d}})}{(1-D_1^{\mathrm{d}})(1-D_2^{\mathrm{d}})} \\ \qquad\qquad \text{when } (D_1^{\mathrm{d}}, D_2^{\mathrm{d}}) \in C. \end{cases} \tag{32}$$

When the low-side voltages are maintained at 72 V and 48 V respectively, as indicated by (32), the voltage conversion ratio of the proposed BDC is presented in Fig. 13. The voltage ratio G_{boost} spans from 2.86 to 40 within the range of $0.1 \le D_1^{\mathrm{d}} \le 0.9$ and $0.1 \le D_2^{\mathrm{d}} \le 0.9$ in the boost mode. This demonstrates that the proposed topology is capable of achieving a wide range of boost ratios.

2) Buck Mode: In zone L of Fig. 12, the voltage-second balance applied to inductors $L_{1\mathrm{A}}$, $L_{1\mathrm{B}}$, $L_{2\mathrm{A}}$ and $L_{2\mathrm{B}}$ is described as

$$\begin{cases} L_{1\mathrm{A}}: \begin{cases} I_{\mathrm{Low1}}R_{\mathrm{Low1}} - V_{\mathrm{C_{1B}}}D_1^{\mathrm{c}} = 0 \\ \qquad\qquad \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in L1 \cup L2 \cup L3 \\ 2I_{\mathrm{Low1}}R_{\mathrm{Low1}} - V_{\mathrm{C_{1B}}} + V_{\mathrm{C_{2A}}}(1-2D_1^{\mathrm{c}}) = 0 \\ \qquad\qquad \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in L4 \cup L5 \end{cases} \end{cases} \tag{33a}$$

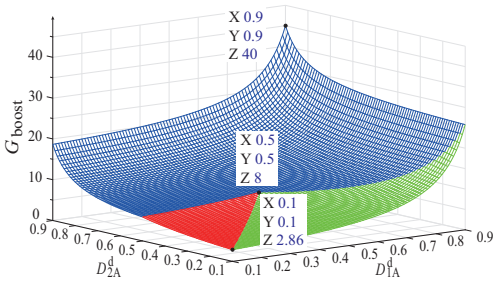


Fig. 13. Theoretical values of DC voltage ratio in the boost mode with M_1 = 1.2 and M_2 = 0.8.

TABLE I
DEFINITIONS OF S AND T IN BUCK MODE

S	T	α, β
$S_{\text{L}} = \dfrac{R_1\beta_{\text{L}}^2 V_{\text{High}}}{R_1\beta_{\text{L}}^2 + R_2\alpha_{\text{L}}^2}$	$T_{\text{L}} = \dfrac{R_2 D_1^{\text{c}}\alpha_{\text{L}} V_{\text{High}}}{R_1\beta_{\text{L}}^2 + R_2\alpha_{\text{L}}^2}$	$\alpha_{\text{L}} = D_1^{\text{c}}$, $\beta_{\text{L}} = D_2^{\text{c}}$
$S_{\text{M}} = \dfrac{R_1\beta_{\text{M}}^2 V_{\text{High}}}{R_1\beta_{\text{M}}^2 + R_2\alpha_{\text{M}}^2}$	$T_{\text{M}} = \dfrac{R_2 D_1^{\text{c}}\alpha_{\text{M}} V_{\text{High}}}{R_1\beta_{\text{M}}^2 + R_2\alpha_{\text{M}}^2}$	$\alpha_{\text{M}} = 1 - D_2^{\text{c}}$, $\beta_{\text{M}} = D_2^{\text{c}}$
$S_{\text{N}} = \dfrac{R_1\beta_{\text{N}}^2 V_{\text{High}}}{R_1\beta_{\text{N}}^2 + R_2\alpha_{\text{N}}^2}$	$T_{\text{N}} = \dfrac{R_2 D_1^{\text{c}}\alpha_{\text{N}} V_{\text{High}}}{R_1\beta_{\text{N}}^2 + R_2\alpha_{\text{N}}^2}$	$\alpha_{\text{N}} = 1 + D_1^{\text{c}} - 2D_2^{\text{c}}$, $\beta_{\text{N}} = D_2^{\text{c}}$

Note: R_1 and R_2 represent R_{Low1} and R_{Low2}, respectively.

$$\begin{cases} L_{1\text{B}}: \begin{cases} I_{\text{Low1}}R_{\text{Low1}} + V_{\text{C}_{1\text{B}}}D_1^{\text{c}} - V_{\text{C}_{2\text{A}}}D_1^{\text{c}} = 0 \\ \qquad \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L1 \cup L2 \cup L3 \\ 2I_{\text{Low1}}R_{\text{Low1}} + V_{\text{C}_{1\text{B}}} - V_{\text{C}_{2\text{A}}} = 0 \\ \qquad \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L4 \cup L5 \end{cases} \\ L_{2\text{A}}: \begin{cases} 2I_{\text{Low2}}R_{\text{Low2}} + 2V_{\text{C}_{2\text{A}}}D_2^{\text{c}} - V_{\text{C}_{2\text{B}}} \\ \qquad + V_{\text{High}}(1 - 2D_2^{\text{c}}) = 0 \\ \qquad \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L1 \\ I_{\text{Low2}}R_{\text{Low2}} + V_{\text{C}_{2\text{A}}}D_2^{\text{c}} - V_{\text{C}_{2\text{B}}}D_2^{\text{c}} = 0 \\ \qquad \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L2 \cup L3 \cup L4 \cup L5 \end{cases} \\ L_{2\text{B}}: \begin{cases} 2I_{\text{Low2}}R_{\text{Low2}} + V_{\text{C}_{2\text{B}}} - V_{\text{High}} = 0 \\ \qquad \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L1 \\ I_{\text{Low2}}R_{\text{Low2}} + V_{\text{C}_{2\text{B}}}D_2^{\text{c}} - V_{\text{High}}D_2^{\text{c}} = 0 \\ \qquad \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L2 \cup L3 \cup L4 \cup L5. \end{cases} \end{cases} \tag{33b}$$

By streamlining (33a) and (33b), the another mathematical expressions are obtained as

$$\begin{cases} V_{\text{C}_{1\text{B}}} = \begin{cases} \dfrac{S_{\text{L}}}{2} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L1 \cup L2 \cup L3 \\ S_{\text{L}}(1 - D_1^{\text{c}}) & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L4 \cup L5 \end{cases} \\ V_{\text{C}_{2\text{A}}} = S_{\text{L}} \\ V_{\text{C}_{2\text{B}}} = \begin{cases} S_{\text{L}} + T_{\text{L}}(1 - D_2^{\text{c}}) & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L1 \\ S_{\text{L}} + \dfrac{T_{\text{L}}}{2} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L2 \cup L3 \cup L4 \cup L5 \end{cases} \\ V_{\text{Low1}} = S_{\text{L}}\dfrac{D_1^{\text{c}}}{2} \\ V_{\text{Low2}} = T_{\text{L}}\dfrac{D_2^{\text{c}}}{2}. \end{cases} \tag{34}$$

The definitions of S and T are provided in TABLE I, which highlight the essential impact of the high-voltage port on the low-voltage ports. Subsequently, in zone M of Fig. 12, the voltage-second balance applied to inductors $L_{1\text{A}}$, $L_{1\text{B}}$, $L_{2\text{A}}$ and $L_{2\text{B}}$ is characterized as

$$\begin{cases} L_{1\text{A}}: \begin{cases} 2I_{\text{Low1}}R_{\text{Low1}} - V_{\text{C}_{1\text{B}}} + V_{\text{High}}(1 - 2D_1^{\text{c}}) = 0 \\ \qquad \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in M1 \\ I_{\text{Low1}}R_{\text{Low1}} - V_{\text{C}_{1\text{B}}}D_1^{\text{c}} = 0 \text{ when } (D_1^{\text{c}}, D_2^{\text{c}}) \in M2 \end{cases} \\ L_{1\text{B}}: 2I_{\text{Low1}}R_{\text{Low1}} - V_{\text{C}_{2\text{A}}}(1 - D_2^{\text{c}}) \\ \qquad + V_{\text{High}}(1 - D_1^{\text{c}} - D_2^{\text{c}}) = 0 \\ L_{2\text{A}}: 2I_{\text{Low2}}R_{\text{Low2}} + 2V_{\text{C}_{2\text{A}}}D_2^{\text{c}} - V_{\text{C}_{2\text{B}}} \\ \qquad + V_{\text{High}}(1 - 2D_2^{\text{c}}) = 0 \\ L_{2\text{B}}: 2I_{\text{Low2}}R_{\text{Low2}} + V_{\text{C}_{2\text{B}}} - V_{\text{High}} = 0. \end{cases} \tag{35}$$

Simplifying (35) then yields the results as

$$\begin{cases} V_{\text{C}_{1\text{B}}} = \begin{cases} S_{\text{M}}(1 - D_1^{\text{c}}) + T_{\text{M}}\dfrac{(1 - 2D_1^{\text{c}})(1 - D_2^{\text{c}})}{D_1^{\text{c}}} \\ \qquad \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in M1 \\ \dfrac{S_{\text{M}}}{2} \qquad \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in M2 \end{cases} \\ V_{\text{C}_{2\text{A}}} = S_{\text{M}} + T_{\text{M}}\dfrac{(1 - D_1^{\text{c}} - D_2^{\text{c}})}{D_1^{\text{c}}} \\ V_{\text{C}_{2\text{B}}} = S_{\text{M}} + T_{\text{M}}\dfrac{(1 - D_1^{\text{c}}D_2^{\text{c}} - D_2^{\text{c}})}{D_1^{\text{c}}} \\ V_{\text{Low1}} = S_{\text{M}}\dfrac{D_1^{\text{c}}}{2} \\ V_{\text{Low2}} = T_{\text{M}}\dfrac{D_2^{\text{c}}}{2}. \end{cases} \tag{36}$$

Finally, in zone N of Fig. 12, the voltage-second balance applied to the inductors $L_{1\text{A}}$, $L_{1\text{B}}$, $L_{2\text{A}}$ and $L_{2\text{B}}$ is articulated as

$$\begin{cases} L_{1\text{A}}: 2I_{\text{Low1}}R_{\text{Low1}} - V_{\text{C}_{1\text{B}}} - 2V_{\text{C}_{2\text{A}}}(D_1^{\text{c}} - D_2^{\text{c}}) \\ \qquad + V_{\text{High}}(1 - 2D_2^{\text{c}}) = 0 \\ L_{1\text{B}}: 2I_{\text{Low1}}R_{\text{Low1}} + V_{\text{C}_{1\text{B}}} - 2V_{\text{C}_{2\text{A}}}(1 - D_2^{\text{c}}) \\ \qquad + V_{\text{High}}(1 - 2D_2^{\text{c}}) = 0 \\ L_{2\text{A}}: 2I_{\text{Low2}}R_{\text{Low2}} + 2V_{\text{C}_{2\text{A}}}D_2^{\text{c}} - V_{\text{C}_{2\text{B}}} \\ \qquad + V_{\text{High}}(1 - 2D_2^{\text{c}}) = 0 \\ L_{2\text{B}}: 2I_{\text{Low2}}R_{\text{Low2}} + V_{\text{C}_{2\text{B}}} - V_{\text{High}} = 0. \end{cases} \tag{37}$$

Streamlining (37) results in the following equations

$$\begin{cases} V_{\text{C}_{1\text{B}}} = S_{\text{N}}(1 - D_1^{\text{c}}) + T_{\text{N}}\dfrac{(1 - D_1^{\text{c}})(1 - 2D_2^{\text{c}})}{D_1^{\text{c}}} \\ V_{\text{C}_{2\text{A}}} = S_{\text{N}} + T_{\text{N}}\dfrac{1 - 2D_2^{\text{c}}}{D_1^{\text{c}}} \\ V_{\text{C}_{2\text{B}}} = S_{\text{N}} + T_{\text{N}}\dfrac{1 + D_1^{\text{c}} - 2D_2^{\text{c}} - D_1^{\text{c}}D_2^{\text{c}}}{D_1^{\text{c}}} \\ V_{\text{Low1}} = S_{\text{N}}\dfrac{D_1^{\text{c}}}{2} \\ V_{\text{Low2}} = T_{\text{N}}\dfrac{D_2^{\text{c}}}{2}. \end{cases} \tag{38}$$

By merging (29) - (31), (34), (36), (38), the comprehensive voltage conversion ratios in the buck mode are derived as

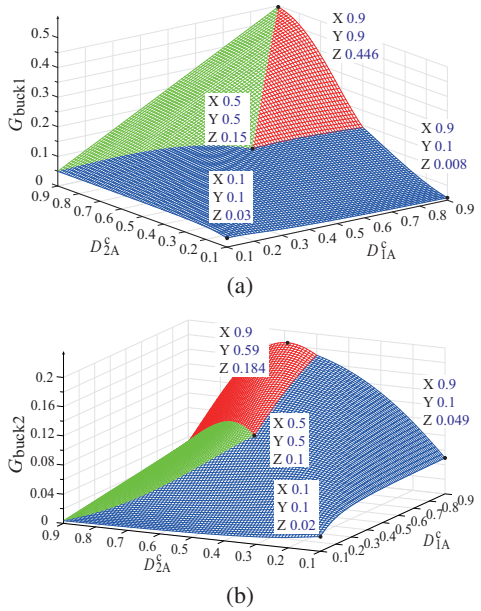


Fig. 14. Theoretical values of DC voltage ratio in the buck mode with $R_{\text{Low1}} = 3.46\,\Omega$ and $R_{\text{Low2}} = 2.30\,\Omega$: (a) G_{buck1}, and (b) G_{buck2}.

$$G_{\text{buck1}} = \frac{V_{\text{Low1}}}{V_{\text{High}}} = \begin{cases} \dfrac{R_{\text{Low1}} D_1^{\text{c}} \left(D_2^{\text{c}}\right)^2}{2\left(R_{\text{Low1}} \left(D_2^{\text{c}}\right)^2 + R_{\text{Low2}} \left(D_1^{\text{c}}\right)^2\right)} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L \\ \dfrac{R_{\text{Low1}} D_1^{\text{c}} \left(D_2^{\text{c}}\right)^2}{2\left(R_{\text{Low1}} \left(D_2^{\text{c}}\right)^2 + R_{\text{Low2}} \left(1 - D_2^{\text{c}}\right)^2\right)} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in M \\ \dfrac{R_{\text{Low1}} D_1^{\text{c}} \left(D_2^{\text{c}}\right)^2}{2\left(R_{\text{Low1}} \left(D_2^{\text{c}}\right)^2 + R_{\text{Low2}} \left(1 + D_1^{\text{c}} - 2D_2^{\text{c}}\right)^2\right)} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in N. \end{cases} \tag{39}$$

$$G_{\text{buck2}} = \frac{V_{\text{Low2}}}{V_{\text{High}}} = \begin{cases} \dfrac{R_{\text{Low2}} \left(D_1^{\text{c}}\right)^2 D_2^{\text{c}}}{2\left(R_{\text{Low1}} \left(D_2^{\text{c}}\right)^2 + R_{\text{Low2}} \left(D_1^{\text{c}}\right)^2\right)} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L \\ \dfrac{R_{\text{Low2}} D_1^{\text{c}} D_2^{\text{c}} (1 - D_2^{\text{c}})}{2\left(R_{\text{Low1}} \left(D_2^{\text{c}}\right)^2 + R_{\text{Low2}} \left(1 - D_2^{\text{c}}\right)^2\right)} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in M \\ \dfrac{R_{\text{Low2}} D_1^{\text{c}} D_2^{\text{c}} \left(1 + D_1^{\text{c}} - 2D_2^{\text{c}}\right)}{2\left(R_{\text{Low1}} \left(D_2^{\text{c}}\right)^2 + R_{\text{Low2}} \left(1 + D_1^{\text{c}} - 2D_2^{\text{c}}\right)^2\right)} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in N. \end{cases} \tag{40}$$

When the high-side voltage is held between $400\,\text{V}$ and $800\,\text{V}$, with $R_{\text{Low1}} = 3.46\,\Omega$ and $R_{\text{Low2}} = 2.30\,\Omega$, as specified by (39) and (40), the voltage conversion ratios of the proposed BDC are illustrated in Figs. 14(a) and (b), respectively. The voltage ratio G_{buck1} covers from 0.02 to 0.3 within the range of $0.1 \le D_1^{\text{c}} \le 0.9$ and $0.1 \le D_2^{\text{c}} \le 0.9$ in the buck mode. Moreover, the voltage ratio G_{buck2} varies from 0.03 to 0.5. This further indicates that the proposed topology is capable of achieving a broad range of buck ratios.

C. Analysis of Voltage Stresses on Power Devices

1) Boost Mode: By substituting (22), (26) and (28) into the state equations, the voltage stresses on the active switches in boost mode can be derived as

$$V_{\text{Q}_{1\text{A}}^{\text{c}}} = \begin{cases} V_{\text{C}_{2\text{A}}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in A \cup C \\ V_{\text{High}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in B. \end{cases} \tag{41}$$

$$V_{\text{Q}_{1\text{A}}^{\text{d}}} = \begin{cases} V_{\text{C}_{1\text{B}}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in B2 \cup C1 \cup C2 \cup C3 \\ V_{\text{C}_{2\text{A}}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in C4 \cup C5 \\ V_{\text{High}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in A \cup B1. \end{cases} \tag{42}$$

$$V_{\text{Q}_{1\text{B}}^{\text{c}}} = \begin{cases} V_{\text{High}} - V_{\text{C}_{1\text{B}}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in B2 \cup C1 \\ V_{\text{C}_{2\text{B}}} - V_{\text{C}_{1\text{B}}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in others. \end{cases} \tag{43}$$

$$V_{\text{Q}_{1\text{B}}^{\text{d}}} = \begin{cases} V_{\text{C}_{2\text{A}}} - V_{\text{C}_{1\text{B}}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in C \\ V_{\text{High}} - V_{\text{C}_{1\text{B}}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in A \cup B. \end{cases} \tag{44}$$

$$V_{\text{Q}_{2\text{A}}^{\text{c}}} = V_{\text{High}} - V_{\text{C}_{2\text{A}}}. \tag{45}$$

$$V_{\text{Q}_{2\text{A}}^{\text{d}}} = \begin{cases} V_{\text{High}} - V_{\text{C}_{2\text{A}}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in A \cup B \cup C1 \\ V_{\text{C}_{2\text{B}}} - V_{\text{C}_{2\text{A}}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in others. \end{cases} \tag{46}$$

$$V_{\text{Q}_{2\text{B}}^{\text{c}}} = V_{\text{Q}_{2\text{B}}^{\text{d}}} = V_{\text{High}} - V_{\text{C}_{2\text{B}}}. \tag{47}$$

2) Buck Mode: By applying (34), (36) and (38) to the state equations, the voltage stresses on the active switches in the buck mode can be expressed as

$$V_{\text{Q}_{1\text{A}}^{\text{c}}} = \begin{cases} V_{\text{C}_{2\text{A}}} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L \cup N \\ V_{\text{High}} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in M. \end{cases} \tag{48}$$

$$V_{\text{Q}_{1\text{A}}^{\text{d}}} = \begin{cases} V_{\text{C}_{1\text{B}}} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L1 \cup L2 \cup L3 \cup M2 \\ V_{\text{C}_{2\text{A}}} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L4 \cup L5 \\ V_{\text{High}} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in M1 \cup N. \end{cases} \tag{49}$$

$$V_{\text{Q}_{1\text{B}}^{\text{c}}} = \begin{cases} V_{\text{High}} - V_{\text{C}_{1\text{B}}} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L1 \cup M2 \\ V_{\text{C}_{2\text{B}}} - V_{\text{C}_{1\text{B}}} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in others. \end{cases} \tag{50}$$

$$V_{\text{Q}_{1\text{B}}^{\text{d}}} = \begin{cases} V_{\text{C}_{2\text{A}}} - V_{\text{C}_{1\text{B}}} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L \\ V_{\text{High}} - V_{\text{C}_{1\text{B}}} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in M \cup N. \end{cases} \tag{51}$$

$$V_{\text{Q}_{2\text{A}}^{\text{c}}} = V_{\text{High}} - V_{\text{C}_{2\text{A}}}. \tag{52}$$

$$V_{\text{Q}_{2\text{A}}^{\text{d}}} = \begin{cases} V_{\text{High}} - V_{\text{C}_{2\text{A}}} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in L1 \cup M \cup N \\ V_{\text{C}_{2\text{B}}} - V_{\text{C}_{2\text{A}}} & \text{when } (D_1^{\text{c}}, D_2^{\text{c}}) \in others. \end{cases} \tag{53}$$

$$V_{\text{Q}_{2\text{B}}^{\text{c}}} = V_{\text{Q}_{2\text{B}}^{\text{d}}} = V_{\text{High}} - V_{\text{C}_{2\text{B}}}. \tag{54}$$

D. Analysis of Inductor Current Ripples

1) Boost Mode: Assuming $L_{1\mathrm{A}}$, $L_{2\mathrm{A}}$, $L_{1\mathrm{B}}$ and $L_{2\mathrm{B}}$ have the same values, by combining (4) - (10), the DC components of the current through $L_{1\mathrm{A}}$, $L_{1\mathrm{B}}$, $L_{2\mathrm{A}}$ and $L_{2\mathrm{B}}$ can be theoretically expressed as (55) and (56), respectively.

$$I_{L_{1\mathrm{A}}} = I_{L_{1\mathrm{B}}} = 0.5I_{L_1} =$$
$$\begin{cases} \dfrac{V_{\mathrm{Leq}}(M_1+M_2)(M_1-D_1^{\mathrm{d}}M_2-D_2^{\mathrm{d}}M_1+2D_2^{\mathrm{d}}M_2)}{R_{\mathrm{High}}(1-D_1^{\mathrm{d}})^2(1-D_2^{\mathrm{d}})} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in A \\ \dfrac{V_{\mathrm{Leq}}(M_1+M_2)(M_1-D_2^{\mathrm{d}}M_1+D_2^{\mathrm{d}}M_2)}{R_{\mathrm{High}}(1-D_1^{\mathrm{d}})^2(1-D_2^{\mathrm{d}})} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in B \\ \dfrac{V_{\mathrm{Leq}}(M_1+M_2)(M_1+M_2-D_1^{\mathrm{d}}M_2-D_2^{\mathrm{d}}M_1)}{R_{\mathrm{High}}(1-D_1^{\mathrm{d}})^2(1-D_2^{\mathrm{d}})} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in C. \end{cases} \tag{55}$$

$$I_{L_{2\mathrm{A}}} = I_{L_{2\mathrm{B}}} = 0.5I_{L_2} =$$
$$\begin{cases} \dfrac{(2D_2^{\mathrm{d}}-D_1^{\mathrm{d}})I_{L_{1\mathrm{A}}}}{1-D_2^{\mathrm{d}}} = \dfrac{(2D_2^{\mathrm{d}}-D_1^{\mathrm{d}})I_{L_{1\mathrm{B}}}}{1-D_2^{\mathrm{d}}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in A \\ \dfrac{D_2^{\mathrm{d}}I_{L_{1\mathrm{A}}}}{1-D_2^{\mathrm{d}}} = \dfrac{D_2^{\mathrm{d}}I_{L_{1\mathrm{B}}}}{1-D_2^{\mathrm{d}}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in B \\ \dfrac{(1-D_1^{\mathrm{d}})I_{L_{1\mathrm{A}}}}{1-D_2^{\mathrm{d}}} = \dfrac{(1-D_1^{\mathrm{d}})I_{L_{1\mathrm{B}}}}{1-D_2^{\mathrm{d}}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in C. \end{cases} \tag{56}$$

The ripple current in each inductor can be expressed on the basis of the waveforms in Figs. 7 and 8 with equations (55) and (56) as

$$\gamma_{\mathrm{L_{1A}}} = \frac{\Delta i_{L_{1\mathrm{A}}}}{2I_{L_{1\mathrm{A}}}} =$$
$$\begin{cases} \dfrac{1}{4Lf_{\mathrm{s}}I_{L_{1\mathrm{A}}}}\left(P\dfrac{1-3D_1^{\mathrm{d}}}{2}-Q\dfrac{D_1^{\mathrm{d}}(2D_2^{\mathrm{d}}-1)}{1-D_1^{\mathrm{d}}}\right) & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in A1\cup A2 \\ \dfrac{1}{4Lf_{\mathrm{s}}I_{L_{1\mathrm{A}}}}\left(P\dfrac{1-3D_1^{\mathrm{d}}}{2}-Q\dfrac{D_2^{\mathrm{d}}(2D_1^{\mathrm{d}}-1)}{1-D_1^{\mathrm{d}}}\right) & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in B1\_1\cup B1\_2 \\ \dfrac{P(1-3D_1^{\mathrm{d}})}{8Lf_{\mathrm{s}}I_{L_{1\mathrm{A}}}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in C4\_1\cup C5\_1 \\ \dfrac{PD_1^{\mathrm{d}}(1-D_1^{\mathrm{d}})}{4Lf_{\mathrm{s}}I_{L_{1\mathrm{A}}}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in others. \end{cases} \tag{57}$$

$$\gamma_{\mathrm{L_{1B}}} = \frac{\Delta i_{L_{1\mathrm{B}}}}{2I_{L_{1\mathrm{B}}}} =$$
$$\begin{cases} \dfrac{P(1-D_1^{\mathrm{d}})}{8Lf_{\mathrm{s}}I_{L_{1\mathrm{B}}}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in A\cup B1\cup C4\cup C5 \\ \dfrac{PD_1^{\mathrm{d}}(1-D_1^{\mathrm{d}})}{4Lf_{\mathrm{s}}I_{L_{1\mathrm{B}}}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in others. \end{cases} \tag{58}$$

$$\gamma_{\mathrm{L_{2A}}} = \frac{\Delta i_{L_{2\mathrm{A}}}}{2I_{L_{2\mathrm{A}}}} =$$
$$\begin{cases} \dfrac{Q(1-3D_2^{\mathrm{d}})}{8Lf_{\mathrm{s}}I_{L_{2\mathrm{A}}}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in A1\cup B1\_1\cup B1\_4\cup B2\_1\cup C1\_1 \\ \dfrac{QD_2^{\mathrm{d}}(1-D_2^{\mathrm{d}})}{4Lf_{\mathrm{s}}I_{L_{2\mathrm{A}}}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in others. \end{cases} \tag{59}$$

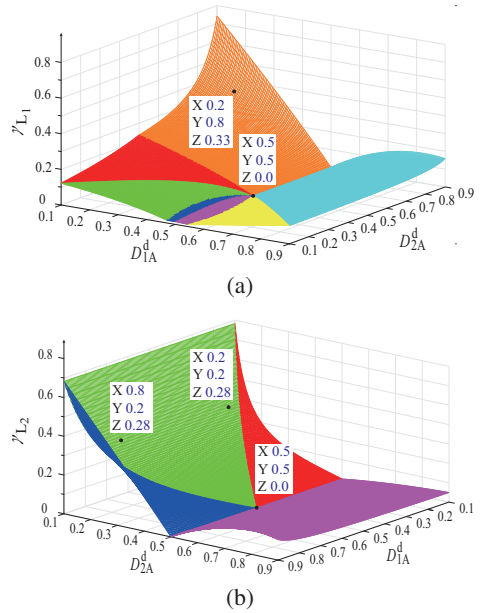
$$\gamma_{\mathrm{L_{2B}}} = \frac{\Delta i_{L_{2\mathrm{B}}}}{2I_{L_{2\mathrm{B}}}} =$$
$$\begin{cases} \dfrac{Q(1-D_2^{\mathrm{d}})}{8Lf_{\mathrm{s}}I_{L_{2\mathrm{B}}}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in A\cup B\cup C1 \\ \dfrac{QD_2^{\mathrm{d}}(1-D_2^{\mathrm{d}})}{4Lf_{\mathrm{s}}I_{L_{2\mathrm{B}}}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in others. \end{cases} \tag{60}$$

The ripple current at each low-voltage side port can be represented on the basis of the waveforms in Figs. 7 and 8 with equation (10) as

$$\gamma_{\mathrm{L_1}} = \frac{\Delta i_{L_1}}{2I_{L_1}} =$$
$$\begin{cases} \dfrac{P(1-D_1^{\mathrm{d}})(1-2D_1^{\mathrm{d}})+QD_1^{\mathrm{d}}(1-2D_2^{\mathrm{d}})}{4Lf_{\mathrm{s}}(1-D_1^{\mathrm{d}})I_{L_1}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in A \\ \dfrac{P(1-D_1^{\mathrm{d}})(1-2D_1^{\mathrm{d}})+Q(1-2D_1^{\mathrm{d}})D_2^{\mathrm{d}}}{2Lf_{\mathrm{s}}(1-D_1^{\mathrm{d}})I_{L_1}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in B1\_1\cup B1\_2\cup B1\_3a\cup B1\_4a \\ \dfrac{QD_2^{\mathrm{d}}(1-2D_2^{\mathrm{d}})}{2Lf_{\mathrm{s}}I_{L_1}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in B1\_3b\cup B1\_4b \\ \dfrac{P(1-D_1^{\mathrm{d}})(1-2D_1^{\mathrm{d}})D_2^{\mathrm{d}}+2Q(1-D_1^{\mathrm{d}}-D_2^{\mathrm{d}})D_2^{\mathrm{d}}}{4Lf_{\mathrm{s}}(1-D_1^{\mathrm{d}})I_{L_1}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in B2\_1a\cup B2\_2a \\ \dfrac{P(1-D_1^{\mathrm{d}})(2D_1^{\mathrm{d}}-1)}{4Lf_{\mathrm{s}}I_{L_1}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in B2\_1b\cup B2\_2b\cup C1\cup C2\cup C3 \\ \dfrac{P(1-2D_1^{\mathrm{d}})}{4Lf_{\mathrm{s}}I_{L_1}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in others. \end{cases} \tag{61}$$

$$\gamma_{\mathrm{L_2}} = \frac{\Delta i_{L_2}}{2I_{L_2}} =$$
$$\begin{cases} \dfrac{Q(1-2D_2^{\mathrm{d}})}{4Lf_{\mathrm{s}}I_{L_2}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in A\cup B\cup C1 \\ \dfrac{Q(1-D_2^{\mathrm{d}})(2D_2^{\mathrm{d}}-1)}{4Lf_{\mathrm{s}}I_{L_2}} & \text{when } (D_1^{\mathrm{d}},D_2^{\mathrm{d}})\in others. \end{cases} \tag{62}$$

The characteristics of current ripple rates in the low-voltage ports as functions of D_1^{d} and D_2^{d} are depicted in Figs. 15(a) and (b) with the following numerical example of parameters: $L_{1\mathrm{A}} = L_{1\mathrm{B}} = L_{2\mathrm{A}} = L_{2\mathrm{B}} = 174\,\mu\mathrm{H}$, switching frequency $f_{\mathrm{s}} = 50\,\mathrm{kHz}$, $V_{\mathrm{Low1}} = 72\,\mathrm{V}$, and $V_{\mathrm{Low2}} = 48\,\mathrm{V}$. In boost mode, the output voltage is maintained between $400\,\mathrm{V}$ and $800\,\mathrm{V}$ and the output power is fixed at $2.5\,\mathrm{kW}$. For $\gamma_{\mathrm{L_1}}$, as D_1^{d} increases, the current ripple firstly decreases and then shows a rising trend, whereas increasing D_2^{d} results in an upward trend in ripple current. Moreover, the peak ripple



(a)

(b)

Fig. 15. Total inductor current ripple rates of low-voltage ports versus duty cycles in a boost mode: (a) γ_{L_1}, and (b) γ_{L_2}.

current occurs in zones $C4$ and $C5$. In the case of inductor γ_{L_2}, the ripple current is primarily affected by D_2^{d}, increasing as D_2^{d} decreases. In general, the duty cycle of a buck/boost converter ranges between 0.2 and 0.8, where the ripple currents of both γ_{L_1} and γ_{L_2} stay below 0.35. Additionally, when the converter operates at (0.5, 0.5), zero ripple current can theoretically be attained for both γ_{L_1} and γ_{L_2}. It is worth noting that the inductor current ripple rate is not only affected by the duty cycle but also by the inductance value, switching frequency and load resistance. To ensure the circuit operates in CCM, these parameters must be meticulously chosen according to the specific application requirements.

2) Buck Mode: By combining (13) - (19), the DC components of the current through $L_{1\mathrm{A}}$, $L_{1\mathrm{B}}$, $L_{2\mathrm{A}}$ and $L_{2\mathrm{B}}$ can be theoretically represented by (63) and (64), respectively.

$$I_{L_{1\mathrm{A}}} = I_{L_{1\mathrm{B}}} = 0.5 I_{L_1} =$$

$$\begin{cases} \dfrac{V_{\mathrm{High}} D_1^{\mathrm{c}} \left(D_2^{\mathrm{c}}\right)^2}{4\left(R_{\mathrm{Low1}} \left(D_2^{\mathrm{c}}\right)^2 + R_{\mathrm{Low2}} \left(D_1^{\mathrm{c}}\right)^2\right)} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in L \\ \dfrac{V_{\mathrm{High}} D_1^{\mathrm{c}} \left(D_2^{\mathrm{c}}\right)^2}{4\left(R_{\mathrm{Low1}} \left(D_2^{\mathrm{c}}\right)^2 + R_{\mathrm{Low2}} \left(1 - D_2^{\mathrm{c}}\right)^2\right)} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in M \\ \dfrac{V_{\mathrm{High}} D_1^{\mathrm{c}} \left(D_2^{\mathrm{c}}\right)^2}{4\left(R_{\mathrm{Low1}} \left(D_2^{\mathrm{c}}\right)^2 + R_{\mathrm{Low2}} \left(1 + D_1^{\mathrm{c}} - 2D_2^{\mathrm{c}}\right)^2\right)} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in N. \end{cases} \tag{63}$$

$$I_{L_{2\mathrm{A}}} = I_{L_{2\mathrm{B}}} = 0.5 I_{L_2} =$$

$$\begin{cases} \dfrac{V_{\mathrm{High}} \left(D_1^{\mathrm{c}}\right)^2 D_2^{\mathrm{c}}}{4\left(R_{\mathrm{Low1}} \left(D_2^{\mathrm{c}}\right)^2 + R_{\mathrm{Low2}} \left(D_1^{\mathrm{c}}\right)^2\right)} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in L \end{cases} \tag{64a}$$

$$\begin{cases} \dfrac{V_{\mathrm{High}} D_1^{\mathrm{c}} D_2^{\mathrm{c}} (1 - D_2^{\mathrm{c}})}{4\left(R_{\mathrm{Low1}} \left(D_2^{\mathrm{c}}\right)^2 + R_{\mathrm{Low2}} \left(1 - D_2^{\mathrm{c}}\right)^2\right)} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in M \\ \dfrac{V_{\mathrm{High}} D_1^{\mathrm{c}} D_2^{\mathrm{c}} \left(1 + D_1^{\mathrm{c}} - 2D_2^{\mathrm{c}}\right)}{4\left(R_{\mathrm{Low1}} \left(D_2^{\mathrm{c}}\right)^2 + R_{\mathrm{Low2}} \left(1 + D_1^{\mathrm{c}} - 2D_2^{\mathrm{c}}\right)^2\right)} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in N. \end{cases} \tag{64b}$$

In a similar manner, the ripple current in each inductor can be calculated by incorporating equations (63) and (64) as

$$\gamma_{L_{1\mathrm{A}}} = \frac{\Delta i_{L_{1\mathrm{A}}}}{2 I_{L_{1\mathrm{A}}}} =$$

$$\begin{cases} \dfrac{S_{\mathrm{L}} D_1^{\mathrm{c}} (1 - D_1^{\mathrm{c}})}{4 L f_{\mathrm{s}} I_{L_{1\mathrm{A}}}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in L1 \cup L2 \cup L3 \cup L4\_2 \cup L5\_2 \\ \dfrac{S_{\mathrm{L}} (3D_1^{\mathrm{c}} - 2)}{8 L f_{\mathrm{s}} I_{L_{1\mathrm{A}}}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in L4\_1 \cup L5\_1 \\ \dfrac{1}{4 L f_{\mathrm{s}} I_{L_{1\mathrm{A}}}} \left(S_{\mathrm{M}} \dfrac{3D_1^{\mathrm{c}} - 2}{2} - T_{\mathrm{M}} \dfrac{(1 - 2D_1^{\mathrm{c}})(1 - D_2^{\mathrm{c}})}{D_1^{\mathrm{c}}}\right) & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in M1\_1 \cup M1\_2 \\ \dfrac{S_{\mathrm{M}} D_1^{\mathrm{c}} (1 - D_1^{\mathrm{c}})}{4 L f_{\mathrm{s}} I_{L_{1\mathrm{A}}}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in M1\_3 \cup M1\_4 \cup M2 \\ \dfrac{1}{4 L f_{\mathrm{s}} I_{L_{1\mathrm{A}}}} \left(S_{\mathrm{N}} \dfrac{3D_1^{\mathrm{c}} - 2}{2} - T_{\mathrm{N}} \dfrac{(1 - D_1^{\mathrm{c}})(1 - 2D_2^{\mathrm{c}})}{D_1^{\mathrm{c}}}\right) & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in N1 \cup N2 \\ \dfrac{S_{\mathrm{N}} D_1^{\mathrm{c}} (1 - D_1^{\mathrm{c}})}{4 L f_{\mathrm{s}} I_{L_{1\mathrm{A}}}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in N3. \end{cases} \tag{65}$$

$$\gamma_{L_{1\mathrm{B}}} = \frac{\Delta i_{L_{1\mathrm{B}}}}{2 I_{L_{1\mathrm{B}}}} =$$

$$\begin{cases} \dfrac{S_{\mathrm{L}} D_1^{\mathrm{c}} (1 - D_1^{\mathrm{c}})}{4 L f_{\mathrm{s}} I_{L_{1\mathrm{B}}}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in L1 \cup L2 \cup L3 \\ \dfrac{S_{\mathrm{L}} D_1^{\mathrm{c}}}{8 L f_{\mathrm{s}} I_{L_{1\mathrm{B}}}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in L4 \cup L5 \\ \dfrac{S_{\mathrm{M}} D_1^{\mathrm{c}}}{8 L f_{\mathrm{s}} I_{L_{1\mathrm{B}}}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in M1 \\ \dfrac{S_{\mathrm{M}} D_1^{\mathrm{c}} (1 - D_1^{\mathrm{c}})}{4 L f_{\mathrm{s}} I_{L_{1\mathrm{B}}}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in M2 \\ \dfrac{S_{\mathrm{N}} D_1^{\mathrm{c}}}{8 L f_{\mathrm{s}} I_{L_{1\mathrm{B}}}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in N. \end{cases} \tag{66}$$

$$\gamma_{L_{2\mathrm{A}}} = \frac{\Delta i_{L_{2\mathrm{A}}}}{2 I_{L_{2\mathrm{A}}}} =$$

$$\begin{cases} \dfrac{T_{\mathrm{L}} (3D_2^{\mathrm{c}} - 2)}{8 L f_{\mathrm{s}} I_{L_{2\mathrm{A}}}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in L1\_1 \\ \dfrac{T_{\mathrm{L}} D_2^{\mathrm{c}} (1 - D_2^{\mathrm{c}})}{4 L f_{\mathrm{s}} I_{L_{2\mathrm{A}}}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in L1\_2 \cup L2 \cup L3 \cup L4 \cup L5 \\ \dfrac{T_{\mathrm{M}} (3D_2^{\mathrm{c}} - 2)}{8 L f_{\mathrm{s}} I_{L_{2\mathrm{A}}}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in M1\_1 \cup M1\_4 \cup M2\_1 \end{cases} \tag{67a}$$

$$\begin{cases} \dfrac{T_{\mathrm{M}} D_2^{\mathrm{c}}(1-D_2^{\mathrm{c}})}{4Lf_{\mathrm{s}}I_{L_{2\mathrm{A}}}} \\ \qquad \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in M1\_2 \cup M1\_3 \cup M2\_2 \\ \dfrac{T_{\mathrm{N}}(3D_2^{\mathrm{c}}-2)}{8Lf_{\mathrm{s}}I_{L_{2\mathrm{A}}}} \qquad \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in N1 \\ \dfrac{T_{\mathrm{N}} D_2^{\mathrm{c}}(1-D_2^{\mathrm{c}})}{4Lf_{\mathrm{s}}I_{L_{2\mathrm{A}}}} \qquad \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in others. \end{cases} \tag{67b}$$

$$\gamma_{L_{2\mathrm{B}}} = \frac{\Delta i_{L_{2\mathrm{B}}}}{2I_{L_{2\mathrm{B}}}} = \begin{cases} \dfrac{T_{\mathrm{L}} D_2^{\mathrm{c}}}{8Lf_{\mathrm{s}}I_{L_{2\mathrm{B}}}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in L1 \\ \dfrac{T_{\mathrm{M}} D_2^{\mathrm{c}}}{8Lf_{\mathrm{s}}I_{L_{2\mathrm{B}}}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in M \\ \dfrac{T_{\mathrm{N}} D_2^{\mathrm{c}}}{8Lf_{\mathrm{s}}I_{L_{2\mathrm{B}}}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in N \\ \dfrac{T_{\mathrm{L}} D_2^{\mathrm{c}}(1-D_2^{\mathrm{c}})}{4Lf_{\mathrm{s}}I_{L_{2\mathrm{B}}}} & \\ & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in others. \end{cases} \tag{68}$$

Utilizing equation (19), the ripple current at each low-voltage side port can be determined as

$$\gamma_{\mathrm{L}_1} = \frac{\Delta i_{L_1}}{2I_{L_1}} =$$

$$\begin{cases} \dfrac{S_{\mathrm{L}} D_1^{\mathrm{c}}(1-2D_1^{\mathrm{c}})}{4Lf_{\mathrm{s}}I_{L_1}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in L1 \cup L2 \cup L3 \\ \dfrac{S_{\mathrm{L}}(2D_1^{\mathrm{c}}-1)}{4Lf_{\mathrm{s}}I_{L_1}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in L4 \cup L5 \\ \max\left(\dfrac{S_{\mathrm{M}} D_1^{\mathrm{c}}(2D_1^{\mathrm{c}}-1) + T_{\mathrm{M}}(2D_1^{\mathrm{c}}-1)(1-D_2^{\mathrm{c}})}{4Lf_{\mathrm{s}}D_1^{\mathrm{c}}I_{L_1}}, \right. & \\ \qquad \left. \dfrac{T_{\mathrm{M}}(1-D_2^{\mathrm{c}})(2D_2^{\mathrm{c}}-1)}{2Lf_{\mathrm{s}}I_{L_1}} \right) & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in M1 \\ \max\left(\dfrac{(1-D_2^{\mathrm{c}})(S_{\mathrm{M}} D_1^{\mathrm{c}}(2D_1^{\mathrm{c}}-1) + 2T_{\mathrm{M}}(D_1^{\mathrm{c}}+D_2^{\mathrm{c}}-1))}{4Lf_{\mathrm{s}}D_1^{\mathrm{c}}I_{L_1}}, \right. & \\ \qquad \left. \dfrac{S_{\mathrm{M}} D_1^{\mathrm{c}}(1-2D_1^{\mathrm{c}})}{4Lf_{\mathrm{s}}I_{L_1}} \right) & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in M2 \\ \dfrac{S_{\mathrm{N}} D_1^{\mathrm{c}}(2D_1^{\mathrm{c}}-1) + T_{\mathrm{N}}(1-D_1^{\mathrm{c}})(2D_2^{\mathrm{c}}-1)}{4Lf_{\mathrm{s}}D_1^{\mathrm{c}}I_{L_1}} & \\ & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in N. \end{cases} \tag{69}$$

$$\gamma_{\mathrm{L}_2} = \frac{\Delta i_{L_2}}{2I_{L_2}} = \begin{cases} \dfrac{T_{\mathrm{L}}(2D_2^{\mathrm{c}}-1)}{4Lf_{\mathrm{s}}I_{L_2}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in L1 \\ \dfrac{T_{\mathrm{M}}(2D_2^{\mathrm{c}}-1)}{4Lf_{\mathrm{s}}I_{L_2}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in M \\ \dfrac{T_{\mathrm{N}}(2D_2^{\mathrm{c}}-1)}{4Lf_{\mathrm{s}}I_{L_2}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in N \\ \dfrac{T_{\mathrm{L}} D_2^{\mathrm{c}}(1-2D_2^{\mathrm{c}})}{4Lf_{\mathrm{s}}I_{L_2}} & \text{when } (D_1^{\mathrm{c}}, D_2^{\mathrm{c}}) \in others. \end{cases} \tag{70}$$

The behavior of current ripple rates in γ_{L_1} and γ_{L_2} with respect to D_1^{c} and D_2^{c} are illustrated in Figs. 16(a) and (b), using the same conditions of inductance and switching frequency as described for the boost mode. In this case, the input voltage is fixed at $400\,\mathrm{V}$, and the low-voltage port 1 is stabilized at $1.5\,\mathrm{kW}$. Additionally, the load on low-voltage

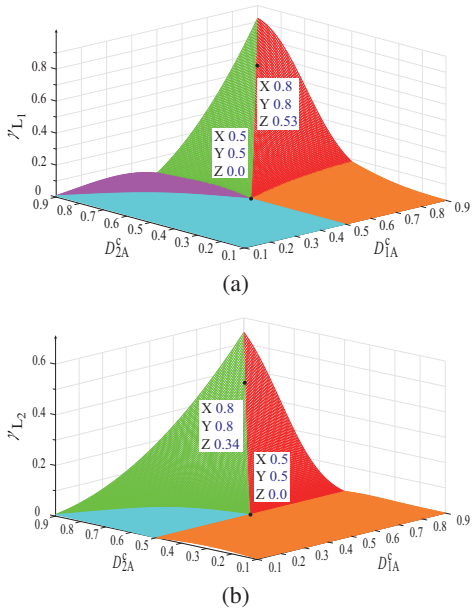


Fig. 16. Total inductor current ripple rates of low-voltage ports versus duty cycles in a buck mode with $R_{\mathrm{Low1}} = 1.5R_{\mathrm{Low2}}$: (a) γ_{L_1}, and (b) γ_{L_2}.

port 1 is maintained at 1.5 times that of low-voltage port 2. In regions M and N, for γ_{L_1}, as either D_1^{c} or D_2^{c} increases, the current ripple exhibits an upward trend. Similarly, for inductor γ_{L_2}, the ripple current follows a comparable pattern. Moreover, in region L, both γ_{L_1} and γ_{L_2} can achieve extremely low ripple current levels. Zero ripple current can also be achieved theoretically when the converter operates at (0.5, 0.5) . It should be remarked here that the inductor current ripple rate is influenced not only by the duty cycle but also by parameters such as inductance, switching frequency, and load resistance.

IV. Design Procedure in Main Circuit

In order to validate the theoretical analysis and assess the performance of the proposed MP-BDC, a 2.5 kW experimental prototype is developed. The prototype operates with low-side voltages of 72 V/48 V, a high-side voltage range of 400 V to 800 V, a switching frequency of 50 kHz, and duty cycles varying between 0.25 and 0.75. The detailed design process is presented in the following sections.

A. Selection of Low-Voltage Module Numbers

Fig. 17 depicts the relationship between the voltage conversion ratio and duty cycle for both the MP-BDC and single module topology (Fig. 3(a)) operating in the boost mode. The low-voltage-side ports are assumed to have the same input voltage. It is evident that the MP-BDC significantly improves the achievable voltage conversion ratio. The duty cycle of a buck/boost converter typically ranges from 0.2 to 0.8, while occasionally between 0.3 and 0.7 [46]. Considering the inductor current ripple in the boost mode as shown in Fig. 15, it is practical to maintain the duty cycle between 0.25 and 0.75 to ensure that the inductor current remains in CCM while providing adequate design margin. When the duty cycle reaches 0.75, the voltage conversion ratio for the single module topology is 8, while for the MP-BDC, it

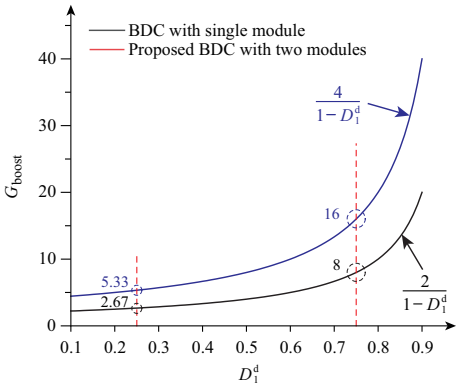


Fig. 17. Voltage conversion ratios versus duty cycle in the boost mode.

increases to 16. To achieve the desired voltage conversion from 72 V/48 V (equivalent to 60 V) to 400 V-800 V, a voltage conversion ratio exceeding 13.3 is required. In addition, a higher voltage conversion ratio is essential to sustain an 800 V output, particularly considering the impact of load effects. It is obvious from the viewpoints of voltage ratio that the MP-BDC is more suitable for the wide range of voltage ratio. In addition, compared to the single module topology, the MP-BDC offers the advantage of doubling the power rating and enabling the integration of multiple ESS units, enhancing overall system flexibility and scalability.

B. Selection of Active Switches

When the low-side voltages are 72 V/48 V and the high-side voltage varies between 400 V and 800 V, the maximum voltage stress on the active switches in boost mode is 480 V. This result is derived from (32) and (42) - (47), considering that the duty cycle adjusts dynamically along the paths of L_{a} and L_{c}. Similarly, in buck mode, based on (39), (40), and (49) - (54), the maximum voltage stress on the active switches along the paths of M_{l} and M_{n} is also 480 V. Furthermore, it can be observed from the waveforms in Figs. 7 - 9 that the maximum current flowing through the active switches equals the total current passing through the four inductors. Therefore, the active switch should meet the following requirements as denoted by

$$\begin{cases} v_{\text{ds}} > 576V \\ i_{\text{ds}} > (1+\gamma_{L_1})I_{L_1} + (1+\gamma_{L_2})I_{L_2}. \end{cases} \tag{71}$$

In order to ensure a voltage margin of over 20%, the rated voltage of 650 V and more are considered suitable for the active switches in the proposed MP-BDC. In particular, 650 V power MOSFETs are regarded as the optimal choice due to their low ON-resistance and reduced gate charge capacitance. When the low-voltage port operates at equal current, a continuous DC drain current of over 42 A is required.

C. Design of Inductors

By applying (57) - (60), the inductance values of $L_{1\text{A}}$, $L_{1\text{B}}$, $L_{2\text{A}}$ and $L_{2\text{B}}$ can be obtained using the following equations:

$$L_{1\text{A}} = \begin{cases} \dfrac{1}{4f_{\text{s}}\gamma_{L_{1\text{A}}}I_{L_{1\text{A}}}}\left(P\dfrac{1-3D_1^{\text{d}}}{2} - Q\dfrac{D_1^{\text{d}}(2D_2^{\text{d}}-1)}{1-D_1^{\text{d}}}\right) & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in A1 \cup A2 \\ \dfrac{1}{4f_{\text{s}}\gamma_{L_{1\text{A}}}I_{L_{1\text{A}}}}\left(P\dfrac{1-3D_1^{\text{d}}}{2} - Q\dfrac{D_2^{\text{d}}(2D_1^{\text{d}}-1)}{1-D_1^{\text{d}}}\right) & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in B1\_1 \cup B1\_2 \\ \dfrac{P(1-3D_1^{\text{d}})}{8f_{\text{s}}\gamma_{L_{1\text{A}}}I_{L_{1\text{A}}}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in C4\_1 \cup C5\_1 \\ \dfrac{PD_1^{\text{d}}(1-D_1^{\text{d}})}{4f_{\text{s}}\gamma_{L_{1\text{A}}}I_{L_{1\text{A}}}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in others. \end{cases} \tag{72}$$

$$L_{1\text{B}} = \begin{cases} \dfrac{P(1-D_1^{\text{d}})}{8f_{\text{s}}\gamma_{L_{1\text{B}}}I_{L_{1\text{B}}}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in A \cup B1 \cup C4 \cup C5 \\ \dfrac{PD_1^{\text{d}}(1-D_1^{\text{d}})}{4f_{\text{s}}\gamma_{L_{1\text{B}}}I_{L_{1\text{B}}}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in others. \end{cases} \tag{73}$$

$$L_{2\text{A}} = \begin{cases} \dfrac{Q(1-3D_2^{\text{d}})}{8f_{\text{s}}\gamma_{L_{2\text{A}}}I_{L_{2\text{A}}}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in A1 \cup B1\_1 \cup B1\_4 \cup B2\_1 \cup C1\_1 \\ \dfrac{QD_2^{\text{d}}(1-D_2^{\text{d}})}{4f_{\text{s}}\gamma_{L_{2\text{A}}}I_{L_{2\text{A}}}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in others. \end{cases} \tag{74}$$

$$L_{2\text{B}} = \begin{cases} \dfrac{Q(1-D_2^{\text{d}})}{8f_{\text{s}}\gamma_{L_{2\text{B}}}I_{L_{2\text{B}}}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in A \cup B \cup C1 \\ \dfrac{QD_2^{\text{d}}(1-D_2^{\text{d}})}{4f_{\text{s}}\gamma_{L_{2\text{B}}}I_{L_{2\text{B}}}} & \text{when } (D_1^{\text{d}}, D_2^{\text{d}}) \in others. \end{cases} \tag{75}$$

In order to ensure that the inductor currents operate in CCM, the values of $\gamma_{L_{1\text{A}}}$, $\gamma_{L_{1\text{B}}}$, $\gamma_{L_{2\text{A}}}$ and $\gamma_{L_{2\text{B}}}$ must be less than 1. In addition, the selected inductors should be able to accommodate the maximum current according to the following requirements.

$$\begin{cases} i_{L_{1\text{A}}} > (1+\gamma_{L_{1\text{A}}})I_{L_{1\text{A}}} \\ i_{L_{1\text{B}}} > (1+\gamma_{L_{1\text{B}}})I_{L_{1\text{B}}} \\ i_{L_{2\text{A}}} > (1+\gamma_{L_{2\text{A}}})I_{L_{2\text{A}}} \\ i_{L_{2\text{B}}} > (1+\gamma_{L_{2\text{B}}})I_{L_{2\text{B}}}. \end{cases} \tag{76}$$

When the ripple current ratio is set to below 0.3, the inductor values are determined based on (72) - (76) as follows: $L_{1\text{A}} \geq 172.74\,\mu\text{H}$, $L_{1\text{B}} \geq 172.74\,\mu\text{H}$, $L_{2\text{A}} \geq 115.16\,\mu\text{H}$ and $L_{2\text{B}} \geq 115.16\,\mu\text{F}$. For the implementation of the proposed converter, the chosen inductor values are $L_{1\text{A}} = 174\,\mu\text{H}$, $L_{1\text{B}} = 174\,\mu\text{H}$, $L_{2\text{A}} = 174\,\mu\text{H}$ and $L_{2\text{B}} = 174\,\mu\text{F}$. On top of that, the inductors must support a current rating of over 13.55A.

D. Design of Capacitors

The maximum charge increment stored in C_{Low1} and C_{Low2} during one cycle in boost mode are, respectively, as

$$\Delta W_{L_1} = \frac{\Delta I_{L_1}}{8f_{\text{s}}} = \frac{\gamma_{L_1} I_{L_1}}{4f_{\text{s}}} \tag{77}$$

$$\Delta W_{L_2} = \frac{\Delta I_{L_2}}{8 f_{\rm s}} = \frac{\gamma_{L_2} I_{L_2}}{4 f_{\rm s}}. \tag{78}$$

Therefore, the minimum capacitance value of $C_{\rm Low1}$ and $C_{\rm Low2}$ can be determined as

$$C_{\rm Low1} = \frac{\gamma_{L_1} I_{L_1}}{4 \Delta V_{C_{\rm Low1}} f_{\rm s}} \tag{79}$$

$$C_{\rm Low2} = \frac{\gamma_{L_2} I_{L_2}}{4 \Delta V_{C_{\rm Low2}} f_{\rm s}}. \tag{80}$$

The switched capacitors $C_{\rm 1B}$, $C_{\rm 2A}$ and $C_{\rm 2B}$ can also be calculated as

$$C_{\rm 1B} \geq \frac{I_{L_{\rm 1A}}}{2 \Delta V_{C_{\rm 1B}} f_{\rm s}} \tag{81}$$

$$C_{\rm 2A} \geq \frac{(1 - D_2^{\rm d}) I_{L_{\rm 2A}}}{\Delta V_{C_{\rm 2A}} f_{\rm s}} \tag{82}$$

$$C_{\rm 2B} \geq \frac{I_{L_{\rm 2A}}}{2 \Delta V_{C_{\rm 2B}} f_{\rm s}}. \tag{83}$$

By the same token, the filter capacitors of high-voltage side $C_{\rm High}$ can be expressed as

$$C_{\rm High} \geq \max\left(\frac{I_{\rm High}}{2 \Delta V_{C_{\rm High}} f_{\rm s}}, \frac{D_2^{\rm d} I_{\rm High}}{\Delta V_{C_{\rm High}} f_{\rm s}} \right). \tag{84}$$

The voltage ripple percentages for the switched capacitors, high-side capacitor, and low-side capacitors are set at 3%, 1%, and 1%, respectively. Based on (79) - (84), the required capacitor values are calculated as: $C_{\rm Low1} \geq 28.93\,\mu$F, $C_{\rm Low2} \geq 43.39\,\mu$F, $C_{\rm 1B} \geq 39.46\,\mu$F, $C_{\rm 2A} \geq 23.68\,\mu$F, $C_{\rm 2B} \geq 10.53\,\mu$F and $C_{\rm High} \geq 23.44\,\mu$F. The actual capacitance values for the proposed MP-BDC are selected as $C_{\rm Low1} = 82\,\mu$F, $C_{\rm Low2} = 100\,\mu$F, $C_{\rm 1B} = 50\,\mu$F, $C_{\rm 2A} = 40\,\mu$F, $C_{\rm 2B} = 30\,\mu$F and $C_{\rm High} = 40\,\mu$F.

E. Implementation of ZVS

As illustrated in Figs. 8 and 9, within zones $C2$ and $C3$, achieving successful ZVS during turn-on and turn-off transitions of the SR switches in boost mode requires that the energy stored in the DC inductors ($L_{\rm 1A}$, $L_{\rm 1B}$, $L_{\rm 2A}$, and $L_{\rm 2B}$) be sufficient to completely discharge the output capacitances ($C_{\rm oss}$) of switches $\rm Q_{1A}^c$, $\rm Q_{1B}^c$, $\rm Q_{2A}^c$, and $\rm Q_{2B}^c$, while simultaneously charging their complementary counterparts during commutation. These conditions are expressed as

$$\begin{cases} L_{\rm 1A}(i_{L_{\rm 1A}})^2 > C_{\rm oss}(V_{\rm Q_{1A,ds}^d})^2 + C_{\rm oss}(V_{\rm Q_{1A,ds}^c})^2 \\ L_{\rm 1B}(i_{L_{\rm 1B}})^2 > C_{\rm oss}(V_{\rm Q_{1B,ds}^d})^2 + C_{\rm oss}(V_{\rm Q_{1B,ds}^c})^2 \\ L_{\rm 2A}(i_{L_{\rm 2A}})^2 > C_{\rm oss}(V_{\rm Q_{2A,ds}^d})^2 + C_{\rm oss}(V_{\rm Q_{2A,ds}^c})^2 \\ L_{\rm 2B}(i_{L_{\rm 2B}})^2 > C_{\rm oss}(V_{\rm Q_{2B,ds}^d})^2 + C_{\rm oss}(V_{\rm Q_{2B,ds}^c})^2. \end{cases} \tag{85}$$

where $C_{\rm oss}$ represents the output capacitance of the power MOSFETs. When the converter operates along the trajectory defined by L_c, the critical load conditions on the high-voltage side for switches $\rm Q_{1A}^c$, $\rm Q_{1B}^c$, $\rm Q_{2A}^c$ and $\rm Q_{2B}^c$ can be derived by combining (23), (24), (29) - (31), and (55) - (60). These conditions are expressed as follows:

For $\rm Q_{1A}^c$ and $\rm Q_{1B}^c$:

$$\left[4(1 - D^{\rm d}) \sqrt{\frac{C_{\rm oss}}{2L}} + \frac{D^{\rm d}(1 - D^{\rm d})^2}{Lf} \right] R_{\rm High} = 4(1 + k). \tag{86}$$

and for $\rm Q_{2A}^c$ and $\rm Q_{2B}^c$:

$$\left[4(1 - D^{\rm d}) \sqrt{\frac{C_{\rm oss}}{2L}} + \frac{D^{\rm d}(1 - D^{\rm d})^2}{Lf} \right] R_{\rm High} = \frac{4(1 + k)}{k}. \tag{87}$$

Due to $0 < k < 1$, (86) must be satisfied to ensure ZVS operation for all the SR switches. Furthermore, the implementation of ZVS in other regions can be analyzed using the same methodology.

Similarly, within zones $L2$ and $L3$, where the converter operates along the path defined by M_l in the buck mode, the essential load conditions for achieving ZVS on both low-voltage sides, involving switches $\rm Q_{1A}^d$, $\rm Q_{1B}^d$, $\rm Q_{2A}^d$ and $\rm Q_{2B}^d$, can be determined by synthesizing (63) - (68), and TABLE I. The derived conditions are outlined as follows:

For switches $\rm Q_{1A}^d$ and $\rm Q_{1B}^d$:

$$\begin{cases} \left[4\sqrt{\frac{C_{\rm oss}}{2L}} + \frac{D^{\rm c}(1 - D^{\rm c})}{Lf} \right] R_{\rm Low1} = D^{\rm c} \\ R_{\rm Low2} = k R_{\rm Low1}. \end{cases} \tag{88}$$

For switches $\rm Q_{2A}^d$ and $\rm Q_{2B}^d$:

$$\begin{cases} \left[4\sqrt{\frac{C_{\rm oss}}{2L}} + \frac{D^{\rm c}(1 - D^{\rm c})}{Lf} \right] R_{\rm Low1} = \frac{D^{\rm c}}{k} \\ R_{\rm Low2} = k R_{\rm Low1}. \end{cases} \tag{89}$$

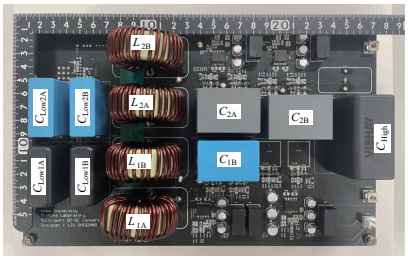
When $0 < k < 1$, the condition (88) must be fulfilled to guarantee ZVS operation across all SR switches. The same analytical approach can be applied to evaluate ZVS performance in other regions.

V. Experimental Verifications

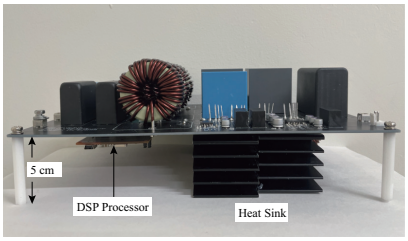
The performances of the MP-BDC are investigated by the experiment of 2.5 kW-50 kHz prototype. The exterior appearance of the prototype is portrayed in Fig. 18, and the specifications are listed in TABLE II. The active switches are implemented with SiC-MOSFETs (IMZA65R027M, 650 V, 59 A, 27 mΩ, 244 pF, Infineon), all of which are driven by isolated gate drivers (UCC21520A,Texas Instruments). The power controller is comprised by a DSP board development kit (LAUNCHXL-F28379D, Texas Instruments).

A. Steady-State Performances in the Boost Mode

1) 72V/48V to 400V: Fig. 19 displays the essential experimental waveforms in the boost mode, where the DC input voltages $V_{\rm Low1}$, $V_{\rm Low2}$ and the load resistance $R_{\rm High}$ are set to 72 V, 48 V and 64 Ω, respectively. As shown in Fig. 19(a), the main switches $\rm Q_{1A}^d$ and $\rm Q_{2A}^d$ are synchronized in a center-aligned configuration with identical phases. Switches $\rm Q_{1B}^d$ and $\rm Q_{2B}^d$ are driven with a phase shift of 180 ° relative to $\rm Q_{1A}^d$ and $\rm Q_{2A}^d$. The duty cycles of $\rm Q_{1B}^d$ and $\rm Q_{2B}^d$ are fixed at 0.5, whereas the duty cycles of $\rm Q_{1A}^d$ and $\rm Q_{2A}^d$ are adjusted to 0.42 and



(a)



(b)

Fig. 18. Exterior appearance of 2.5 kW - 50 kHz prototype: (a) top view, (b) side view.

TABLE II
SPECIFICATIONS OF THE MP-BDC CONVERTER

Item	Symbol	Value [unit]
High-side voltage	V_{High}	$400-800$ [V]
Low-side voltage 1	V_{Low1}	72 [V]
Low-side voltage 2	V_{Low2}	48 [V]
Output power rating	P_{o}	2.5 [kW]
Switching frequency	f_{s}	50 [kHz]
DC inductors	$L_{1\mathrm{A}}, L_{1\mathrm{B}}$, $L_{2\mathrm{A}}, L_{2\mathrm{B}}$	174 [μH]/20A
High-side capacitor	C_{High}	40 [μF]/900V
Low-side capacitor 1	$C_{\mathrm{Low1A}}, C_{\mathrm{Low1B}}$	82 [μF]/100V
Low-side capacitor 2	$C_{\mathrm{Low2A}}, C_{\mathrm{Low2B}}$	100 [μF]/63V
Switched capacitor	$C_{1\mathrm{B}}$	50 [μF]/450V
Switched capacitor	$C_{2\mathrm{A}}$	40 [μF]/600V
Switched capacitor	$C_{2\mathrm{B}}$	30 [μF]/800V
Power MOSFETs	$\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$–$\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}$	IMZA65R027M
DSP controller chip		TMS320F28379D
Voltage sampling chip		AMC1311BDWVR
Current sampling chip		CZ3A04

0.47, respectively. The current waveforms of the DC inductors are depicted in Fig. 19(b). The average currents through $L_{1\mathrm{A}}$, $L_{1\mathrm{B}}$, $L_{2\mathrm{A}}$, and $L_{2\mathrm{B}}$ are measured as $I_{L_{1\mathrm{A}}} = 10.59\,\mathrm{A}$, $I_{L_{1\mathrm{B}}} = 10.68\,\mathrm{A}$, $I_{L_{2\mathrm{A}}} = 10.57\,\mathrm{A}$, and $I_{L_{2\mathrm{B}}} = 10.64\,\mathrm{A}$, respectively, indicating a balanced average inductor current in each low-side port achieved by the proposed converter with the A-DLC2. The current ripples for $i_{L_{1\mathrm{A}}}$, $i_{L_{1\mathrm{B}}}$, $i_{L_{2\mathrm{A}}}$, and $i_{L_{2\mathrm{B}}}$ are $\Delta I_{L_{1\mathrm{A}}} = 3.52\,\mathrm{A}$, $\Delta I_{L_{1\mathrm{B}}} = 4.16\,\mathrm{A}$, $\Delta I_{L_{2\mathrm{A}}} = 2.87\,\mathrm{A}$, and $\Delta I_{L_{2\mathrm{B}}} = 3.04\,\mathrm{A}$. The current ripple rates for these inductors are found to be as 0.167, 0.195, 0.136, and 0.143, respectively, which corresponds well with the theoretical analyses in (57) - (60). Thus, the current ripple analysis for duty cycles in Zone A is actually verified herein. Fig. 19(c) demonstrates that the current ripple rates for i_{L_1} and i_{L_2} are further reduced to 0.074 and 0.031, respectively, due to the implementation of interleaved switching patterns and reduction of the size of filtering capacitors.

Fig. 19(d) shows the steady-state voltages across the switched capacitors, where the measured values are $V_{C_{1\mathrm{B}}} = 100.3\,\mathrm{V}$, $V_{C_{2\mathrm{A}}} = 229.3\,\mathrm{V}$ and $V_{C_{2\mathrm{B}}} = 311.5\,\mathrm{V}$, which align with (22). Additionally, the output voltage is recorded as $V_{\mathrm{High}} = 400.2\,\mathrm{V}$, thereby validating the expression in (32) is revealed. Fig. 19(e) illustrates the voltage stresses on switches $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$, $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}$, $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$, and $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$. The observed steady-state turn-off values are $V_{\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}} = 234.5\,\mathrm{V}$, $V_{\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}} = 413.7\,\mathrm{V}$, $V_{\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}} = 214.6\,\mathrm{V}$ and $V_{\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}} = 313.9\,\mathrm{V}$. It should be noted here that some voltage stresses are even less than half of V_{High}. Moreover, the black dashed circles in Fig. 19(f) highlight the successful ZVS turn-on and turn-off commutations of switches $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ under the condition of SR.

2) 72V/48V to 800V: Fig. 20 displays the essential experimental waveforms in a boost mode, where the DC input voltages V_{Low1} and V_{Low2} are set to 72 V and 48 V, respectively, with a load resistance R_{High} of 256 Ω. It can be observed in Fig. 20(a) that the main switches $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}$ are center-aligned with identical phases. Switches $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$ and $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}$ operate with a phase shift of 180 ° relative to $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}$. During this period, the A-DLC2 is inactive and the duty cycle for all the main switches is maintained at 0.72. The current waveforms of the inductors are shown in Fig. 20(b). The average currents for $L_{1\mathrm{A}}$, $L_{1\mathrm{B}}$, $L_{2\mathrm{A}}$, and $L_{2\mathrm{B}}$ are measured as $I_{L_{1\mathrm{A}}} = 10.51\,\mathrm{A}$, $I_{L_{1\mathrm{B}}} = 10.54\,\mathrm{A}$, $I_{L_{2\mathrm{A}}} = 10.62\,\mathrm{A}$, and $I_{L_{2\mathrm{B}}} = 10.58\,\mathrm{A}$, demonstrating well-balanced average inductor currents in the proposed BDC. The current ripples for $i_{L_{1\mathrm{A}}}$, $i_{L_{1\mathrm{B}}}$, $i_{L_{2\mathrm{A}}}$, and $i_{L_{2\mathrm{B}}}$ are $\Delta I_{L_{1\mathrm{A}}} = 5.81\,\mathrm{A}$, $\Delta I_{L_{1\mathrm{B}}} = 5.83\,\mathrm{A}$, $\Delta I_{L_{2\mathrm{A}}} = 4.05\,\mathrm{A}$, and $\Delta I_{L_{2\mathrm{B}}} = 4.11\,\mathrm{A}$, respectively. The relevant current ripple ratios are 0.276, 0.277, 0.191 and 0.194, agreeing well with the theoretical predictions (57) - (60). The current ripple ratios for i_{L_1} and i_{L_2} are further minimized to 0.082 and 0.057, respectively owing to the interleaved switching scheme as shown in Fig. 20(c).

Fig. 20(d) shows that the steady-state voltages across the switched capacitors, with measured values of $V_{C_{1\mathrm{B}}} = 248.7\,\mathrm{V}$, $V_{C_{2\mathrm{A}}} = 495.1\,\mathrm{V}$ and $V_{C_{2\mathrm{B}}} = 650.3\,\mathrm{V}$, which are consistent with the theoretical values from (28). The output voltage is obtained as $V_{\mathrm{High}} = 800.3\,\mathrm{V}$. Fig. 20(e) depicts the voltage stresses on switches $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$, $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}$, $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ and $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}$. The steady-state turn-off voltages are observed as $V_{\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}} = 330.7\,\mathrm{V}$, $V_{\mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}} = 166.9\,\mathrm{V}$, $V_{\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}} = 167.4\,\mathrm{V}$ and $V_{\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}} = 165.9\,\mathrm{V}$. It is noteworthy that some voltage stresses on power devices are even below half of V_{High}. In addition, Fig. 20(f) shows the successful achievement of ZVS turn-on and turn-off commutations on the counterpart switches $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$ under the SR conditions.

B. Steady-State Performances in the Buck Mode

1) 400V to 72V/48V: Fig. 21 provides a detailed depiction of key experimental waveforms in a buck mode, where the DC input voltage V_{High} and the load resistances R_{Low1}, R_{Low2} are set as 400 V, 3.46 Ω and 2.30 Ω, respectively. As shown in Fig. 21(a), the main switches $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$ are center-aligned with the same phase. In contrast, $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$ and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ operate with a 180° phase shift relative to $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$. The duty cycles for $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$ and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ are consistently fixed at 0.5, while those for $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$ are set at 0.64 and 0.55, respectively.

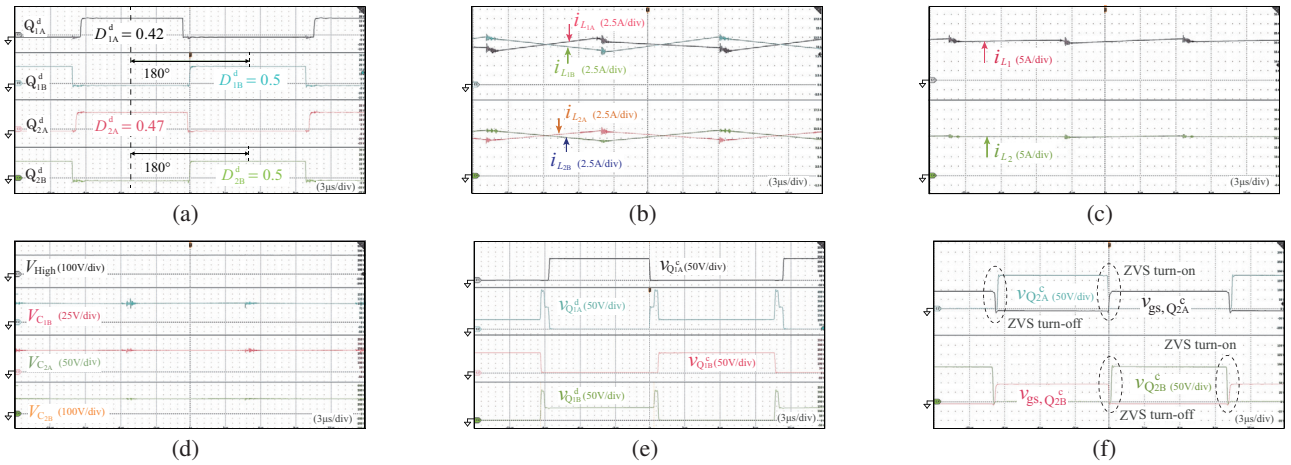


Fig. 19. Observed waveforms in a boost mode with $V_{\mathrm{Low1}} = 72\,\mathrm{V}$, $V_{\mathrm{Low2}} = 48\,\mathrm{V}$ and $R_{\mathrm{High}} = 64\,\Omega$ for $V_{\mathrm{High}} = 400\,\mathrm{V}$: (a) gate signals, (b) DC inductor currents, (c) DC inductor total currents in each low-side port, (d) output voltage and switched capacitor voltages, (e) power switch voltage stresses, and (f) synchronous rectifier voltages.

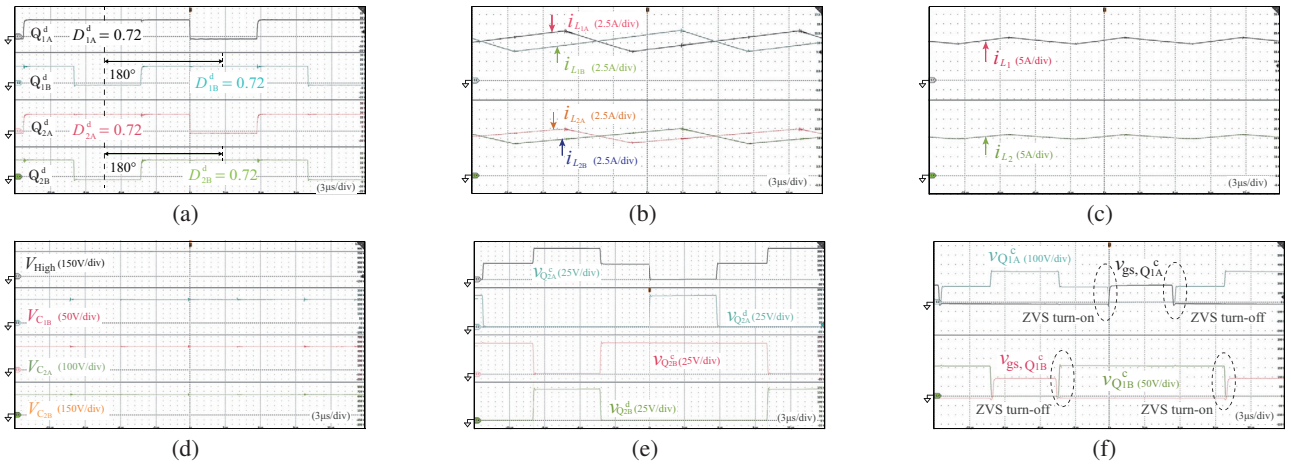


Fig. 20. Observed operating waveforms in a boost mode with $V_{\mathrm{Low1}} = 72\,\mathrm{V}$, $V_{\mathrm{Low2}} = 48\,\mathrm{V}$ and $R_{\mathrm{High}} = 256\,\Omega$ for $V_{\mathrm{High}} = 800\,\mathrm{V}$: (a) gate signals, (b) DC inductor currents, (c) DC inductor total currents in each low-side port, (d) output voltage and switched capacitor voltages, (e) power switch voltage stresses, and (f) synchronous rectifier voltages.

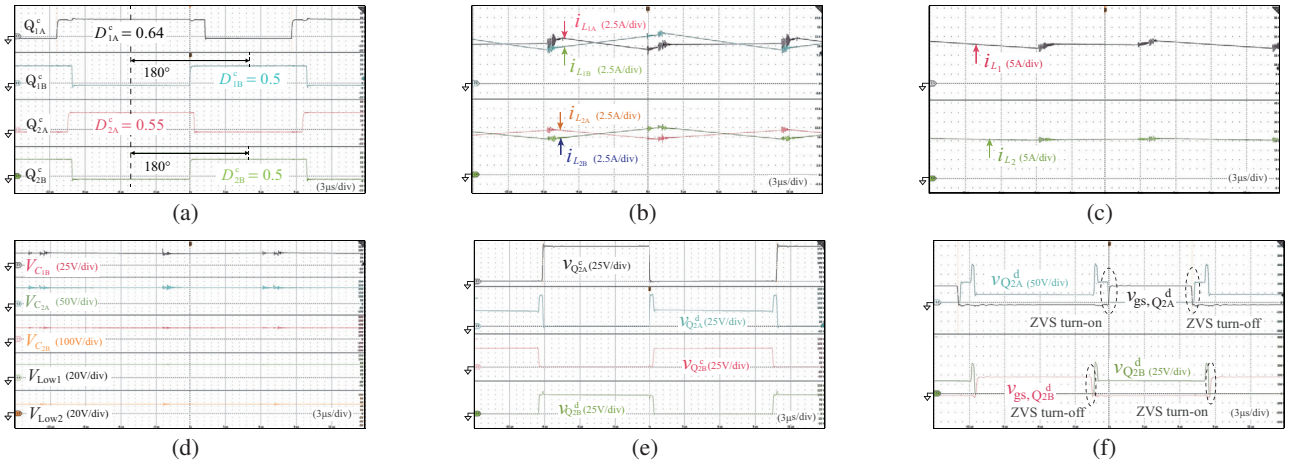


Fig. 21. Observed operating waveforms in a buck mode with $V_{\mathrm{High}} = 400\,\mathrm{V}$, $R_{\mathrm{Low1}} = 3.46\,\Omega$ and $R_{\mathrm{Low2}} = 2.30\,\Omega$ for $V_{\mathrm{Low1}} = 72\,\mathrm{V}$ and $V_{\mathrm{Low2}} = 48\,\mathrm{V}$: (a) gate signals, (b) DC inductor currents, (c) DC inductor total currents in each low-side port, (d) output voltages and switched capacitor voltages, (e) power switch voltage stresses, and (f) synchronous rectifier voltages.

The current waveforms of the DC inductors are illustrated in Fig. 21(b). The average currents for $L_{1\mathrm{A}}$, $L_{1\mathrm{B}}$, $L_{2\mathrm{A}}$, and $L_{2\mathrm{B}}$ are measured as $I_{L_{1\mathrm{A}}} = 10.60\,\mathrm{A}$, $I_{L_{1\mathrm{B}}} = 10.72\,\mathrm{A}$, $I_{L_{2\mathrm{A}}} = 10.69\,\mathrm{A}$, and $I_{L_{2\mathrm{B}}} = 10.61\,\mathrm{A}$ respectively, indicating a balanced average inductor current in the proposed BDC with A-DLC1. The current ripples for $i_{L_{1\mathrm{A}}}$, $i_{L_{1\mathrm{B}}}$, $i_{L_{2\mathrm{A}}}$, and $i_{L_{2\mathrm{B}}}$ are observed as $\Delta I_{L_{1\mathrm{A}}} = 3.37\,\mathrm{A}$, $\Delta I_{L_{1\mathrm{B}}} = 4.74\,\mathrm{A}$, $\Delta I_{L_{2\mathrm{A}}} = 2.74\,\mathrm{A}$, and $\Delta I_{L_{2\mathrm{B}}} = 3.01\,\mathrm{A}$, respectively. The

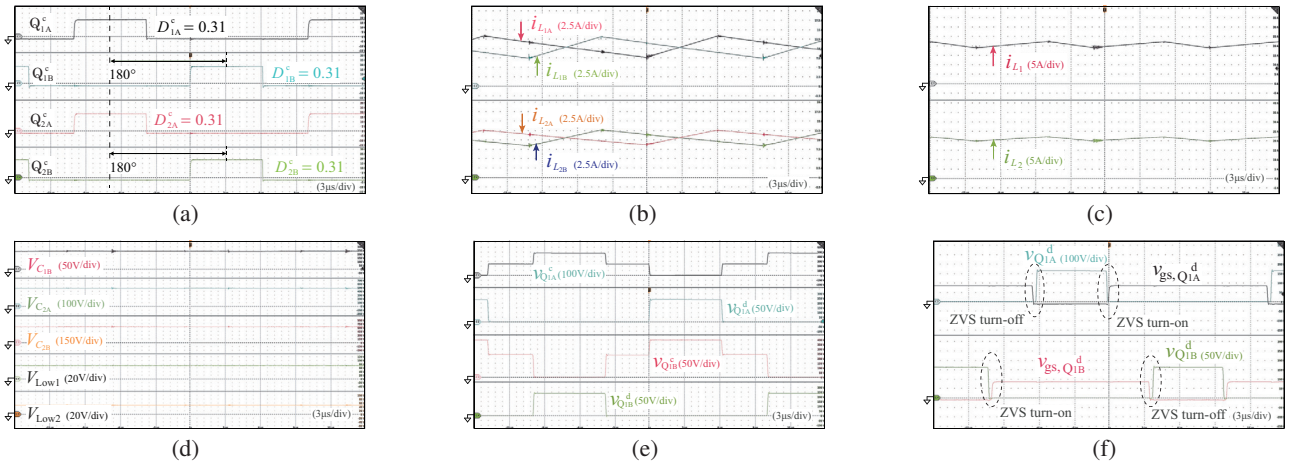


Fig. 22. Observed operating waveforms in a buck mode with $V_{\mathrm{High}} = 800\,\mathrm{V}$, $R_{\mathrm{Low1}} = 3.46\,\Omega$ and $R_{\mathrm{Low2}} = 2.30\,\Omega$ for $V_{\mathrm{Low1}} = 72\,\mathrm{V}$ and $V_{\mathrm{Low2}} = 48\,\mathrm{V}$: (a) gate signals, (b) DC inductor currents, (c) DC inductor total currents in each low-side port, (d) output voltages and switched capacitor voltages, (e) power switch voltage stresses, and (f) synchronous rectifier voltages.

current ripple rates for these inductors are found to be 0.159, 0.221, 0.128, and 0.142, respectively, matching the theoretical values in (65) - (68). Fig. 21(c) demonstrates that the current ripple ratios for i_{L_1} and i_{L_2} are further reduced to 0.112 and 0.030, respectively, due to the interleaved switching patterns, which helps in minimizing the need for filtering capacitors.

Fig. 21(d) presents the steady-state voltages across the capacitors. The measured values are, $V_{C_{1\mathrm{B}}} = 78.99\,\mathrm{V}$, $V_{C_{2\mathrm{A}}} = 215.7\,\mathrm{V}$, and $V_{C_{2\mathrm{B}}} = 302.8\,\mathrm{V}$, corresponding well with (38). Additionally, the output voltages are controlled as $V_{\mathrm{Low1}} = 72.09\,\mathrm{V}$ and $V_{\mathrm{Low2}} = 48.05\,\mathrm{V}$,in accordance with the command value, whereby the validity of (39) and (40) are revealed. Fig. 21(e) illustrates the steady-state voltage stresses on switches $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$, $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}$, $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ and $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}$, whereby $V_{\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}} = 187.9\,\mathrm{V}$, $V_{\mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}} = 168.5\,\mathrm{V}$, $V_{\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}} = 100.1\,\mathrm{V}$ and $V_{\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}} = 100.5\,\mathrm{V}$. It should be remarked herein some voltage stresses are even lower than half of V_{High}. The black dash-circles in Fig. 21(f) reveal the successful achievement of both ZVS turn-on and turn-off transitions on the counterpart switches $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{B}}$ under the condition of SR.

2) 800V to 72V/48V: Fig. 22 illustrates the primary experimental waveforms in a buck mode, where the DC input voltage V_{High} and the load resistances R_{Low1}, R_{Low2} are set as $800\,\mathrm{V}$, $3.46\,\Omega$ and $2.30\,\Omega$, respectively. As depicted in Fig. 22(a), the main switches $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$ are center-aligned with identical phases. In contrast, $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$ and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ are operated with 180° phase shift relative to $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$. Under this condition, the A-DLC1 is inactive, and the duty cycle for all the main switches is uniformly set to 0.31. Fig. 22(b) displays the current waveforms of the DC inductors. The average currents in $L_{1\mathrm{A}}$, $L_{1\mathrm{B}}$, $L_{2\mathrm{A}}$, and $L_{2\mathrm{B}}$ are measured as $I_{L_{1\mathrm{A}}} = 10.51\,\mathrm{A}$, $I_{L_{1\mathrm{B}}} = 10.47\,\mathrm{A}$, $I_{L_{2\mathrm{A}}} = 10.61\,\mathrm{A}$, and $I_{L_{2\mathrm{B}}} = 10.56\,\mathrm{A}$, respectively, demonstrating the balance of average inductor currents. In addition the current ripples for $i_{L_{1\mathrm{A}}}$, $i_{L_{1\mathrm{B}}}$, $i_{L_{2\mathrm{A}}}$, and $i_{L_{2\mathrm{B}}}$ are $\Delta I_{L_{1\mathrm{A}}} = 5.95\,\mathrm{A}$, $\Delta I_{L_{1\mathrm{B}}} = 5.97\,\mathrm{A}$, $\Delta I_{L_{2\mathrm{A}}} = 4.21\,\mathrm{A}$, and $\Delta I_{L_{2\mathrm{B}}} = 4.25\,\mathrm{A}$, respectively. The corresponding ripple ratios for these inductors are recognized as 0.284, 0.285, 0.198, and 0.201, respectively, which well agrees with the theoretical values in (65) - (68). Due to the adoption of interleaved switching topologies, the current ripple rates for i_{L_1} and i_{L_2} are further reduced to 0.096 and 0.055, respectively as shown in Fig. 22(c).

Fig. 22(d) demonstrates that the steady-state voltages across the switched capacitors are $V_{C_{1\mathrm{B}}} = 238.3\,\mathrm{V}$, $V_{C_{2\mathrm{A}}} = 480.9\,\mathrm{V}$ and $V_{C_{2\mathrm{B}}} = 637.6\,\mathrm{V}$, which correspond well with the theoretical predictions in (34). Fig. 22(e) illustrates the steady-state voltage stresses on switches $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$, $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}$, $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$, and $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$. The observed turn-off voltages are $V_{\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}} = 481.0\,\mathrm{V}$, $V_{\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}} = 240.3\,\mathrm{V}$, $V_{\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}} = 400.2\,\mathrm{V}$ and $V_{\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}} = 236.6\,\mathrm{V}$, all of which are below the high voltage. Additionally, the black dash-circles in Fig. 22(f) highlight the successful ZVS turn-on and turn-off commutations on the counterpart switches $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$ under the SR conditions.

C. Power Conversion Efficiencies and Loss Analysis

In addition to voltage ratio range and current ripple rates, conversion efficiency is a critical index for evaluating the performance of the converter. The proposed MP-BDC, employing the A-DLC control strategy, is evaluated for efficiency in both the boost and buck modes under a closed-loop control scheme. The high-side voltage conditions are set to $V_{\mathrm{High}} = 400\,\mathrm{V}$ and $V_{\mathrm{High}} = 800\,\mathrm{V}$, respectively. In boost mode, the maximum efficiencies are recorded as $98.02\,\%$ and $98.39\,\%$, respectively, as shown in Fig. 23(a). In buck mode, the maximum efficiencies reach $98.04\,\%$ and $98.46\,\%$, respectively, as illustrated in Fig. 23(b). These results demonstrate the outstanding high efficiency performance of the MP-BDC in the bidirectional power conversion. It should be remarked here that efficiencies exceeding $97\,\%$ are consistently achieved within the $20\,\%$–$100\,\%$ load range in both operating modes.

A detailed analysis of power losses in the boost mode is presented below. Fig. 24 shows the theoretical power loss distribution for the experimental prototype operating with input voltages $V_{\mathrm{Low1}} = 72\,\mathrm{V}$ and $V_{\mathrm{Low2}} = 48\,\mathrm{V}$, and an output power of $P_{\mathrm{o}} = 2.5\,\mathrm{kW}$. When the high-side output voltage is set to $V_{\mathrm{High}} = 400\,\mathrm{V}$, the total power loss is $65\,\mathrm{W}$, resulting in an efficiency of $\eta = 97.47\,\%$, as depicted in Fig. 24(a). The power losses are distributed as follows: conduction losses and switching losses in the power switches amount to $32.34\,\mathrm{W}$ and $20.56\,\mathrm{W}$, accounting for $49.75\,\%$ and $31.63\,\%$ of the total

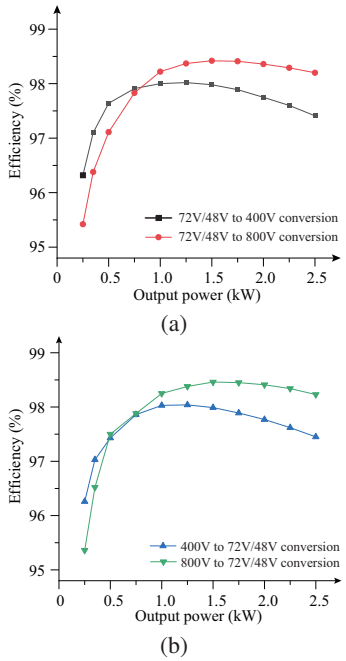


Fig. 23. Actual conversion efficiencies in the MP-BDC: (a) boost mode, and (b) buck mode (measured by YOKOGAWA WT1800 power analyzer).

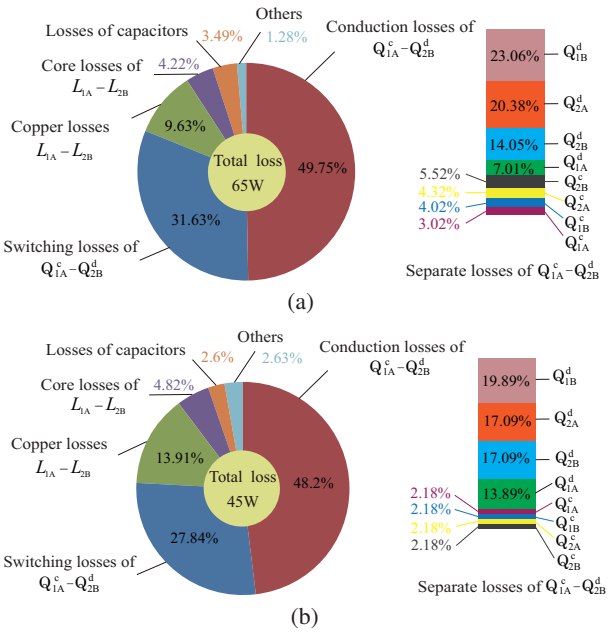


Fig. 24. Power loss breakdown in a boost mode with $V_{\mathrm{Low1}} = 72\,\mathrm{V}$, $V_{\mathrm{Low2}} = 48\,\mathrm{V}$ and $P_{\mathrm{o}} = 2.5\,\mathrm{kW}$: (a) $V_{\mathrm{High}} = 400\,\mathrm{V}$, and (b) $V_{\mathrm{High}} = 800\,\mathrm{V}$.

losses, respectively. Copper losses and iron core losses in the inductors are observed as $6.26\,\mathrm{W}$ and $2.74\,\mathrm{W}$, representing $9.63\,\%$ and $4.22\,\%$ of the total losses, while the total capacitor power losses are $2.27\,\mathrm{W}$ ($3.49\,\%$). Other losses, including PCB trace losses and gate driver losses are calculated as $0.73\,\mathrm{W}$. Among these, conduction losses in power switches dominate during high-power output scenarios. It should be remarked here that the losses for $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$ and $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}$ are outstanding as $14.99\,\mathrm{W}$ and $13.25\,\mathrm{W}$, respectively. Meanwhile, the switching losses for components $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{A}}$, $\mathrm{Q}^{\mathrm{c}}_{1\mathrm{B}}$, $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{A}}$ and $\mathrm{Q}^{\mathrm{c}}_{2\mathrm{B}}$ are negligible due to ZVS turn-on and turn-off operations. Consequently, thermal management on $\mathrm{Q}^{\mathrm{d}}_{1\mathrm{B}}$ and $\mathrm{Q}^{\mathrm{d}}_{2\mathrm{A}}$ will reduce the power losses effectively.

When the high-side output voltage increases to $V_{\mathrm{High}} = 800\,\mathrm{V}$, the total power loss decreases significantly to $45\,\mathrm{W}$, corresponding to an efficiency of $\eta = 98.23\,\%$, as shown in Fig. 24(b). Under this condition, conduction and switching losses in the switches are $21.69\,\mathrm{W}$ and $12.53\,\mathrm{W}$, accounting for $48.2\,\%$ and $27.84\,\%$ of the total losses, respectively. Copper and core losses in the inductors are $6.26\,\mathrm{W}$ and $1.17\,\mathrm{W}$, while capacitor losses account for $2.03\,\mathrm{W}$. Compared to the operating condition that $V_{\mathrm{High}} = 400\,\mathrm{V}$ case, the increased high-side voltage reduces current stress on the power switches by nearly half, significantly lowering conduction and switching losses. This enhancement results in higher conversion efficiency in a higher output dc voltage. Overall, in the boost mode, conduction losses in power switches remain the primary source of power loss. Increasing the high-side voltage not only reduces these losses but also alleviates thermal management challenges for the switches. A similar analysis can be applied to buck mode.

D. Dynamic Performances

Fig. 25 (a) and (b) illustrate the waveforms of the output voltage V_{High} and inductor currents i_{L1} and i_{L2} in the boost mode, where the input voltages are regulated at $V_{\mathrm{High}} = 400\,\mathrm{V}$ and $V_{\mathrm{High}} = 800\,\mathrm{V}$, respectively. The output power periodically alternates between $2.5\,\mathrm{kW}$ and $1.25\,\mathrm{kW}$. The transitional performance clearly demonstrates that V_{High} is effectively regulated at the target voltage despite load variations, highlighting the robustness of the proposed converter.

Fig. 25(c) presents the waveforms of the output voltage V_{Low} and inductor currents i_{L1} and i_{L2} in the buck mode. In this scenario, the input voltage is maintained at $V_{\mathrm{High}} = 400\,\mathrm{V}$, and the load resistance alternates periodically between $1.44\,\Omega$ ($2.5\,\mathrm{kW}$) to $2.88\,\Omega$ ($1.25\,\mathrm{kW}$). Due to the limitations of the laboratory setup, where electronic loads cannot synchronize dynamically, the low-voltage ports are combined into a single port for the experiment. This adjustment ensured practical validation of the closed-loop control under the given constraints. The dynamic waveforms clearly indicate that the output voltage V_{Low} is consistently regulated at $60\,\mathrm{V}$, maintaining stable operation despite variations in load resistance. When the input voltage increases to $V_{\mathrm{High}} = 800\,\mathrm{V}$, the dynamic response exhibits similar results.

E. Robustness of Average Inductor Current

Fig. 26(a) showcases the experimental results in the boost mode, highlighting the tolerance of the four inductors' variations on the average inductor current. The inductances of $L_{1\mathrm{A}}$, $L_{1\mathrm{B}}$, $L_{2\mathrm{A}}$ and $L_{2\mathrm{B}}$ are set to $219\,\mu\mathrm{H}$ (1.26 times the nominal value), $174\,\mu\mathrm{H}$ (the nominal value), $174\,\mu\mathrm{H}$ and $219\,\mu\mathrm{H}$ (1.26 times the nominal value), respectively. The results confirm that applying A-DLC achieves balanced average inductor currents at each low-voltage port in CCM, even with inductance value fluctuations of up to $26\,\%$. Furthermore, as shown in Fig. 26(b), where D^{d}_1 and D^{d}_2 satisfy equation L_a, the balance of all inductor currents is maintained even under significant inductance variations. As a result, the proposed

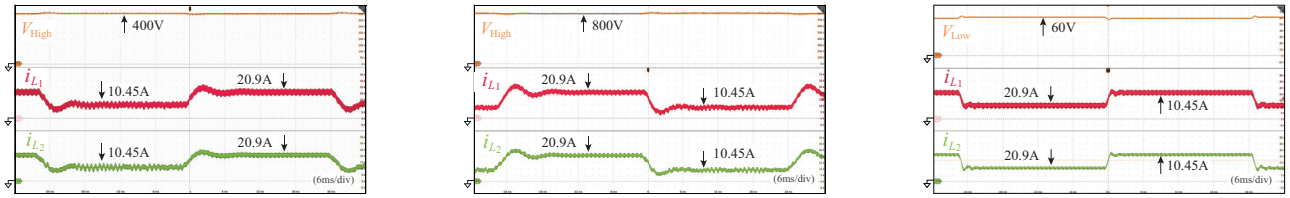


Fig. 25. Transient waveforms of the output voltage and inductor currents under the condition of closed loop: (a) boost mode for $V_{\mathrm{High}} = 400\,\mathrm{V}$ output with $V_{\mathrm{Low1}} = 72\,\mathrm{V}$ and $V_{\mathrm{Low2}} = 48\,\mathrm{V}$ inputs, (b) boost mode for $V_{\mathrm{High}} = 800\,\mathrm{V}$ output with $V_{\mathrm{Low1}} = 72\,\mathrm{V}$ and $V_{\mathrm{Low2}} = 48\,\mathrm{V}$ inputs, and (c) buck mode for $V_{\mathrm{Low1}} = V_{\mathrm{Low2}} = 60\,\mathrm{V}$ outputs with $V_{\mathrm{High}} = 400\,\mathrm{V}$ input.

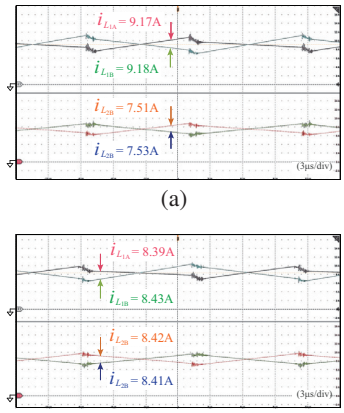


Fig. 26. Tolerances on the average inductor current for the DC inductor variations with $V_{\mathrm{Low1}} = 72\,\mathrm{V}$, $V_{\mathrm{Low2}} = 48\,\mathrm{V}$ and $R_{\mathrm{High}} = 80\,\Omega$ for $V_{\mathrm{High}} = 400\,\mathrm{V}$: (a) $D_1^{\mathrm{d}} = D_2^{\mathrm{d}} = 0.46$, and (b) $D_1^{\mathrm{d}} = 0.42$, $D_2^{\mathrm{d}} = 0.472$.

control strategy exhibits remarkable robustness to variations in the DC inductors.

F. Comparison of Relevant BDCs

In order to reveal the performance of the proposed MP-BDC, a comprehensive comparison with the existing BDC topologies are summarized in TABLE III. An isolated MP-BDC for integrating hybrid renewable energy systems into a DC microgrid is proposed in [17]. While the converter achieves soft switching, its use of multiple transformers results in relatively low efficiency at high output power. A dual transformer-based triple-port active bridge converter with self-current balancing is introduced in [20], enabling power sharing among low-voltage ports. However, it involves a large number of power devices and a complex control strategy, with efficiency not explicitly addressed. In [22], a partially isolated MP-BDC integrating an interleaved PWM converter and a DAB converter achieves inductor current balancing. However, it relies on a high transformer turns ratio (3:50) to attain a substantial voltage conversion ratio, and its efficiency at full load is only 93.5%, limiting its adaptability for high-power applications. Similarly, [23] proposed a soft-switched current-fed dual-input isolated DC–DC converter with a simple topology and minimal components. However, this topology should make the two DC sources as identical, restricting the application extended for a variety of energy sources. Additionally, primary-side switches must operate with duty cycles above 50%, imposing any constraint on the achievable voltage conversion ratio.

Non-isolated converters generally exhibit higher efficiency compared to isolated designs, as shown in Table III. For instance, [36] proposed a non-isolated converter with coupled inductors and a voltage multiplier circuit to achieve a high voltage ratio with fewer active switches. However, the leakage inductance and hard switching degrade the efficiency. A multi-port DC–DC converter with four ports for renewable energy applications was introduced in [48]. While it combines quasi-interleaved boost converters, a switched capacitor, and a voltage multiplier to achieve a high voltage ratio, it suffers from low output power and efficiency, which is not suitable for high-power EV fast charging. An evolutionary dual-input single-output DC–DC converter with multi-mode operation was proposed in [49], combining a conventional boost and a modified buck-boost converter. However, its output power is limited to 100 W, accordingly the circuit topology is not suitable for high-power scenarios. The circuit topology proposed in [50] integrates three basic boost cells, enabling flexible operating modes among the input ports. However, its reliance on equal duty-cycle control restricts its inductor current balancing capabilities across the full range of duty cycle, and the large inductors required hinder miniaturization and high-density integration. The converter in [52] adopts a switched capacitor and an asymmetric duty-cycle limit control strategy, enhancing inductor current balance and reducing counts of components. Furthermore, the use of SiC-MOSFETs achieves an efficiency exceeding 97%. However, the high-efficiency performance is constrained in a narrow range of voltage conversion ratio, which is obstacle for applications for the scenarios with wide range of voltage ratios. In order to address these limitations, a floating four-phase interleaved charge pump bidirectional DC–DC converter with an asymmetric duty-cycle limit control strategy is proposed in [53]. This strategy ensures inductor current balance across the entire duty-cycle range. However, the converters presented in [52] and [53] are difficult to implement in the multi-port system architectures of DC microgrids.

The proposed BDC overcomes these challenges by achieving multi-port operation, a higher voltage conversion ratio, and enhanced efficiency. Despite necessity of relatively more active components, the use of SiC-MOSFETs significantly reduces switching losses and improves overall efficiency, even with hard switching. The ZVS in SR switches further optimizes efficiency. Additionally, although MOSFETs in zones B or M are subjected to voltage stress equal to the high-voltage side, the converter predominantly operates in zones A/C and L/M, where the maximum voltage stress on the active switches is lower, facilitating the selection of lower voltage-rated power devices.

TABLE III
COMPARISON OF PROPOSED AND EXISTING BIDIRECTIONAL DC–DC CONVERTERS FOR DC MICROGRID

Reference (Type)	Peak Efficiencies (Boost/Buck)	Voltage Conversion Ratio		Components	Specifications	Maximum Voltage Stress		Inductor Current Balance
		Boost	Buck			Capacitors	MOSFETs	
[17] Multi-port isolated	95%/94.8%	Low	Low	T:2; L:1 C:5; SW:6 D:2	36V/43V/180V 120W/50kHz/GaN PWM+Phase shift	$\frac{U_{\text{high}}}{2}$	U_{high}	——
[20] Multi-port isolated	——/——	Low	Low	T:2; L:3 C:3; SW:12	70V/100V/—— 1kW/20kHz/Si PWM+Phase shift	U_{high}	U_{high}	Full duty
[22] Multi-port isolated	94.4%/93.5%	High	High	T:1; L:2 C:5; SW:8	12V/48V/400V 1kW/50kHz/Si PWM+Phase shift	U_{high}	U_{high}	Full duty
[23] Multi-port isolated	96%/95.2%	Low	Low	T:1; L:3 C:8; SW:4	0-30V/150V 250W/62kHz/Si PWM	$\frac{U_{\text{high}}}{2}$	U_{high}	Half duty
[36] Multi-port non-isolated	93.5%/——	High	High	L:2; CL:1 C:6; SW:4 D:4	24/24V/300V 300W/50kHz/Si PWM	U_{high}	$\frac{2U_{\text{high}}}{3}$	No
[48] Multi-port non-isolated	94.8%/93.2%	High	High	L:4; C:7 SW:4; D:5	20V/20V/24V/400V 250W/50kHz/Si PWM	U_{high}	——	No
[49] Multi-port non-isolated	96%	High	High	L:3; C:5 SW:3; D:3	12/24V/150V 100W/50kHz/Si PWM	U_{high}	$\frac{NU_{\text{high}}}{N+1}$	No
[50] Multi-port non-isolated	95.7%	Medium	Medium	L:3; C:6 SW:9	12V/12V/12V/100V 200W/50kHz/Si PWM	U_{high}	——	No
[52] Two-port non-isolated	97.5%/97.5%	Low	Low	L:2; C:3 SW:4	60V/200-380V 500W/50kHz/SiC PWM(A-DLC)	U_{high}	U_{high}	Full duty
[53] Two-port non-isolated	97.6%/98.3%	High	High	L:4; C:5 SW:8	72V/400-800V 1kW/50kHz/SiC PWM(A-DLC)	$\frac{U_{\text{high}}+U_{\text{low}}}{2}$	$\frac{U_{\text{high}}+U_{\text{low}}}{2}$	Full duty
[Proposed] Multi-port non-isolated	98.4%/98.0%	High	High	L:4; C:6 SW:8	72V/48V/400-800V 2.5kW/50kHz/SiC PWM(A-DLC)	U_{high}	U_{high}	Full duty

N: windings turns ratio; T: transformer; L: inductor; CL: coupled inductor; C: capacitor; SW: power switch; D: diode; —— : not reported

VI. CONCLUSIONS

The new MP-BDC topology for DC microgrid energy systems has been proposed in this article, and its operating principle and the steady-state performance have been demonstrated by comprehensive steady-state analysis. The essential performances of the proposed MP-BDC have been validated through experiments including enhanced voltage ratios, high efficiency, and balanced currents in the DC inductors.

The proposed circuit topology and duty cycle control scheme enable wide buck/boost voltage ratios and full-range inherent current balancing. The asymmetrical DLC strategy has been demonstrated for an EV-connected DC microgrid system featuring a wide high-side voltage range. A prototype utilizing SiC-MOSFETs is developed with specifications of 2.5 kW - 50 kHz, showcasing the actual performance of the MP-BDC. This prototype effectively validate a wide voltage ratio range between the variable high-side voltage (400 - 800 V) and the constant low-side voltages (72 V/48 V). Efficiencies exceeding 97 % are achieved within the 20 % - 100 % load range, attributed to the utilization of SiC-MOSFETs.

Future work will focus on exploring the energy transfer between the PV/FC and ESS, as well as implementing soft switching for all the main switches. Efforts will also be directed toward increasing the operating frequency and enhancing power density to broaden the applicability of the BDC in diverse fields, including EV fast charging and renewable energy integration.

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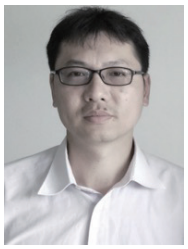

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