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(Citation)
Memoirs of the Graduate Schools of Engineering and System Informatics Kobe University,8:1-4

(Issue Date)
2016

(Resource Type)
departmental bulletin paper

(Version)
Version of Record

(URL)
https://hdl.handle.net/20.500.14094/81009697

Memoirs of the Graduate Schools of Engineering and System Informatics Kobe University
No. 8, pp. 1–4, 2016. doi:10.5047/gseku.e.2016.002

[Research Paper]

A novel test scheme for detecting faulty recall margin cells for 6T-4C FeRAM

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(Received January 30, 2017; Accepted February 7, 2017; Online published February 13, 2017)

Keywords: *FeRAM, Memory Testing, Non-volatile Memory, Recall Margin.*

This paper proposes a novel test scheme that can detect faulty margin cells in non-volatile 6T-4C FeRAM (six-transistor four-capacitor ferroelectric random access memory). The FeRAM behaves as a non-volatile memory using spontaneous polarization characteristic of the ferroelectric capacitor. The datum is stored as a difference in the polarization direction, and is read out as potential difference of the polarization direction. The proposed test scheme can screen the faulty cells that have smaller recall margins by injecting offset voltage to the memory cell. The proposed scheme is evaluated by Monte Carlo simulations of 16,000 times. The proposed test scheme is possible to detect all fault cells by injecting the offset voltage of 100 mV in a 0.13 μm CMOS process.

1. Introduction

Recently, most of system LSIs are using static random access memory (SRAM) to memorize data because it features fast operation, low energy consumption, and high compatibility with logic circuits. On the other hand, the SRAM is volatile memory that needs a certain amount of energy for a standby state to keep the data. Thus, in an application that has a low activation ratio, the SRAM degrades its performance in energy. These days, non-volatile memory is employed in a system-on-a-chip (SoC) for various applications, such as a sensor network, biomedical monitoring and so on. They have strict constraints in its standby power consumption to reduce battery capacity and the system size. For this reason, non-volatile memory is suitable for the low-leakage applications. There are many kinds of studies of non-volatile memories. In this paper, we focus on the 6T-4C FeRAM which benefit is low-voltage and low-power operation [1,2]. The 6T-4C FeRAM acts as 6T SRAM in read and write operations for high-speed operation and low active power. The data are transferred to ferroelectric capacitors in a standby state. Then, the power supply to the memory cells can be cut off. Therefore, the 6T-4C FeRAM is able to operate at higher speed than other types of the FeRAM. However, there are some extra operations are needed to transfer a datum between non-volatile and volatile memory. These operations are called store and recall operations. The characteristics of a ferroelectric capacitor affects the operating margin. Some defective cells exist because of variation of the ferroelectric capacitances, which causes faulty operation in the recall operation. To make the matter worse, from previous research [3], the ferroelectric capacitance is decreased by repetitive switching. The degradation is called fatigue and caused by repeating reversal polarizations in a ferroelectric capacitor. The effect of the fatigue in a capacitor has a serious impact to the recall operation. Therefore, it is important to evaluate the recall margin in the manufacturing process. In reality, the 6T-4C FeRAM has a structure that is impossible to evaluate its capacitor directly. For this reason, there is a need for an indirect scheme to detect the margin failure cells. Accordingly, the trial measurement for the detection of smaller margin cells is important. We propose a novel test scheme to detect the smaller margin cells in the 6T-4C FeRAM. The outline of this paper is as follows: In Section 2, the details of 6T-4C non-volatile FeRAM is explained. The proposed test scheme to detect faulty margin cells is described in Section 3. The last section concludes this paper.

2. 6T-4C non-volatile memory

The schematic of the 6T-4C FeRAM memory cell is shown in Figure 1. The word lines are shared in each row and the bit line pairs are also shared in each column. Note that two plate lines (PL1, PL2) are prepared to supply voltages to the ferroelectric capacitors, which are shared as well as the bit lines along with the column direction.

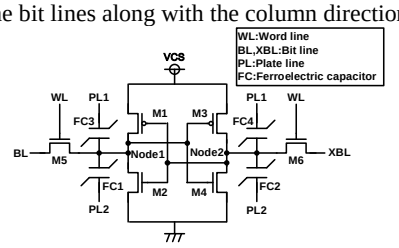

Fig. 1 Schematic of 6T-4C memory cell.

The FeRAM cell consists of two drive transistors (M2, M4), two load transistors (M1, M3), two access transistors (M5, M6), and four ferroelectric capacitors (FC1-4). The internal Nodes1 and Node2 are storage nodes of the flip-flop. A pair

of bit lines (BL and XBL) is connected to the two access transistors as I/O ports. The gates of access transistors are also connected to a word line (WL). The 6T-4C FeRAM cell accommodates two capacitors in each internal node; two plate lines (PL1 and PL2) are connected to the four ferroelectric capacitors to control their directions of polarization. Due to the capacitor pairs, the 6T-4C FeRAM has a better recall margin than other types of FeRAMs (e.g. 6T-2C FeRAM) [3].

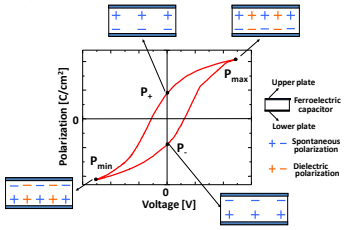

Fig. 2 P-V characteristics of a ferroelectric capacitor [4].

The ferroelectric capacitor consists of filmy ferroelectrics and two electrodes. Figure 2 shows P-V characteristics of the ferroelectric capacitor: the x axis shows the voltage of the electrodes and the y axis shows the polarization of the capacitor. The ferroelectric capacitor has a hysteresis loop. When the capacitor state is at P_-, there is no voltage difference between the electrodes, although the capacitor possesses negative spontaneous polarization. Positive dielectric polarization is generated by applying a positive potential. The direction of the spontaneous polarization begins to invert. Then, the change of the spontaneous polarization completes at P_{max}. After that, without voltage potential, the spontaneous polarization still keeps its direction at P_+, which is the basis of memory function. Similarly, applying a negative potential moves the capacitor's state from P_- to P_{min}. The spontaneous polarization is used as a nonvolatile binary datum in the FeRAM. This FeRAM has four operation modes. The read operation and the write operation are performed while the power is on. These operations are the same as that of 6T SRAM. On the other hand, the store and recall operations are performed before the power is off and on, respectively.

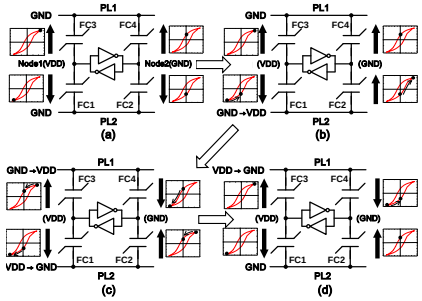

Fig. 3 State change diagram of store operation: (a) initial state, (b) PL2 activation state, (c) PL1 activation state, and (d) completing state.

The memory datum is written to the ferroelectric capacitor in the store operation. The state transition diagram of the store operation is shown in Figures 3. The black arrows in the figure show the directions of the polarization. In the initial state of Figure 3 (a), the two plate lines are grounded and all capacitors are polarized in a certain direction. The first step of the store operation is in Figure 3 (b); the voltage of PL1 has been fixed to the ground although the voltage of PL2 is supplied to VDD. After a sufficient time for switching the spontaneous polarization, the PL2 voltage is turned down. In Figure 3 (c), PL1 takes the same procedure as Figure 3 (b) in which PL1 turns on to VDD. The last step of Figure 3 (d) is a shutdown process.

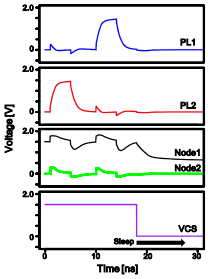

Fig. 4 State change waveforms of store operation.

Figure 4 shows the waveforms of the store operation. The internal nodes are fluctuated by coupling due to the large capacitance of the ferroelectric capacitors. The capacitance is 92fF or 264fF; depending on their polarizaion. However, the data are not disturbed because the potentials of the both nodes are changed in the same direction. The SRAM datum of the volatile memory is transferred to the nonvolatile memory with this operation.

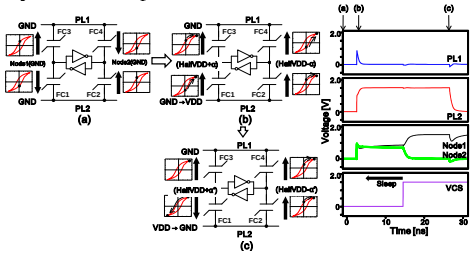

Fig. 5 State change diagrams and waveforms of recall operation: (a) initial state, (b) PL2 activation state, and (c) completing state.

The nonvolatile memory data is retrieved by the recall operation. Figures 5 shows the state transition diagrams and waveforms of the recall operation. The supply voltage of the flip-flop in the SRAM (VCS) is turned off at this moment. Figure 5 (a) is the initial state. In Figure 5 (b), the PL2 voltage is supplied at VDD. This potential biases FC1 and FC4 to the inverting direction; in other words, the capacitances of FC1 and FC4 become larger. At the same time, the PL2 voltage biases FC2 and FC3 to the non-inverting direction; the capacitances of FC2 and FC3 become smaller. Thereby, as the right figure shows, the voltage of the Node1 becomes larger than half VDD (half VDD + α) and the voltage of the Node2 becomes smaller (half VDD - α). The VCS is then turned on to distinguish the datum after waiting sufficient time. At the last process of Figure 5 (c), PL2 gets back to the ground and the recall operation is completed. The ferroelectric capacitor datum of the nonvolatile memory is transferred to the SRAM by this operation.

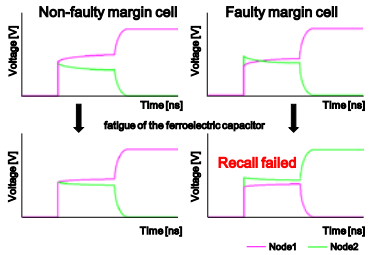

Fig. 6 Recall failure mode caused by fatigue of ferroelectric capacitor.

The waveforms of recall failure mode are shown in Figure 6. The non-faulty margin cell has an enough recall margin. The non-faulty margin cell can operate normally. On the other hand, the faulty cell will fail to transfer a datum from the

capacitance in the recall operation. This means that a faulty margin cell cannot operate normally the recall operation due to fatigue of the ferroelectric capacitor. To avoid the failure by faulty recall margin of the cell, we propose a test scheme to detect smaller margin cell. The read and write operations are not treated in this paper because they are almost the same as the SRAM operations.

3. Test scheme for detecting faulty margin cells

The proposed test scheme is named “offset voltage injection scheme”. This scheme biased one of the cell nodes to screening faulty cell during recall operation. The proposed scheme makes the recall margin degrade by the offset voltage. The trial recall operation gives the stress to a cell and tests whether the cell is possible to perform a normal recall operation. In this paper, all simulations use a commercial HSPICE transistor model in a 0.13-μm bulk CMOS process. Local variation in transistors is also considered in the model. A simulation model of a ferroelectric capacitor is described in Verilog-AMS. The ferroelectric capacitor has variation in capacitance, which is based on actual measurement data. The faulty recall margin is set to 50 mV in the simulation. Note that the faulty recall margin depends on process and circuitry.

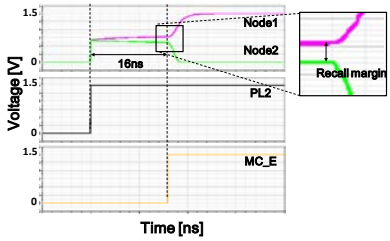

Fig. 7 Simulation waveforms of normal recall operation.

The offset value between the bitlines is determined by the recall margin, which is required by application. Therefore, injecting an arbitrary value of the offset voltage is useful as a test scheme. Figures 7 show the simulation waveforms of the normal recall operation. In this test scheme, the Node1 is set to High and the Node2 is set to Low; the recall margin is defined as a potential difference between Node1 and Node2 after 16 ns from the power-on of PL2. This is because the test circuit assumes an operating frequency of 25 MHz. In timing design, the maximum time during which we could wait for internal nodes to be separated in the recall operation is 16 ns.

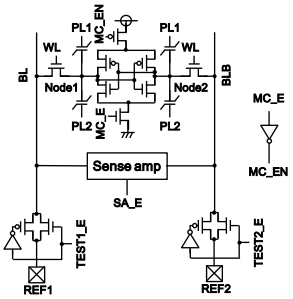

Fig. 8 Circuit schematic of 6T-4C FeRAM cell and peripheral.

The circuit diagram of the proposed test circuit is shown in Figure 8. A pair of ports with transmission gates are added to the bit line pair for external inputs. The proposed test scheme is carried out in three steps. In Step 1, the offset voltage of REF1 or REF2 is injected to the Node1 and Node2 respectively when WL is on. In Step 2, PL2 turns on and the recall operation is performed. In Step 3, supplying power to the cell after 16 ns from the start of the recall operation. The faulty cell, which datum is inverted, is screened because the recall margin of the faulty cell is smaller by the offset voltage. A larger offset voltage causes more unsuccessful recall operation.

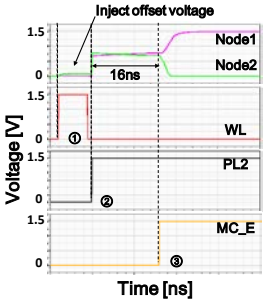

Fig. 9 Recall operation waveforms of non-faulty cell in the proposed scheme.

Figure 9 shows the waveforms of the trial recall operation for a non-faulty cell. The numbers in the figure correspond to the above-mentioned steps of the proposed test scheme. The injected offset voltage is 100 mV. At the beginning of the second step, the voltage of the Node2 becomes higher due to the offset voltage, and the voltage difference of the internal nodes turns out inverted in the last of the second step (compare to Figure 7). However, this non-faulty cell has tolerance against the offset voltage injection because the recall operation is correctly completed after all.

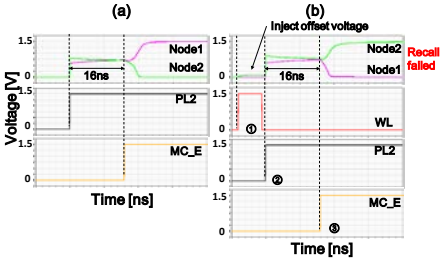

Fig. 10 (a) Recall operation waveforms of faulty cell (a) without and (b) with the proposed test scheme.

In contrast, Figures 10 shows the recall operation waveforms of a faulty cell. Figure 10 (a) corresponds to the normal use without the voltage offset of the proposed test scheme, in which it happens to be read out successfully. However, this cell is flipped under the proposed test scheme as shown in Figure 10 (b). We carried out 32,000 times of Monte Carlo simulations, giving variations to the ferroelectric capacitors and transistors. This means the number of simulations for each case when 16000 cells have data 0 and data 1. This is because our test macro capacity is 16 kb. The faulty margin cell is defined as a cell with a recall margin of 50 mV or less in this simulation. However, as the target recall margin decreases, the offset voltage necessary for detection also decreases. We assumed that a margin of 50 mV is necessary for this supposed application.

Figure 11 illustrates the scatter plot of the Monte Carlo simulation results in case of Node2 datum is Low. The x and y axes shows the respective potentials at Node1 and Node2 at the time of 16 ns elapsed from the start of the recall operation. Each point means a cell that is given transistor and ferroelectric capacitor variations with the Monte Carlo simulation. In other words, the potential difference between Node2 and Node1 is the recall margin. The simulation results are classified into four categories. First of all, we determined “Negative” for those detected as defective cells by the proposed method and “Positive” for those that were

not detected. Next, we classified whether the classification is true by "True" or "False"; note that these classifications are only possible on simulation and only "Positive" or "Negative" is actually observed. "True Positive" (colored with red in Figure 11) means that a faulty margin cell is correctly detected by the proposed scheme. "True Negative" (colored with blue in Figure 11) means that cell has enough margin. "False Positive" (colored with green in Figure 11) means that the proposed scheme erroneously detected a normal cell as a defective cell. "False Negative" (colored with black, but not appear in Figure 11) means that a cell which could not be detected by the proposed method despite being a defective cell. The number of "FN" should be zero.

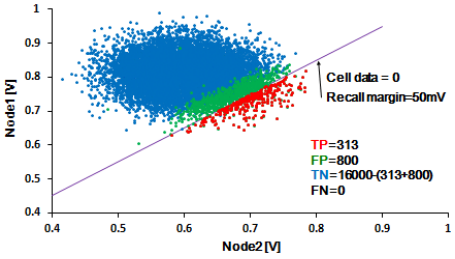

Fig. 11 Scatter plot, when the cell data is Low, at a recall margin of 50 mV and an offset injection of 100 mV. "TP", "FP", "TN", and "FN" mean "Ture Positive", "False Positive", "True Negative", and "False Negative", respectively.

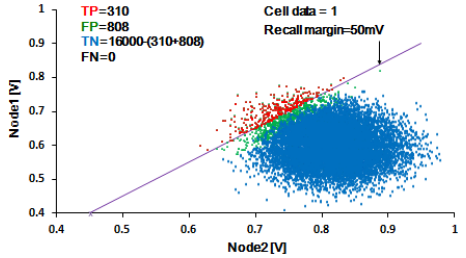

Fig. 12 Scatter plot, when the cell data is High, at a recall margin of 50 mV and an offset injection of 100 mV.

The area of the lower right that the recall margin is less than 50mV is for the faulty cells. The number of the "FN" becomes zero when the cell data is Low and the offset voltage is set to 100 mV, in which case the number of "FPs" is 800. Although the margin of the capacitor in the "FP" cell is normal, due to the transistor variation, it behaves the same as the margin defect cell as a result. Therefore "FP" cells can be treated as potential recall margin defective cells. Figure 12 shows the scatter plot when the cell data is High, as well.

The overhead cost for the detection of faulty recall margin cells with the proposed test scheme is also evaluated. The proposed test can inject a static offset voltage to all cells at the same time; the testing time to adjust an analog voltage is minimized, and there is no testing cycle overhead in the recall operation. The number of test cycles for store and recall operations to/from all ferroelectric capacitors is one each. The number of test cycles for write and read operations from/to all cells depends on memory macro structure. In our design, the total test cycles are 2,052. Table I shows the overhead cost for memory capacity when the offset voltage is varied. At the offset voltage of 100 mV, the "FN" becomes zero; the memory capacity overhead, however, results in 10.1% (= 1,608 / 16,000) although the faulty cells are 3.9% (= 623 / 16,000). If the offset voltage is set to 120 mV, the overhead will be doubled from 10.1% to 20.7%. Therefore, the margin of the offset voltage will be set to less than at most 20 mV in this case. Note that some fault tolerance scheme should be implemented to repair margin defective cells in real application. Another overhead is required for a redundancy technique.

We assume that the proposed scheme is suitable as an initial test for a manufacturer before shipment. A field test is, however, possible if supplies for the offset voltage are available on site.

Table 1 Comparison of the capacity overhead for the offset margin.

Offset [mV]	80	90	100	110	120	130
Counts of Positive	1318	1709	2231	2827	3934	4792
Counts of TP	609	619	623	623	623	623
Counts of FP	709	1090	1608	2204	3311	4169
Counts of FN	14	4	0	0	0	0
Counts of TN	14668	14287	13769	13173	12066	11208
Detection ratio	97.8%	99.4%	100.0%	100.0%	100.0%	100.0%
Overhead ratio	4.4%	6.8%	10.1%	13.8%	20.7%	26.1%

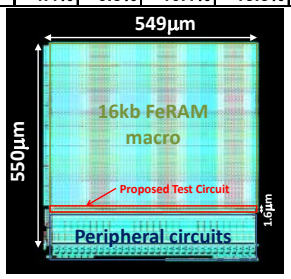

Fig. 13 The layout of 16kb FeRAM macro.

4. Macro implementation and conclusion

We designed a 16-kb 6T-4C FeRAM macro in a 130-nm process technology as shown in Figure 13. The area is 550.2 × 549.6 µm^2. The height of the test circuitry is merely 1.6 µm. Thus the area overhead of the proposed test scheme in the 16-kb macro is less than 0.29%. In this paper, we proposed a novel test scheme for detecting faulty margin cells in 6T-4C FeRAM. The potential difference of the spontaneous polarization between the internal nodes is defined as a recall margin, and a memory cell with the recall margin of 50 mV or less is defined as a faulty one. The proposed test scheme using the offset voltage injection is evaluated by 32,000 times of Monte Carlo simulations. It is confirmed by the simulation that the proposed test scheme is effective to detect all the fault cells at the offset voltage of 100 mV, in which case the memory capacity overhead is 10.1%.

5. Acknowledgments

This research supported by the Ministry of Economy, Trade and Industry (METI) and the New Energy an Industrial Technology Development Organization (NEDO).

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