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Abstract

Growth process of crystalline GaAs on Si(110) surface kept at 773K and the nanostructural analysis of the interface have been studied by a combination of reflection high energy electron diffraction (RHEED) and cross-sectional transmission electron microscopy (TEM) observations. The Si(110) facetted surface along the <001> direction consists of vicinal surfaces inclined +_2 degrees from the <110> direction. In earlier stage of the growth up to the coverage of 12 ML, the vicinal facetted surface is filled from the bottom terraces by GaAs layers and consequently a flat surface is constructed. With increasing layer thickness of GaAs, stacking faults and the subsequent deformation twins are introduced to relax the lattice strain accumulated in the layer by themselves.

1. Introduction

Heteroepitaxial growth of GaAs on Si substrates has attracted much attention due to its many excellent potential for devices of monolithic opto-electronic integrated circuit [1-3] and high efficiency solar cell [4,5]. However, there are inherent difficulties for the preparation of GaAs layer on Si substrates. The large lattice mismatch of 4.1% and the thermal expansion coefficient difference of 60 % [6] will easily cause lattice defects such as threading dislocations which make the quality of the devices critically decrease [7-9]. Therefore, appropriate growth conditions at very early stage are required for the epitaxial growth because a coalescence of GaAs nuclei on Si substrate is a source of the threading dislocations at the early stage.

It is well-known that tilted off Si (100) substrates with periodic step edges on surface are effective to reduce the lattice defects in the GaAs layer deposited on the Si substrate [2,4,10,11]. A homogeneous coverage is enhanced at the early stage of nucleation of crystalline GaAs because adatoms diffusing on surface preferentially adsorb at the step edge sites and step-flow growth is promoted [12-16]. Such morphology of substrate surface affects quality of crystalline materials deposited. It has been reported that quality of crystalline GaAs initially grown on Si surface greatly depends on the atomic surface morphology such as step edge distribution [12].

The Si(110) surface has spontaneously a vicinal facetted structure which consists of step edges, terraces, ledges and kinks due to higher surface energy [17-21], and is expected to produce good epitaxial growth without the tilting substrate. However, to the authors' knowledge, experimental studies on the epitaxial growth of crystalline GaAs on Si(110) surface are few because of complex phase transition of surface reconstruction which depends on the substrate temperature [22-26]. In the present study, growth process of crystalline GaAs on Si(110) and interfacial nanostructure have been studied by reflection high-energy electron diffraction (RHEED) and transmission electron microscopy (TEM), in order to see how crystalline GaAs grown on the Si(110) surface is affected by the characteristic morphology of surface.

2. Experimental

Exactly Si(110)-oriented substrates (p-type Boron doped, Virginia Semiconductor, Inc.)

were loaded into vacuum chamber with base pressure less than 2.0×10^{-7} Pa. The Si substrates were annealed at 1100K for 5 min to remove native oxide from the surface, and then cooled down to the growth temperature with no background flux in the chamber. The Knudsen-cell shutters of Ga and As_4 were opened at the same time. After this procedure, crystalline GaAs layers were grown on Si(110) surface in the chamber by molecular beam epitaxy (MBE). The growth temperature, growth rate and effective V/III pressure ratio were 773K, approximately 0.8 monolayer (ML)/s and 30, respectively. The growth rate was roughly estimated by thickness measurements using the latter cross-sectional TEM observations. The growth process has been observed *in situ* by RHEED at an accelerating voltage of 28 kV. A video tape recorder (VTR) was used for *in situ* recording. The micrographs were reproduced from the VTR data with image processing software. After the depositions, cross-sectional specimens for TEM were prepared by sequential mechanical polishing and dimpling, followed by argon ion milling to electron transparency. The interfacial structures between GaAs and Si were observed by bright-field images (BFIs) and high-resolution images (HRIs) using Hitachi HF-2000 TEM, operating at an accelerating voltage of 200 kV.

3. Results and discussion

Figures 1(a) and 1(b) show RHEED patterns taken from Si(110) surface in <110> and <100> incidence azimuth, respectively. The half-order Laue zone emerges between the zeroth- and the first-order Laue zone, as indicated in Fig. 1(a). The fundamental reflections 10, -10 with the lattice spacing of 0.543nm which corresponds to 001 of the bulk material and the higher orders are recognized in the zeroth-order Laue zone. The reflections 1/2 1/2, -1/2 1/2, and the higher orders appear in the half-order Laue zone. The rods of the half-order and first-order reflections extend to directions inclined approximately +_2 degrees from the <110> direction. The splitting of the rods becomes large with increasing the order of the reflections. The weak fundamental reflections 01, -01 with the lattice spacing of 0.384nm which corresponds to 110 of the bulk materials and the higher orders are recognized in Fig. 1(b). The fundamental reflections are divided into three equal parts by fractional order reflections, as indicated with arrows.

From the result that two kinds of rods which elongate normal to the vicinal surface, i.e.,

2 degrees clockwise and anticlockwise inclined from the direction perpendicular to the shadow edge are observed in Fig. 1(a), it was revealed that the Si(110) facetted surface along the <001> direction consists of vicinal surfaces inclined +_2 degrees from the <110> direction. The vicinal facetted surface may be composed of (110) terraces and mono-step arranged in the <001> directions. On the other hand, the fractional order reflections observed in Fig. 1(b) will arise from kinks on step edges of the vicinal (110) surface. A kink on step edges is composed of three unit cells to the <01> direction at least. It is suggested that arrangement of kinks leads to form 1×3 superlattice reflections. It was suggested from these facts that the Si(110) surface is vicinal to the <100> direction and may have kinks on step edge. This suggestion is different from previously reported surface structure which has 16×2 reconstruction structure and (17,15,1) vicinal plane at 997K [27]. In this study, Si(110) surface might form transiently unique vicinal plane as a metastable phase due to lower substrate temperature.

Figure 2 shows the successive stages of GaAs layer growth at 773K by RHEED patterns in the <110> incidence azimuth. Figures 2(a) and 2(b) show after approximately 12 ML and 43 ML deposition, respectively. The rods of the half-order and first-order reflections extended to directions inclined approximately +_2 degrees from the <110> direction disappear and only rods extended normal to the (110) surface are recognized in the zeroth-order Laue zone, as seen from a comparison of Fig. 1(a) and Fig. 2(a). With increasing layer thickness of GaAs, the RHEED pattern changed from rods to net pattern with weak streaks above 12 ML thickness, as seen from a comparison of Fig. 2(a) and 2(b). The net pattern in Fig. 2(b) can be indexed as the <011> zone axis pattern of GaAs, in which extra spots of 200, 311 and 400 families are superimposed. The extra spots are positioned on one-third of neighboring points in the <111> directions, and result from the reciprocal lattice of the matrix by mirror reflections about the {111} planes. The streaks and extra spots in the RHEED indicate that planer defects such as stacking faults and twin boundaries have been introduced with increasing layer thickness.

From the results, it was revealed that after 12 ML deposition the vicinal facetted surface disappears and the surface was flattened by the GaAs layer, and subsequently with increasing layer thickness, the surface roughening takes place at the same time as planer defects are introduced.

The cross-sectional TEM observations of the interface between GaAs and Si have been carried out, in order to see the growth process at early stage. Figures 3(a) and (b) depict a BFI and HRI in which the incident beam direction is <110>, respectively. In Fig. 3(a), strain contrasts and planer defects appear near the interface and in the layer, respectively. The surface roughening by grooves observed across planer defects threaded to the surface of GaAs layer with the thickness of about 50 nm is consistent with the result of the change in the RHEED to net pattern diffracted by transmitted electrons with increasing layer thickness of GaAs. In Fig. 3(b), the interface estimated from discontinuities between the lattice of GaAs and Si is indicated with a white solid line. Two kinds of misfit dislocations are observed on the interface as indicated with the symbol ⊥ and ⊥. One is a mixed and the other is a pure edge dislocation as indicated with ⊥ and ⊥, respectively. The interface is positioned on these dislocation cores. It has been indicated from this observation that the interface is inclined +_2~4 degrees from <110> direction.

The vicinal surface expected by the RHEED has also been confirmed by the fact that the interface is inclined. Changes from rods to net pattern with weak streaks in the RHEED with increasing layer thickness is related to such a stacking fault and a twin boundary introduced in the layer as observed in Fig. 3(b). The planer defects denuded zone is observed in the thickness of 12 ML from the bottom of the vicinal interface. This result is consistent with the fact that only rods extended normal to the (110) surface in the RHEED are recognized in the early stage of the growth.

The growth process has been discussed based on the above results. In earlier stage of the growth up to the coverage of 12 ML, the gallium and arsenic atoms preferentially stick at the step edges of the vicinal facetted surface [16,28] and the subsequent nucleation of crystalline GaAs and step-flow growth are induced. The vicinal facetted surface is filled from the bottom terraces by the GaAs layers and consequently a flat surface is constructed on the low coverage. On the low coverage, the lattice distortion of GaAs near the interface is tightly bound on the terraces of the vicinal facetted surface of the substrate and partially relaxed toward the refreshed surface. Such an interfacial strain may be relaxed in the different manner depending on the film thickness. With increasing layer thickness, the strain accumulated in the crystalline GaAs layer has to be released by itself. The formation of stacking faults and the subsequent deformation twining become one of passes to relax the lattice strain. The

critical layer thickness below which no planer defects are introduced in the crystalline GaAs was around 12 ML in this case. This value is much higher than that on tilted Si(100) surface of around 2 ML [29]. The reason is that the good epitaxial growth may be attributed to not only the step edge sites of the vicinal surface but also cancellation of interface charge imbalance of polar Ga and As atoms. A total electrostatic charge of the polar Ga and As atoms would be cancelled in each monolayer on Si(110) surface, and does not accumulate during the deposition [30]. The planer defects introduced in the layer with more than the critical thickness thread to the surface and grooves due to different crystal orientations across the planer defects are formed. Consequently, the atomically flat surface changes to rough surface.

4. Summary

Growth process of crystalline GaAs on Si(110) surface kept at 773K and the nanostructural analysis of the interface have been studied by a combination of RHEED and cross-sectional TEM observations. In earlier stage of the growth up to the coverage of 12 ML, the vicinal facetted surface is filled from the bottom terraces by the GaAs layers and consequently a flat surface is constructed. With increasing layer thickness, stacking faults and the subsequent deformation twins are introduced to relax the lattice strain accumulated in the layer by themselves. The critical layer thickness below which no planer defects are introduced in the crystalline GaAs was around 12 ML in this case. The interfacial strain may be relaxed in the different manner depending on the film thickness. Studies to produce planer defect free GaAs layers on Si(110) surface in detail are in progress in our laboratory.

Acknowledgements

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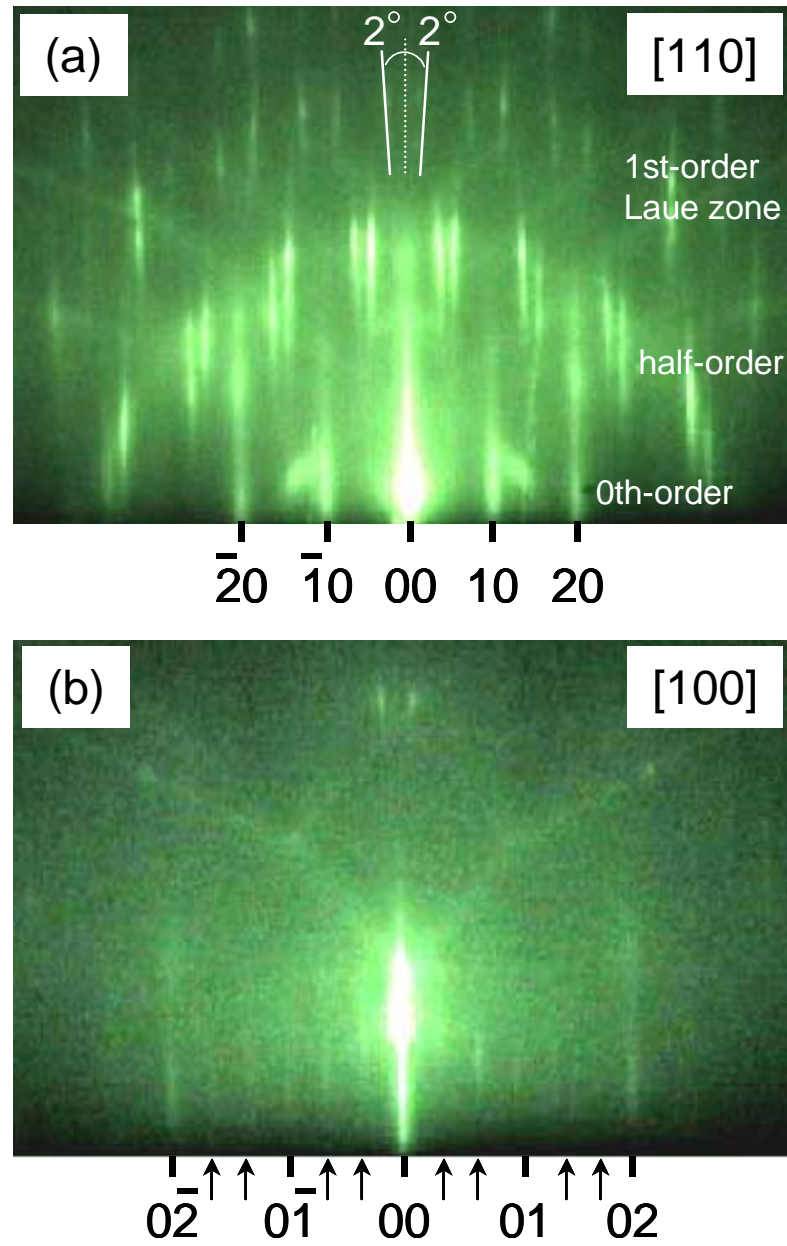[30] W. A. Harrison, E. A. Kraut, J. R. Waldrop, R. W. Grant, Phys. Rev., 18(1978)4402.

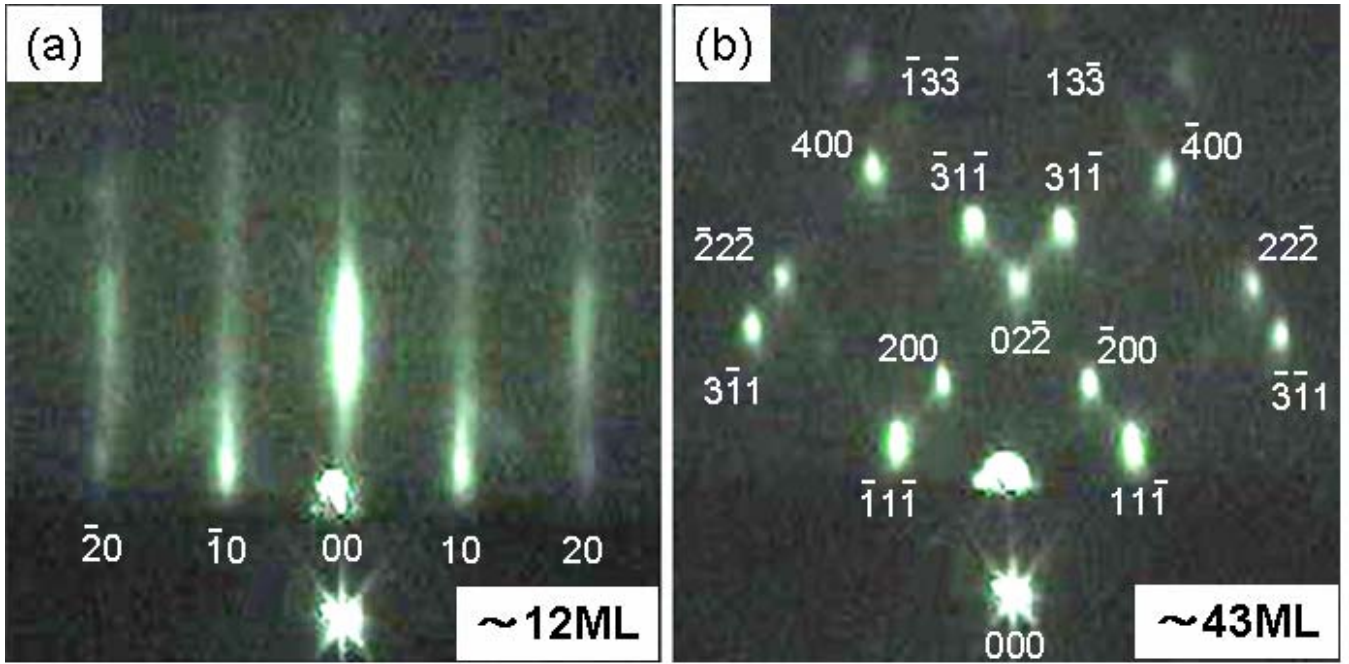Fig.1 RHEED patterns taken from Si(110) surface, (a) <110> incidence azimuth, (b) <100> incidence azimuth.

Fig.2. Successive stages of GaAs layer growth at 773K shown by RHEED patterns in the <110> incidence azimuth, (a) after approximately 12 ML deposition, (b) after approximately 43 ML deposition.
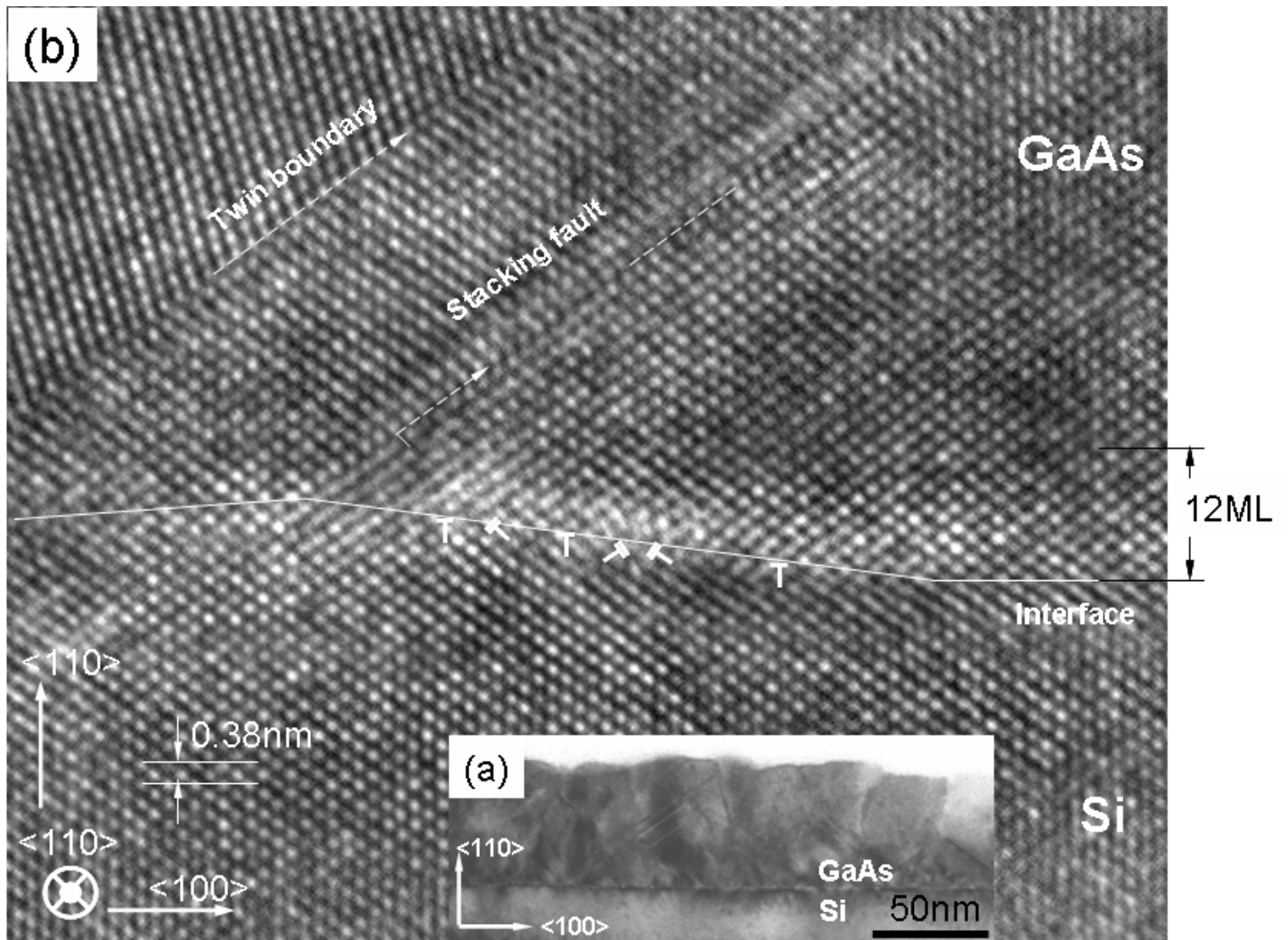
Fig.3 Cross-sectional TEM images of GaAs/Si(110) interface with (a) low magnification and (b) high magnification. The white solid line indicates the boundary plane between GaAs layer and Si. The mixed and pure edge dislocations are indicated with ⊥ and ⊥, respectively.