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Enhancement of ballistic efficiency due to source to channel heterojunction barrier in Si metal oxide semiconductor field effect transistors

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In this paper, we study the influences of a channel source-end potential profile on the ballistic transport of carriers in Si metal oxide semiconductor field effect transistors (MOSFETs) based on a quantum-corrected Monte Carlo device simulation. As a result, we found that higher ballistic efficiency is expected in MOSFETs with a heterojunction bottleneck barrier, such as Schottky source/drain MOSFETs, compared to that with the conventional *p-n* junction source and drain. Such a superior ballistic behavior is demonstrated due to the narrower bottleneck potential profile formed at the source-channel interface. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3186028]

I. INTRODUCTION

Schottky source/drain (S/D) technologies in metal oxide semiconductor field effect transistors (MOSFETs) replace S/D impurity doping with metal, typically silicide. There are numerous motivations for Schottky S/D MOSFETs, including low parasitic S/D resistance, increased immunity to process variation due to the elimination of S/D dopants, and inherent physical scalability to sub-10-nm gate-length dimensions due to the low resistance of metal and the atomically abrupt junctions at the silicide-silicon interface.[1,2] Despite the geometric similarities, the Schottky S/D MOSFET and the conventional *p-n* junction S/D MOSFET have very different physical behaviors, as shown in Fig. 1,[3] where typical potential profiles along the channel for (a) a *p-n* junction S/D MOSFET and (b) a Schottky S/D MOSFET at high gate voltages are illustrated. In the Schottky S/D MOSFETs, carrier flow from the source to the conduction channel takes place mainly by tunneling through the Schottky barrier at the metal-silicon interface. The width of the barrier is spatially modulated by the gate voltage, and tunneling injection occurs when the barrier is sufficiently thin.

Furthermore, it should be noted that the length of the so-called "*kT*-layer"[4,5] (the distance over which the channel potential energy drops by *kT* compared to the maximum value of the source to channel bottleneck barrier) is smaller for the Schottky S/D than for the *p-n* junction S/D due to the abruptness of the Schottky barrier, as shown in Fig. 1. Since the *kT*-layer length represents the critical distance over which carriers are backscattered to the source, a lower backscattering coefficient is expected in the Schottky S/D MOSFETs. Furthermore, the narrower bottleneck profile helps achieve ballistic current since the backscattering is suppressed due to energy relaxation induced by the inelastic phonon emission processes.[6–8] Therefore, the Schottky S/D architecture is considered to be one of the promising candidates to enhance the ballistic efficiency.

As described above, the source to channel heterojunction barrier plays an important role on the ballistic transport of carriers in Schottky S/D MOSFETs. Then, we theoretically study the influences of the heterojunction bottleneck barrier on the carrier transport in MOSFETs based on a quantum-corrected Monte Carlo device simulation.

II. DEVICE MODEL AND COMPUTATIONAL METHOD

The device model used in this study is shown in Fig. 2, where the S/D conduction band offset is formed by the electron affinity difference between the S/D and the channel regions.[9] In other words, the source is a smaller bandgap semiconductor injecting electrons into a larger bandgap semiconductor. In the present simulations, the electron affinity of S/D electrodes, χ_{SD}, was varied from 4.20 to 4.45 eV, but other physical parameters of the electrodes, such as effective mass, dielectric constant, Fermi energy, and scattering probability, were assumed to be the same as those of Si; also, the doping density was set to be a typical value of

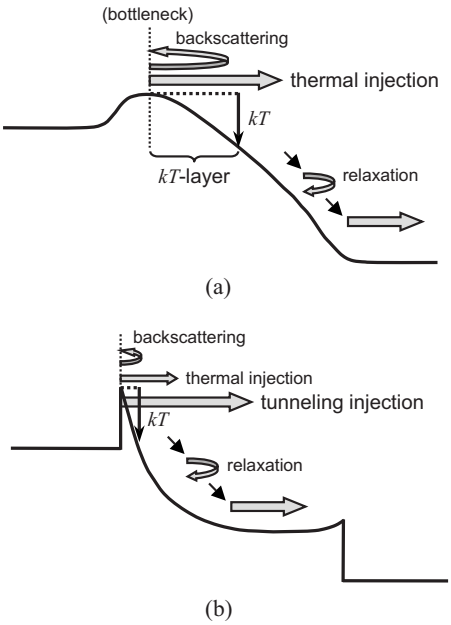

FIG. 1. Typical potential profiles along channel for (a) *p-n* junction S/D MOSFET and (b) Schottky S/D MOSFET at high gate voltages. In Schottky S/D MOSFET, narrower *kT*-layer is expected.

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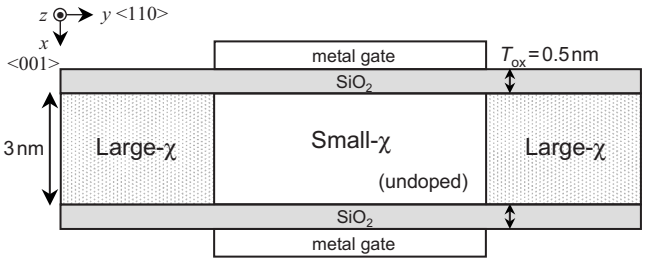


FIG. 2. Device model investigated in this study. The S/D regions are assumed to be silicon with electron affinity larger than that of ordinary silicon.

doped Si electrodes, which is 10^{20} cm^{-3}. This is to directly identify the effects of the source-end heterobarrier on the ballistic transport of carriers. Since the affinity of a Si channel is assumed to be 4.15 eV, the barrier height $\Delta\varphi$ is varied from 0.05 to 0.3 eV. In addition, the double-gate structure with an ultrathin body Si channel was employed so that the carrier's ballistic transport can be well articulated under perfectly controlled gate electrostatics even in a 10 nm order of channel lengths. Further, surface roughness scattering associated with a fluctuation in the subband energy profiles in the ultrathin body structure[10] was not considered, assuming perfect interfaces, because the purpose of this paper is to analyze the influences of the spatially dependent source-end potential in ideal conditions. Since surface roughness scattering is an elastic process as in acoustic phonon scattering and is supposed to affect equally on the heterojunction S/D and *p-n* junction S/D devices, the conclusion will not change even in the presence of surface roughness scattering.

The electrical characteristics were computed using the Monte Carlo device simulator with quantum mechanical correction (MONAQO) developed at Kobe University.[8,11–13] In this method, the equations of motion for particles in free flight are given as

$$\frac{d\mathbf{r}}{dt} = \mathbf{v}, \tag{1}$$

$$\frac{d\mathbf{k}}{dt} = -\frac{1}{\hbar}\nabla(U + U_\nu^{qc}), \tag{2}$$

where the quantum correction of the potential U_ν^{qc} is represented as[8,11–13]

$$U_\nu^{qc} = -\frac{\hbar^2}{12m_x^\nu}\frac{\partial^2 \ln(n_\nu)}{\partial x^2} - \frac{\hbar^2}{12m_y^\nu}\frac{\partial^2 \ln(n_\nu)}{\partial y^2}. \tag{3}$$

We considered the six equivalent conduction band valleys ($\nu = 1, 2, \ldots, 6$) around the X point in the Brillouin zone. n_ν represents the carrier density, and m_x^ν and m_y^ν are the effective masses of the ellipsoidal band structure. It has been demonstrated that quantized subbands in the inversion layer and S/D tunneling can be incorporated by considering the quantum correction of potential U_ν^{qc} in Eq. (3).[12–14] We have also confirmed that tunneling injection through the heterobarrier is represented with this approach. In this study, we further considered the image potential from S/D electrodes, so that the present model calculation mimics Schottky S/D MOSFETs. For scattering processes, we considered intravalley acoustic phonon, intervalley phonon, and impurity scatterings. In the S/D electrodes, plasmon scattering was also included to activate the rapid decay of hot electrons.[8] Surface roughness scattering was not included as mentioned before.

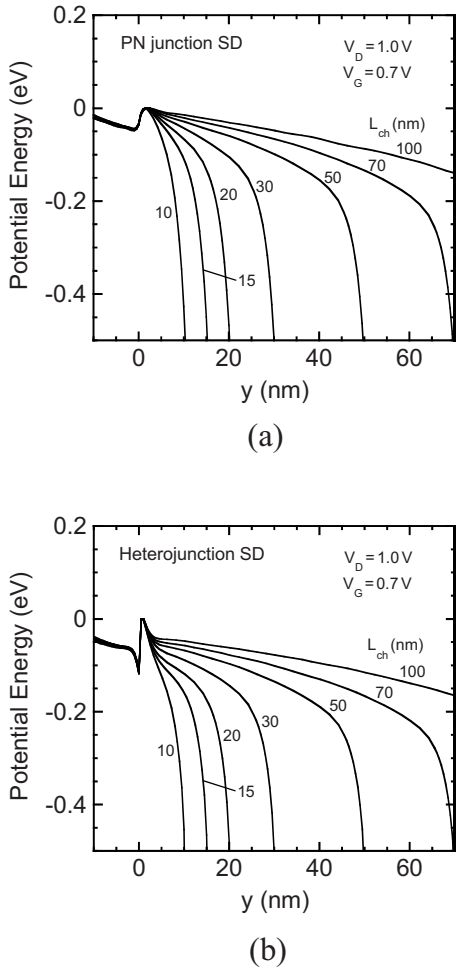


FIG. 3. Potential energy profiles for (a) *p-n* junction S/D and (b) heterojunction S/D MOSFETs along the channel direction computed for various channel lengths at V_D=1.0 V and V_G=0.7 V. The metallurgical junction between source and channel is located at y=0, and the potential maximum of source to channel barrier is set to be zero in the vertical axis. Note that the image potential energy is soundly taken into account in (b).

III. COMPUTED RESULTS

First, we compare the potential profiles along the channel direction computed for *p-n* junction S/D and heterojunction S/D MOSFETs with χ_{SD}=4.35 eV, which corresponds to $\Delta\varphi$=0.2 eV (NiSi), as shown in Fig. 3. The plotted potentials are averaged over the carrier density in the vertical direction. The channel length is varied from 100 to 10 nm. Here, note that the image potential energy is included in Fig. 3(b), and therefore the barrier height is smaller than $\Delta\varphi$ =0.2 eV. It is found that a narrower kT-layer is actually formed in the heterojunction S/D MOSFETs at this high gate voltage, so an improved ballistic transport due to the reduced kT-layer[8] is expected.

To estimate the ballistic parameters such as ballistic efficiency and backscattering coefficient, we computed the I_D-V_G characteristics *with* and *without* the scattering pro-

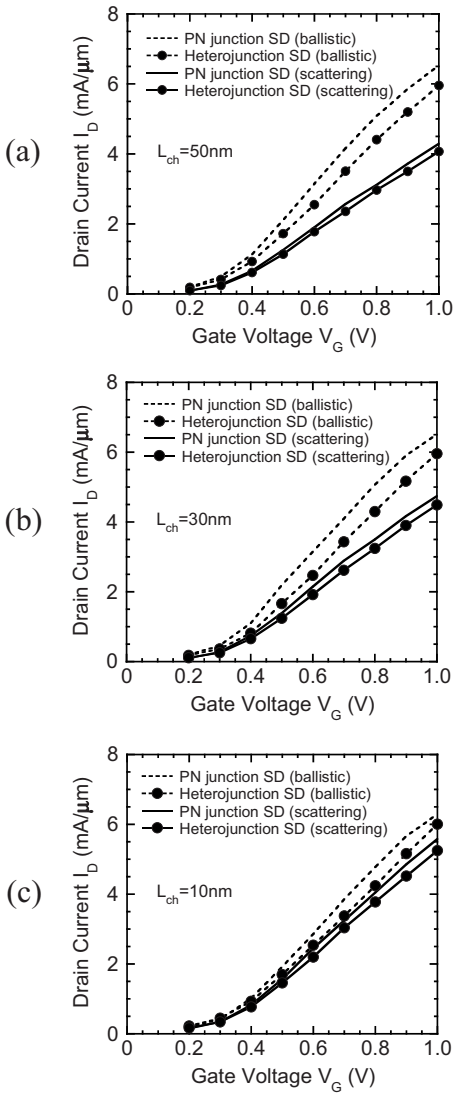


FIG. 4. I_D-V_G characteristics computed for *p-n* junction S/D and heterojunction S/D MOSFETs at $V_D=1.0$ V, where (a) $L_{ch}=50$ nm, (b) 30 nm, and (c) 10 nm, and V_{th} is set at 0.3 V. Ballistic I_D-V_G characteristics are also plotted in the dashed lines.

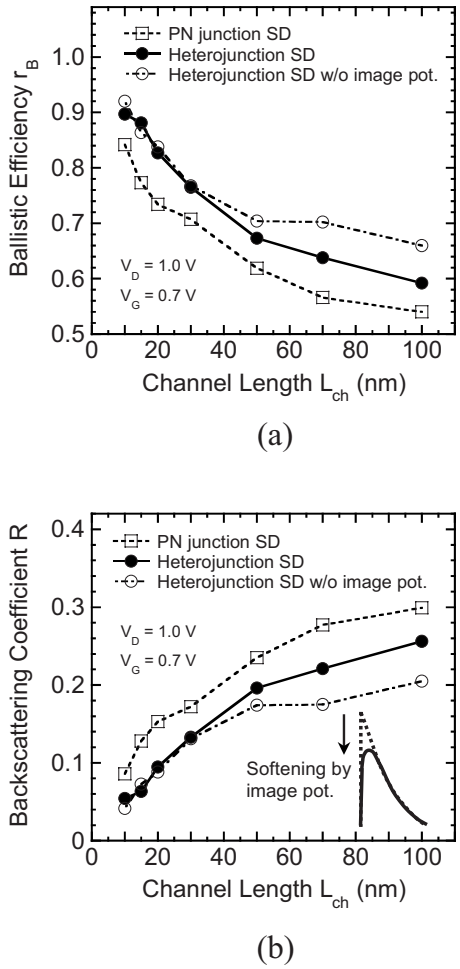


FIG. 5. (a) Ballistic efficiency and (b) backscattering coefficient computed as a function of channel length at $V_D=1.0$ V and $V_G=0.7$ V, where results without image potential are also plotted. The inset in (b) represents the Schottky barrier softening by image potential.

cesses in the channel, as shown in the solid and the dashed lines of Fig. 4, respectively. The channel length L_{ch} are given as (a) 50 nm, (b) 30 nm, and (c) 10 nm. Due to the presence of the source-end heterobarrier, the drain currents in the heterojunction S/D MOSFETs are always smaller, but the subequal currents to the *p-n* junction S/D MOSFETs are obtained, especially when the scatterings are included. This is due to the consideration of the tunneling injection process and the higher ballistic efficiency presented later. Further, we notice that the drain current increases as the channel length reduces when the scatterings are included, which is due to the ballistic transport effects, as previously reported by several researchers.[11,15–17] On the other hand, the I_D-V_G characteristics at the ballistic limit, denoted in the dashed lines, are independent of the channel length for both devices. This demonstrates that the short channel effects are well suppressed until the channel length is scaled down to the 10 nm scale.

By using the solid and the dashed lines shown in Fig. 4, we can evaluate the ballistic efficiency r_B and the backscattering coefficient R by using the relation of $r_B = I(\text{scattering})/I(\text{ballistic}) = (1-R)/(1+R)$.[4] Although the above relationships are approximate and, in principle, the backscattering coefficient is extracted directly by counting the fraction of injected electrons, which are backscattered to the source, we employed the present approach here to coincide with the experimental extraction method of ballistic parameters.[18] We are interested in a comparison with the direct counting of backscattering electrons, which is worth the ensuing research project. The computed results are shown in Fig. 5, where (a) ballistic efficiency and (b) backscattering coefficient are computed as functions of the channel length. Note that the results without an image potential are also plotted. It is found that higher ballistic efficiency and lower backscattering coefficient are obtained in the heterojunction S/D MOSFETs for the whole channel length. Here, it is noteworthy that the image potential softens the heterojunction barrier profile, as schematically shown in the inset of Fig. 5(b), so the critical length for the backscattered carriers increases compared to the case without an image potential. Therefore, the ballistic properties are degraded by considering the image potential from S/D electrodes, as shown

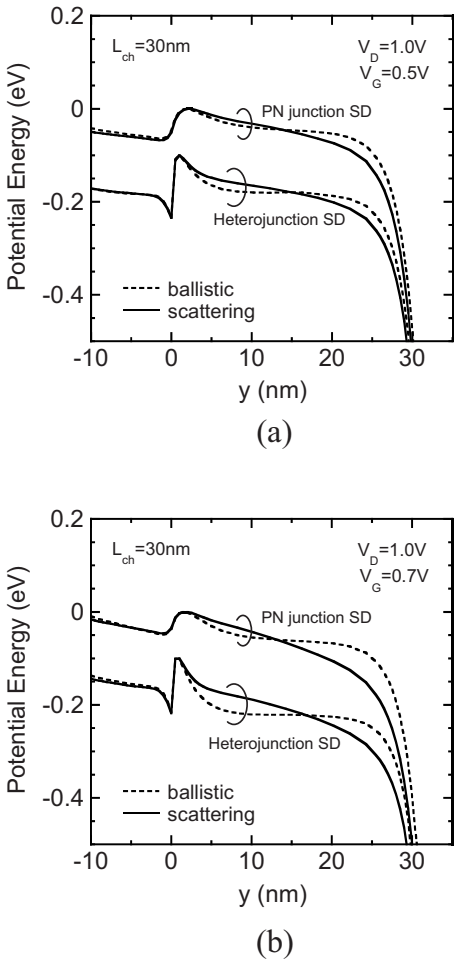


FIG. 6. Potential energy distributions computed for *p-n* junction and heterojunction S/D MOSFETs with and without scattering processes in the channel, where L_{ch}=30 nm, and (a) and (b) correspond to V_G=0.5 and 0.7 V, respectively. The potential distributions for the heterojunction S/D device are shifted downward by 0.1 eV for clarity.

in Fig. 5. Nonetheless, we can emphasize that the heterojunction S/D architecture offers a superior ballistic transport than the *p-n* junction S/D architecture, as confirmed in Fig. 5.

Here, we have to add that the ballistic properties reported in this study are essentially determined by the carrier transport inside the channel, hardly affected by the carrier transport in the source where there exists a non-negligible electric field, as shown in Fig. 3. In fact, the potential distributions for the *p-n* junction and the heterojunction S/D devices with and without the scattering processes in the channel are shown in Fig. 6, where (a) and (b) correspond to V_G=0.5 and 0.7 V, respectively. The channel length is 30 nm. It is found that the channel potentials are greatly modified by the scatterings, while the source potentials are almost unchanged. We obtained the same results for all the other gate biases and channel lengths. The above results mean that the carrier injection process into the channel is hardly affected by the scatterings inside the channel, and therefore the evaluated ballistic parameters represent the ballistic transport properties of the channel. We also need to point out that an *effective* electric field that electrons feel before the channel in the heterojunction S/D devices is modified to yield a normal electric field due to the quantum correction of potential U^{qc},

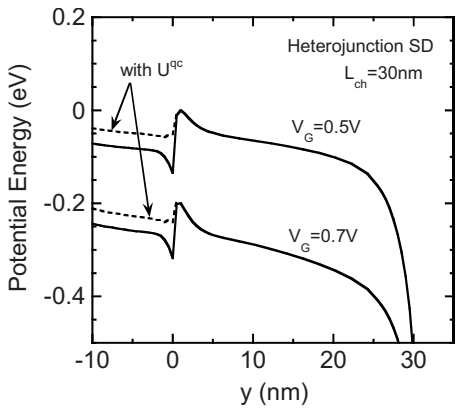


FIG. 7. Potential energy distributions for heterojunction S/D MOSFET with scattering in the channel. The effective potential energies including U^{qc} in the source region are plotted in the dashed lines both for V_G=0.5 and 0.7 V. The potential distribution for V_G=0.7 V is shifted downward by 0.2 eV for clarity.

as shown in Fig. 7,[14] where the effective potential energies including U^{qc} in the source region are plotted in the dashed lines both for V_G=0.5 and 0.7 V. Therefore, there is no significant difference in the carrier injection processes from the source between the *p-n* junction S/D and the heterojunction S/D devices in the present quantum-corrected simulation.

Next, we computed the gate bias dependences of the backscattering coefficient for L_{ch}=100, 30, and 10 nm, as shown in Fig. 8, where the lower backscattering coefficients are obtained in the heterojunction S/D devices even when the gate bias voltage increases. It is interesting to note that the backscattering coefficients indicate a slight decreasing trend as a function of the gate voltage. To clarify its origin, we plotted the magnified profiles of the potentials at the source-channel junction, as shown in Fig. 9, where L_{ch}=100 nm and the results for V_G=0.5, 0.6, 0.7, and 0.8 V are plotted for both devices. It is clearly found that the potential gradient of the bottleneck barrier increases with gate voltage, and then the *kT*-layer length becomes shorter. This *kT*-layer narrowing reduces backscattering, and the backscattering coefficient decreases as a function of the gate voltage, as shown in Fig. 8.

We further investigated the barrier height $\Delta\varphi$ dependences of ballistic behaviors. Figure 10 shows the $\Delta\varphi$ dependences of (a) the backscattering coefficient and (b) the drain

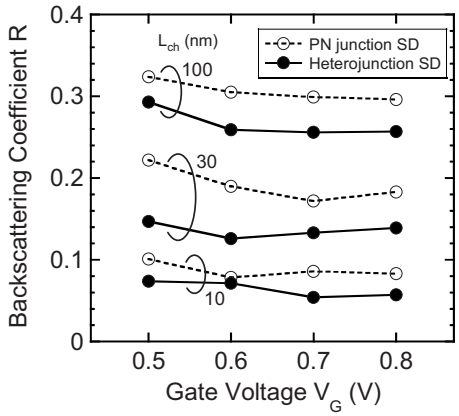


FIG. 8. Gate bias dependences of backscattering coefficient for L_{ch}=100, 30, and 10 nm at V_D=1.0 V.

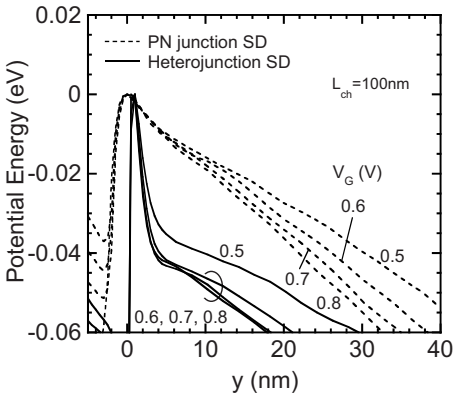
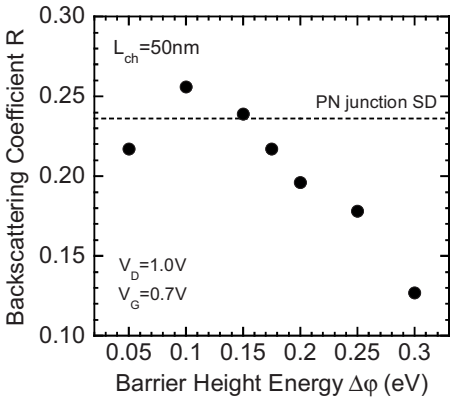
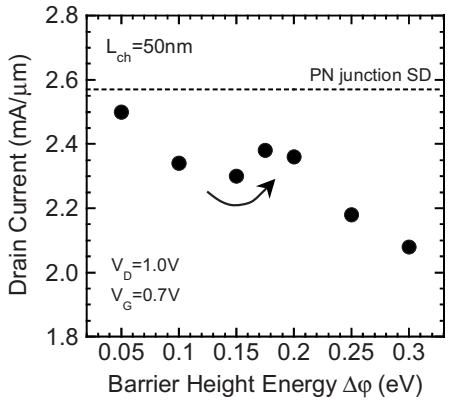


FIG. 9. Gate bias dependences of potential distributions at source-channel junction, where L_{ch}=100 nm and V_D=1.0 V, and the results for V_G=0.5, 0.6, 0.7, and 0.8 V are plotted for both devices. The potential maximum of source to channel barrier is set to be zero in the vertical axis.

current, where L_{ch}=50 nm, V_D=1.0 V, and V_G=0.7 V. For reference, the values for the corresponding *p-n* junction S/D MOSFET are indicated by the horizontal dashed lines. First, the backscattering coefficient is found to be nearly equal to that of the *p-n* junction SD until $\Delta\varphi \approx 0.15$ eV, and then it monotonously decreases with $\Delta\varphi$. This suggests that the barrier height larger than 0.15 eV is needed to enhance the ballistic transport in the present device. Such a barrier height dependence of the backscattering coefficient is qualitatively explained in terms of the *kT*-layer narrowing with increasing $\Delta\varphi$, of which potential distributions are shown in Fig. 11, where (a) $\Delta\varphi$=0.10 eV, (b) $\Delta\varphi$=0.175 eV, and (c) $\Delta\varphi$=0.25 eV. Note that the potential distribution for the corresponding *p-n* junction S/D is also plotted in the dashed lines for comparison. We can confirm that the source-end *kT*-layer becomes narrower as the barrier height increases, and the Schottky-like potential profile is formed in Figs. 11(b) and 11(c). Due to this *kT*-layer narrowing, the backscattering coefficient decreases with $\Delta\varphi$ for the barrier height larger than 0.15 eV. Interestingly, as shown in Fig. 10(b), such a backscattering suppression due to the narrower *kT*-layer induces the drain current increase around $\Delta\varphi$=0.175 eV, on the decreasing trend of the current with $\Delta\varphi$. Although the maximum drain current is still smaller than that of the *p-n* junction S/D MOSFET, the introduction of real metal S/D and dopant-segregated technique will be able to outperform the counterpart MOSFETs in terms of drive current capability.



(a)



(b)

FIG. 10. Barrier height dependences of (a) backscattering coefficient and (b) drain current for L_{ch}=50 nm, where bias conditions are given as V_D=1.0 V and V_G=0.7 V. The horizontal dashed lines denote the values for the corresponding *p-n* junction S/D MOSFET.

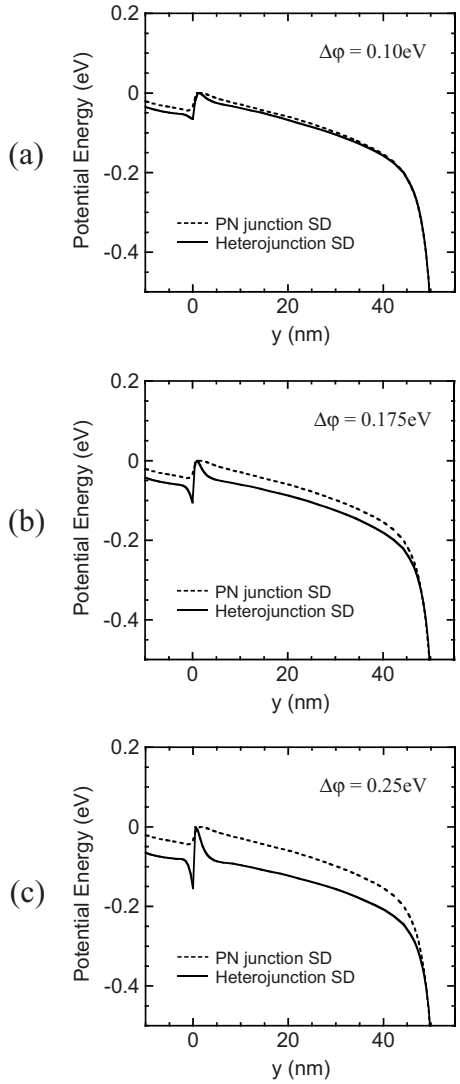


FIG. 11. Potential energy distributions computed for heterojunction barrier heights of (a) $\Delta\varphi$=0.10 eV, (b) $\Delta\varphi$=0.175 eV, and (c) $\Delta\varphi$=0.25 eV. The dashed line represents the result for the corresponding *p-n* junction S/D MOSFET. L_{ch}=50 nm, V_D=1.0 V, and V_G=0.7 V. The potential maximum of source to channel barrier is set to be zero in the vertical axis.

IV. CONCLUSION

We have studied the influences of the source to channel heterojunction barrier on the ballistic transport of carriers in Si MOSFETs based on the quantum-corrected Monte Carlo device simulation. As a result, we found that the ballistic efficiency is enhanced due to the narrower bottleneck barrier formed in the heterojunction S/D MOSFETs, as compared with the conventional *p-n* junction S/D MOSFETs. We also demonstrated that a certain amount of barrier height, which is larger than 0.15 eV in the present model calculation, is needed to narrow the source-end *kT*-layer and enhance the ballistic efficiency. Such a relatively large barrier height may reduce the drain current, and thus an optimum device design introducing metal S/D electrodes with low parasitic S/D resistance and dopant-segregated Schottky S/D technique will actually be necessary.

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