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# Comparative Study on Drive Current of III-V Semiconductor, Ge and Si Channel n-MOSFETs based on Quantum-Corrected Monte Carlo Simulation

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***Abstract*—Recently, a variety of new channel materials have been intensively studied to achieve a continuous enhancement in drive current of *n*-channel MOSFETs. In this paper, we performed a quantum-corrected Monte Carlo device simulation to examine advantages of new channel materials such as III-V compound semiconductors and Ge, by considering scattering effects, quantum mechanical effects and new device structure. Then, we found that all materials converge to the similar current level as the channel length decreases, but Ge-MOSFET with (111) surface orientation and InP MOSFET provide higher drive current than the other materials under the quasi-ballistic transport. Furthermore, we demonstrated that the reduction of parasitic resistance in source and drain regions will be indispensable to maintain a definite advantage of III-V materials.**

***Index Terms*—Drive current, high mobility channel materials, nanoscale MOSFETs, quantum-corrected Monte Carlo simulation, ballistic transport**

## I. Introduction

For almost forty years, the progress of LSI technology has been based on downsizing of MOSFETs, because the downsizing has been the most effective way to improve the LSI circuit performance. But, in the present post-scaling technology, the downsizing is becoming not effective to improve the device performance, because we need to suppress leakage current, minimize short channel effects, and maintain high drive current at the same time. To meet these requirements, the application of technology boosters such as new channel materials, multi-gate architectures and quasi-ballistic transport is highly expected [1]. There are two main directions for such a technology innovation. One is the introduction of new device structures. For example, ultrathin-body structure and multi-gate architecture are investigated, which are considered to be effective to suppress the short channel effect. The other is the application of new channel materials. For *p*-channel MOSFETs, (110) surface orientation, uni-axial compressive strain and even Ge channels have been proposed. On the other hand, for *n*-channel MOSFETs few promising concepts have been proposed since the tensile strain has been successfully introduced [2].

Under the circumstances, the application of III-V compound semiconductors to the Si platform has been intensively studied to achieve a drive current enhancement of *n*-channel MOSFETs, because III-V compound semiconductors such as GaAs and InP have quite higher electron mobility than Si and Ge. The recently reported theoretical analyses on these new materials have been based on a perfect ballistic transport for bulk [2] and double-gate [3, 4] MOSFETs. However, the scattering effects are still important in such new channel materials, for instance, as expected from the Gunn effect in GaAs, which is caused by electron transfer to higher valleys with heavier transport effective mass due to the phonon scattering. So, in this study we performed a quantum-corrected Monte Carlo device simulation to examine advantages of the new channel materials by considering scattering effects, quantum mechanical effects and new device structure.

## II. Simulation model

Fig. 1 shows the device model used in this study, where ultrathin-body (UTB) structure with $T_{Si}$ = 5nm is employed. When the high mobility materials are introduced into the channel, the usage of the UTB structure is required to minimize the short channel effects because electron wave-functions spread deeply into the substrate region due to the small effective mass [2]. The advantage of the UTB structure will be discussed later. The UTB channels are formed onto the $SiO_2$ layer and the bottom substrate is assumed to be Si. The surface orientation is (100) for Si, GaAs and InP, and (100) and (111) for Ge, because the smaller transport effective mass is expected for Ge (111) surface orientation [5]. The channel direction is taken as <110> and the channel length $L_{ch}$ is varied from 70 to 20nm, where the channel region is assumed to be undoped.

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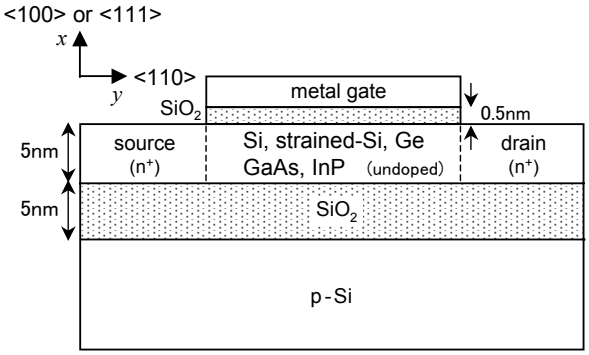


Fig. 1. Device model used in the simulation, where ultrathin-body (UTB) structure is employed. The channel length $L_{ch}$ is varied from 70 to 20nm, and the channel region is assumed to be undoped.

TABLE I. Effective masses and valleys used in the simulation. Fermi levels in III-V materials are a few hundreds meV, which is much higher than that of Si [6].

| | | Si | Ge | GaAs | InP |
|---|---|---|---|---|---|
| mass (Γ) | | – | 0.037 | 0.067 | 0.082 |
| mass (X) | $m_t$ ($m_0$) | 0.19 | 0.29 | – | – |
| | $m_l$ ($m_0$) | 0.98 | 1.35 | – | – |
| mass (L) | $m_t$ ($m_0$) | – | 0.082 | 0.127 | 0.153 |
| | $m_l$ ($m_0$) | – | 1.59 | 1.538 | 1.878 |
| nonparabolicity $\alpha$ | | 0.5 (X) | 0.65 (L, Γ, X) | 0.61 (Γ) 0.46 (L) | 0.61 (Γ) 0.49 (L) |
| $\Delta E_{\Gamma L}$ (eV) | | – | – | 0.33 | 1.492 |
| $\Delta E_{L\Gamma}$ / $\Delta E_{LX}$ (eV) | | – | 0.14 / 0.18 | – | – |
| permittivity $\varepsilon_r$ | | 11.9 | 16.0 | 12.9 | 12.6 |
| $E_f$ of S/D (eV) | | 0.064 | 0.138 | 0.278 | 0.326 |

Here, we should pay attention to the physical limits of solid solubility of donors in III-V semiconductors. Namely, activated donor concentrations larger than $2\times10^{19}$ cm$^{-3}$ cannot be obtained in III-V semiconductors [6]. So, in this study the donor concentration of $2\times10^{19}$ cm$^{-3}$ was assumed in the source and drain (S/D) regions for GaAs and InP, while a higher donor concentration of $1\times10^{20}$ cm$^{-3}$ was used for Si and Ge.

The electrical characteristics were computed by using a quantum-corrected Monte Carlo (MC) method proposed by the authors [7, 8]. This method can simulate the quantized subbands in the inversion-layer and also consider scattering effects, so it has been successfully applied to an analysis of quasi-ballistic transport of Si-MOSFETs [9]. In the quantum-corrected Monte Carlo method, carriers are evolved under both the classical built-in potential $U$ and quantum correction of potential $U_v^{QC}$ as follows.

$$\frac{d\mathbf{r}}{dt}=\mathbf{v},\quad \frac{d\mathbf{k}}{dt}=-\frac{1}{\hbar}\nabla_{\mathbf{r}}\left(U+U_v^{QC}\right). \tag{1}$$

For the two-dimensional device structure shown in Fig. 1, the $U_v^{QC}$ is given by

$$U_v^{QC}=-\frac{\hbar^2}{12m_x^v}\frac{\partial^2\ln(n_v)}{\partial x^2}-\frac{\hbar^2}{12m_y^v}\frac{\partial^2\ln(n_v)}{\partial y^2}\ , \tag{2}$$

where the superscript $v$ denotes the valley numbers of the material's bandstructures and $n_v$ the carrier density distribution, and $m_x^v$ and $m_y^v$ the effective masses in each direction. The first term in the right-hand side of eq. (2) represents the quantum confinement in the $x$-direction, and the second one the source-drain tunneling in the $y$-direction. In this study, we extended the quantum-corrected MC method to III-V compound semiconductors and Ge.

Table 1 shows the effective masses and the valley information used in the simulation. As pointed out by S. Takagi [2], the energy differences between the lowest and higher valleys as $\Delta E_{\Gamma L}$ and $\Delta E_{LX}$ are important physical parameters in the new channel materials, because an electron transfer to the higher valleys, which usually have a heavier transport effective mass, degrades the device performance significantly. For the strained-Si device, a bi-axially 1% tensile strain is assumed to be applied in both the channel and S/D regions. The band edge energy variations due to the bi-axial strain with $x$ % was given by $\Delta E_{2f}$=-0.66$x$ (eV) and $\Delta E_{4f}$=0.86$x$ (eV) for the 2-fold and 4-fold valleys, respectively, which was derived in our laboratory by using the first-principles calculation for bulk Si. In this study, the scattering processes considered are impurity and phonon scatterings, where polar optical phonon scattering is also considered for GaAs and InP. The phonon scattering parameters are taken from [10] for Si, [11] for Ge, and [12] for GaAs and InP. The roughness and electron-electron scatterings are ignored in this study, to evaluate the device performances governed by the intrinsic transport properties of each material. The enhanced scattering probabilities due to the confinement of wave-functions are approximately considered by adding the quantum correction energy into the electron kinetic energy [9]. We also disregarded the X valley states in GaAs, because it is enough to include the Γ and L valleys to reproduce the Gunn effect in GaAs.

## III. Advantage of UTB Structure

First, we demonstrate the advantage of the UTB structure for the III-V MOSFETs. Fig. 2 shows the $I_D$ - $V_G$ characteristics computed for the bulk and UTB structures with Si and GaAs channels, where $L_{ch}$ = 50nm and threshold voltage $V_{th}$ is set at 0.3V. The drain voltage is given as 0.5V. For the bulk MOSFETs, the acceptor density in the substrate was given as $N_A=1\times10^{18}$ cm$^{-3}$ in the simulation. Although the acceptor in the

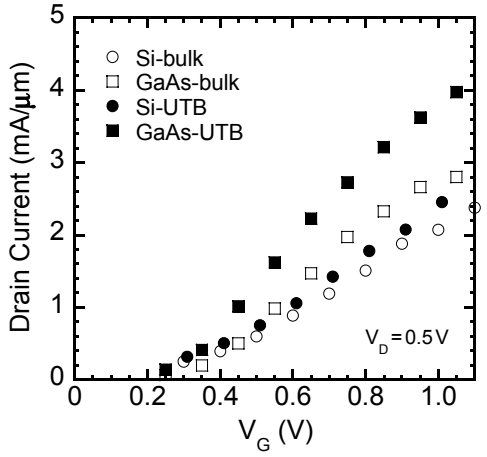


Fig. 2. $I_D$ - $V_G$ characteristics computed for bulk and UTB structures with Si and GaAs channels, where $L_{ch}$ = 50nm and $V_{th}$ is set at 0.3V. The drain voltage is given as 0.5V.

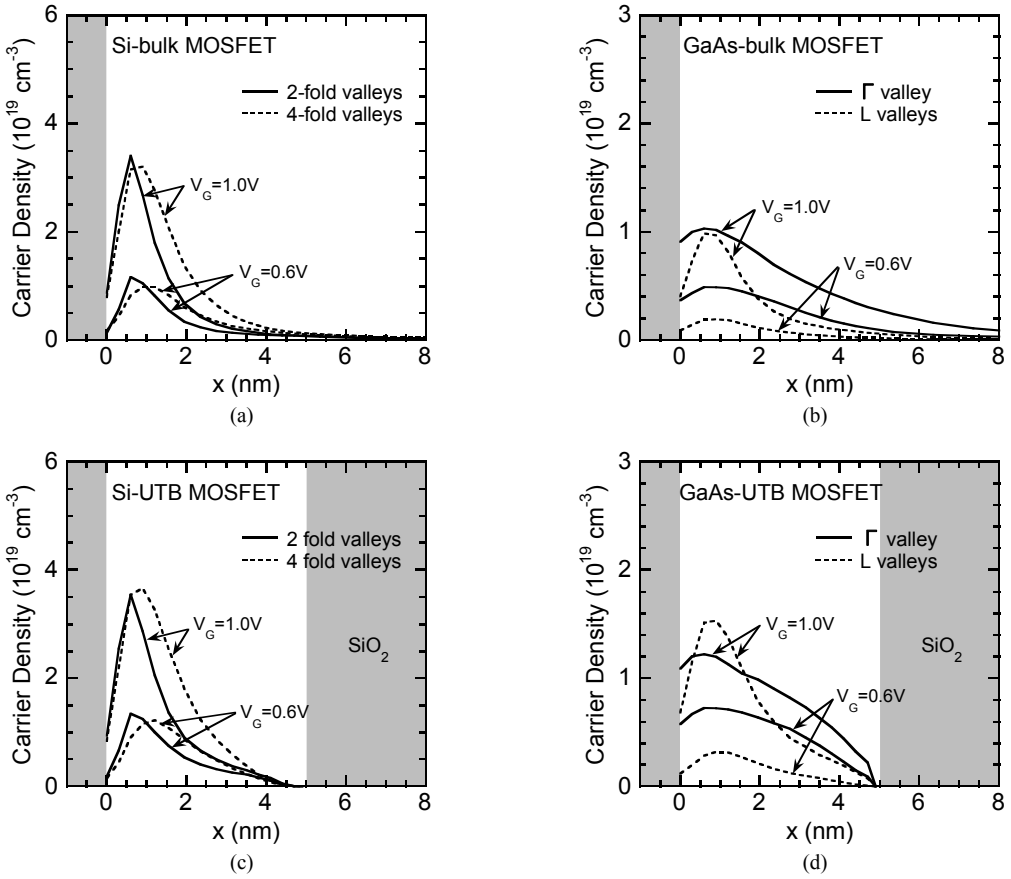


Fig. 3. Electron density distributions in the inversion-layers computed for bulk and UTB structures with Si and GaAs channels, where (a) Si-bulk, (b) GaAs-bulk, (c) Si-UTB and (d) GaAs-UTB MOSFETs. The distributions for each valley are separately plotted. The gate bias voltages are given as 0.6 and 1.0V, and the drain voltage is set at 0.5V. Note that these profiles are extracted in the middle of channel region.

substrate increases the threshold voltage, the impurity scattering due to the acceptor is considered to be negligible for the drive current estimation at on-state. From Fig. 2, it is found that the drive current enhancement in the GaAs channel is considerably improved by using the UTB structure. As predicted in [2], the performance improvement in the GaAs-UTB structure should be due to the smaller inversion-layer thickness, which is owing to the physical confinement of electron wave-functions. To demonstrate this, Fig. 3 shows the electron density distributions in the inversion-layers computed for each device structure, where the distributions for each valley are separately plotted. The gate bias voltages are given as 0.6 and 1.0V, and the drain voltage is set at 0.5V. Note that these distributions are extracted in the middle of channel, so the profiles are influenced by the applied drain voltage. As shown in Fig. 3 (b), the electrons in the Γ valley of the GaAs bulk MOSFET spread deeply into the substrate due to the quantum confinement effect, while those in the L valleys are confined within a few nm region from the $Si/SiO_2$ interface ($x = 0$). This is due to the difference in the effective masses between the Γ and L valleys in the confinement direction. Here, note that as the gate bias increases, more electrons occupy the L valleys in GaAs. This is due to the small $\Delta E_{\Gamma L}$ and also the preferential increase in the quantized subband energy of the Γ valley. This causes the saturation in the drain current as shown in Fig. 2 [2].

Compared to the bulk structure, the Γ valley electrons in the UTB structure are also confined in the ultrathin channel region by the buried oxide layer as shown in Fig. 3 (d). As a result, the inversion-layer thickness decreases and then the inversion-layer capacitance increases, which leads to the increase of gate capacitance in the UTB MOSFETs. Therefore, the drive current in the GaAs UTB MOSFET significantly enhances as shown in Fig. 2. The advantage of the UTB structure also applies to other III-V materials such as InP.

On the other hand, the electron density distributions in the Si channels are almost the same in the two structures as shown in Figs. 3 (a) and (c), because the inversion-layer thickness is less than 5nm for the present Si MOSFETs. The above results suggest that the UTB structure is indispensable to realize high performance III-V MOSFETs.

## IV. Drive Current of Each Channel Materials

Next, we compare the drive current of Si, strained-Si, Ge, GaAs and InP all with the UTB structure shown in Fig. 1. First, the inversion-layer electron density distributions computed for strained-Si, Ge (100), Ge (111) and InP are shown in Fig. 4, where the bias conditions are the same as in Fig. 3. For the InP channel, there is no electron population in the L valleys even at the high gate voltage, which is due to the large $\Delta E_{\Gamma L}$ shown in

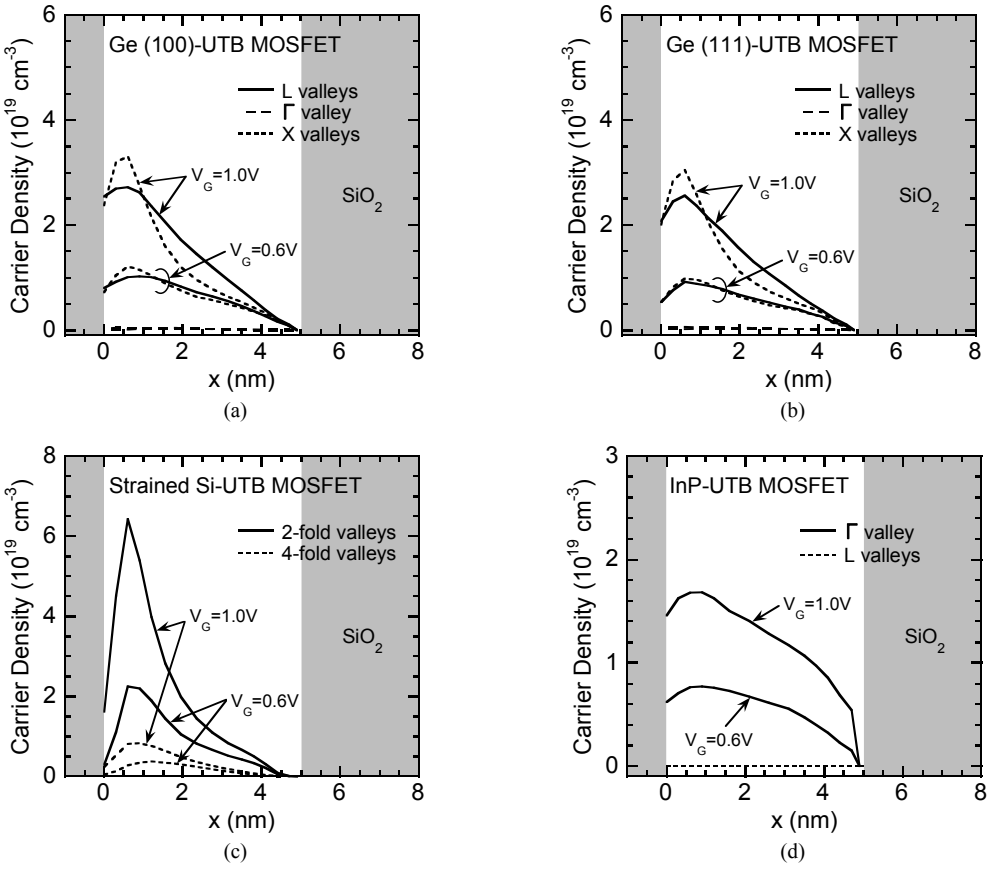


Fig. 4. Electron density distributions in the inversion-layers computed for (a) Ge (100), (b) Ge (111), (c) strained-Si and (d) InP with UTB structure. The bias conditions are the same as in Fig. 3.

Table 1. On the other hand, the Ge channels have the comparable electron populations in the L and X valleys for the both surface orientations, which is due to the much smaller $\Delta E_{LX}$ and more importantly, a high transition rate from the L to X valleys due to the inter-valley phonon scattering [13]. Furthermore, the electron population in the Γ valley of Ge is vanishingly small, because a much higher subband level is formed in the Γ valley due to the smaller effective mass shown in Table 1. For the strained-Si channel, the electron population in the 2-fold valleys is found to be dominant compared to the unstrained Si channel shown in Fig. 3 (c).

Fig. 5 shows the $I_D$ - $V_G$ characteristics computed for all channel materials, where the solid and the open symbols represent the group III-V and the group IV materials, respectively. $L_{ch}$ = 50nm and $V_{th}$ is set at 0.3V. It is found that the III-V materials provide higher on-current, $I_{ON}$, than the group IV materials in the present long channel devices. We also found that $I_{ON}$ of the Ge (111)-MOSFET is the highest among the group IV materials.

To understand the mechanism on such a large current enhancement in the III-V MOSFETs, we computed the averaged electron velocities and sheet electron densities as shown in Figs. 6 (a) and (b), respectively, where $V_G$ = 0.6V and $V_D$ = 0.5V, and the channel region extends from $y$ = 20 to 70nm. It is found that the III-V materials have about three times higher velocities than those of the group IV materials at the source-end of channel. On the other hand, the sheet electron density decreases to about a half of those in the group IV materials due to the S/D parasitic resistance, but it is not crucial owing to the UTB structure. As a result, the higher velocities effectively enhance $I_{ON}$ of the III-V long channel MOSFETs as shown in Fig. 5.

Here, we discuss on ultimate device performance at ballistic limit. We computed the $I_D$ - $V_G$ characteristics for perfectly

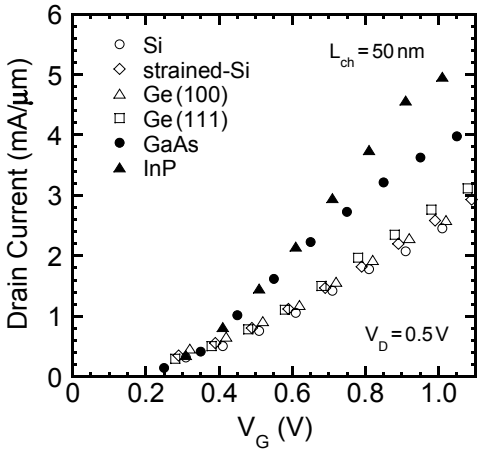


Fig. 5. $I_D$ - $V_G$ characteristics computed for all channel materials, where the solid and the open symbols represent the group III-V and the group IV materials, respectively. $L_{ch}$ = 50nm and $V_{th}$ is set at 0.3V.

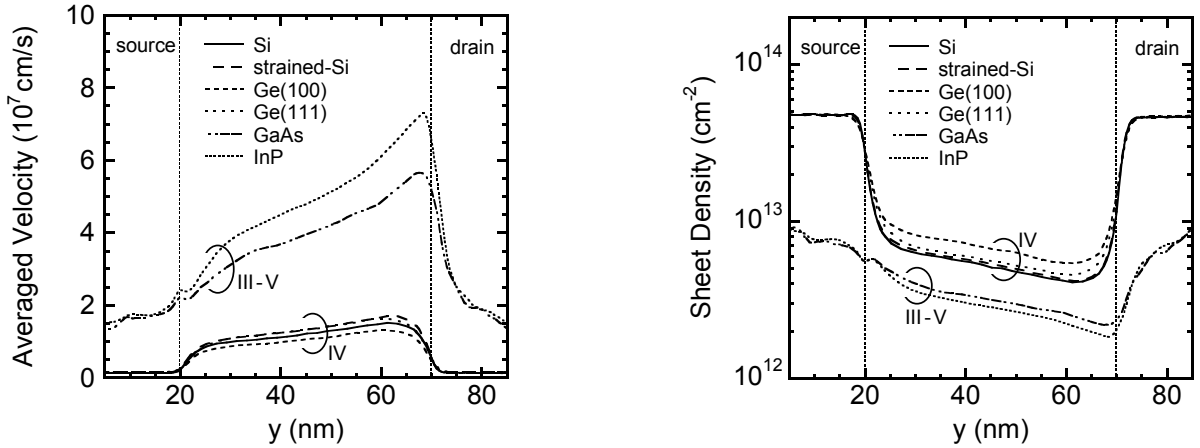


Fig. 6. (a) Averaged electron velocities and (b) sheet electron densities computed for all channel materials, where $V_G = 0.6$V and $V_D = 0.5$V. The channel region extends from $y = 20$ to 70nm.

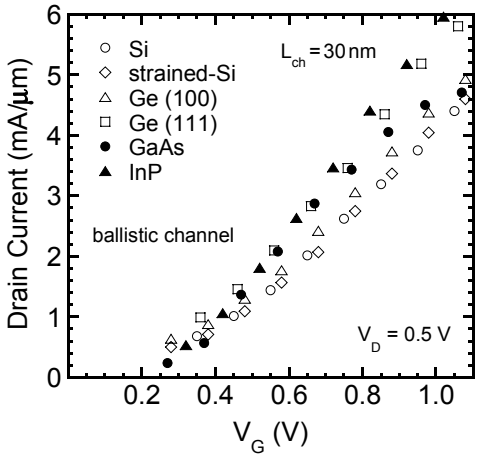


Fig. 7. $I_D$ - $V_G$ characteristics for perfectly ballistic MOSFETs, where all scattering processes in the channel region are ignored, while the scatterings in the source and drain are considered. $L_{ch} = 30$nm and $V_{th}$ is set at 0.3V.

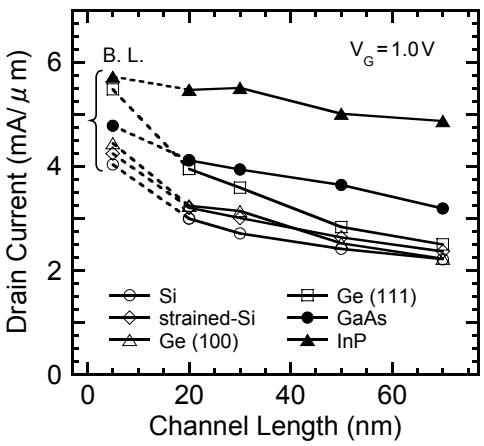


Fig. 8. Computed channel length dependences of $I_{ON}$ for all channel materials, where $V_G = 1.0$V. The current data computed from $L_{ch} = 70$ to 20 nm are plotted, and also the ballistic data are indicated on the extreme left as B. L.

ballistic MOSFETs as shown in the Fig. 7, where the "perfectly ballistic" means that all scattering processes in the channel region are ignored, while the scatterings in the S/D regions are considered. The channel length is taken as 30nm. From Fig. 7, the superiority of the III-V materials becomes smaller at the ballistic limit, though the higher $I_{ON}$ is still expected for the InP channel. To examine this ballistic behavior more in detail, we computed channel length dependences of $I_{ON}$ as shown in Fig. 8, where $V_G = 1.0$V. In Fig. 8, the current data computed from $L_{ch} =$ 70 to 20 nm are plotted, and also the ballistic limit data are indicated on the extreme left as B. L. First, it is found that the current enhancement due to the ballistic transport is more effective in the group IV materials than in the group III-V ones. Furthermore, it is interesting to note that in the long channel devices, the drain current depends on the channel materials, but all curves converge to the similar current level as the channel length becomes shorter. This result is essentially the same as previously reported in [6]. However, it is worth noting that the Ge (111)- and InP-MOSFETs provide substantially higher drive current than the Si and strained-Si MOSFETs under the quasi-ballistic transport. We have to mention that the electron-electron scattering, which was ignored in the present simulation, will not change the conclusion in essence, because the role of the electron-electron scattering should not be significantly different for the semiconductor materials considered here.

## V. Influence of S/D Parasitic Resistance in III-V MOSFETs

Finally, we investigated the influence of the donor concentration in the S/D regions for the III-V MOSFETs, where only the ballistic limit of $L_{ch} = 30$nm was considered. Fig. 9 shows the $I_D$ - $V_G$ characteristics computed for fictitious III-V MOSFETs with higher doped S/D as $1\times10^{20}$ $cm^{-3}$, where we assumed the same Fermi energies in the S/D electrodes as in Table 1, to examine the direct effects from the parasitic resistance. In Fig. 9, the results for the group IV materials are also plotted. Compared to Fig. 7, the drive current of the III-V MOSFETs is found to increase remarkably with the higher doped S/D, so the superiority of the III-V materials clearly remains even at the ballistic limit. Based on this result, we

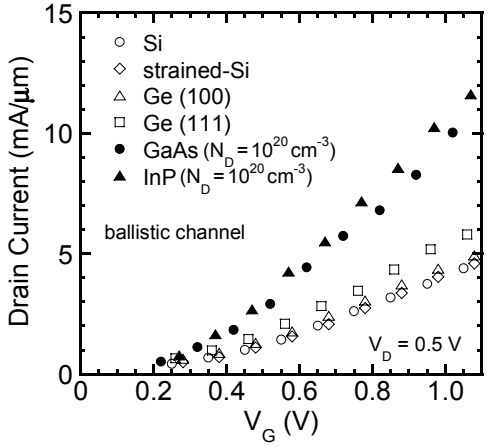


Fig. 9. $I_D$ - $V_G$ characteristics computed for fictitious III-V MOSFETs with higher doped source and drain as $1\times10^{20}$ cm$^{-3}$. $L_{ch}$ = 30nm and perfectly ballistic channel is assumed.

propose that a metal S/D and UTB III-V MOSFET can be one of the promising candidates for *n*-channel MOSFETs.

## VI. Conclusion

The quantum-corrected Monte Carlo device simulator has been successfully extended to emerging nano-MOS simulation with new channel materials. By using this simulator, we found that the drive current depends on the channel materials for long channel devices, but all materials converge to the similar current level at the ballistic limit. However, we also found that Ge (111)- and InP-MOSFETs provide substantially higher drive current than the Si and strained-Si MOSFETs under the quasi-ballistic transport. Moreover, a metal S/D and UTB III-V MOSFET has been proposed for an ultimate high performance device concept for *n*-channel MOSFETs.

## References

[1] http://www.itrs.net/

[2] S. Takagi and S. Sugahara, "Comparative study on influence of subband structures on electrical characteristics of III-V semiconductors, Ge and Si channel n-MISFETs," Extended Abstracts of Int'l Conf. on Solid State Devices and Materials (SSDM06), pp. 1056-1057, Yokohama, September 2006.

[3] A. Rahman, G. Klimeck, and M. Lundstrom, "Novel channel materials for ballistic nanoscale MOSFETs-bandstructure effects", Tech. Dig. of Int'l Electron Devices Meeting (IEDM2005), pp. 615-618, Washington, Dec. 2005.

[4] A. Pethe, T. Krishnamohan, D. Kim, S. Oh, H.-S. Philip Wong, Y. Nishi, and K. C. Saraswat, "Investigation of the performance limits of III-V double-gate n-MOSFETs", Tech. Dig. of Int'l Electron Devices Meeting (IEDM2005), pp. 619-622, Washington, Dec. 2005.

[5] S. Takagi, "Physical origin of drive current enhancement in ultra-thin Ge-On-Insulator (GOI) MOSFETs under full ballistic transport," Extended Abstracts of Int'l Conf. on Solid State Devices and Materials (SSDM04), pp. 10-11, Tokyo, September 2004.

[6] M. V. Fischetti and S. E. Laux, "Monte Carlo simulation of transport in technologically significant semiconductors of the diamond and zinc-blende structure–Part II: Submicrometer MOSFET's," IEEE Trans. on Electron Devices, vol. 38, no. 3, pp. 650-660, March 1991.

[7] H. Tsuchiya, M. Horino, M. Ogawa, and T. Miyoshi, "Quantum transport simulation of ultrathin and ultrashort silicon-on-insulator metal-oxide-semiconductor field-effect transistors," Jpn. J. Appl. Phys., vol. 42, no. 12, pp. 7238-7243, Dec. 2003.

[8] H. Tsuchiya, A. Oda, M. Ogawa, and T. Miyoshi, "Quantum-corrected Monte Carlo and molecular dynamics simulation on electron-density-dependent velocity saturation in silicon metal-oxide-semiconductor field-effect transistors," Jpn. J. Appl. Phys., vol. 44, no. 11, pp. 7820-7826, Nov. 2005.

[9] H. Tsuchiya, K. Fujii, T. Mori, and T. Miyoshi, "A quantum-corrected monte carlo study on quasi-ballistic transport in nanoscale MOSFETs," IEEE Trans. on Electron Devices, vol. 53, no. 12, pp. 2965-2971, Dec. 2006.

[10] C. Jacoboni and L. Reggiani, "The Monte Carlo method for the solution of charge transport in semiconductors with applications to covalent materials", Rev. Mod. Phys., vol. 55, no. 3, pp. 645-705, July 1983.

[11] C. Jacoboni, F. Nava, C. Canali, and G. Ottaviani, "Electron drift velocity and diffusivity in germanium", Phys. Rev. B, vol. 24, no. 2, pp. 1014-1026, July 1981.

[12] M. V. Fischetti and S. E. Laux, "Monte Carlo simulation of transport in technologically significant semiconductors of the diamond and zinc-blende structure–Part I: Homogeneous transport," IEEE Trans. on Electron Devices, vol. 38, no. 3, pp. 634-649, March 1991.

[13] Y. Azuma, T. Mori, and H. Tsuchiya, "Drive current of ultrathin Ge-on-Insulator n-channel MOSFETs," Abstracts of 34th Int'l Symp. on Compound Semiconductors (ISCS2007), p. 131, Kyoto, October 2007.

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