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Comparisons of Performance Potentials of Silicon Nanowire and Graphene Nanoribbon MOSFETs Considering First-Principles Bandstructure Effects

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Abstract—In this paper, we investigate performance potentials of silicon nanowire (SNW) and semiconducting graphene nanoribbon (GNR) MOSFETs, by using the first-principles bandstructures and ballistic current estimation based on the "top-of-the-barrier" model. As a result, we found that SNW-MOSFETs display a strong orientation dependence via the atomistic bandstructure effects, and [110]-oriented SNW-MOSFETs provide smaller intrinsic device delays than Si ultrathin-body (UTB) MOSFETs when the wire size is scaled smaller than 3nm. Furthermore, GNR-MOSFETs are found to exhibit promising device performance if ribbon width is designed larger than a few nanometers and a finite bandgap can be established.

Index Terms—Nanotransistors, silicon nanowire, graphene nanoribbon, bandstructure, ballistic transport, first-principles calculation

I. INTRODUCTION

It has been well recognized that the conventional device-scaling has not been an effective way to enhance the MOSFET performance under sub-100nm regime, due to several physical and essential limitations such as gate tunneling current, junction leakage current, channel mobility degradation and increased source resistance, which are directly related to the device miniaturization [1]. To overcome these difficulties and make both requirements of low power consumption and high performance compatible, the introduction of high carrier mobility channels and multi-gate architecture becomes crucially important. Recently, high-current-drive MOSFETs using strained-Si, Ge and III-V semiconductors have been studied aggressively [1, 2], while entirely new types of devices such as nanowire transistors and carbon-based transistors have been also explored. In this paper, we focus on emerging nanotransistors, that is, Si nanowire (SNW) MOSFETs and graphene nanoribbon (GNR) MOSFETs to assess their advantages over the conventional Si-MOSFETs.

It is well-known that SNW-MOSFET should offer better electrostatic gate control than planar MOSFETs by employing gate-all-around (GAA) configurations, and furthermore its device performance should display a strong orientation dependence via the bandstructure effects [3]. On the other hand, the GNRs are graphene sheet monolayers [4] patterned along a specific channel transport direction with a narrow channel width [5, 6]. Bulk graphene exhibits ultrahigh electron mobility in excess of 200,000 $cm^2 V^{-1} s^{-1}$ at electron density of ~2×10^{11} cm^{-2} at T=5K [7]. The GNR is known to be a semimetal, but the spatial confinement in its transverse direction can induce a bandgap [8, 9], so appears to be promising for FET applications [9, 10, 11]. In the GNR-MOSFETs, the possibility to pattern nanoscale strip of graphene, which has a definite orientation relative to the substrate, is expected to overcome the carbon nanotube chirality control problem. The ultrathin GNR channel is also effective to provide the superior immunity to short channel effect such as drain-induced-barrier-lowering.

In this paper, we investigate the upper limit performances of SNW-MOSFETs and GNR-MOSFETs by using the first-principles bandstructures and ballistic current estimation based on the "top-of-the-barrier" model [12]. As a result, we found that electronic properties of SNWs and GNRs are a strong function of their transport orientation and width quantization. And in particular, [110]-oriented SNW-MOSFETs and GNR-MOSFETs are shown to exhibit promising device performances if proper

device dimensions can be achieved.

This paper is organized as follows. Si-UTB MOSFETs are first analyzed in Section II to investigate an ultimate device performance of the mainstream planar Si-MOSFETs, where effects of the termination of dangling bonds at Si surfaces by using hydrogen-termination and SiO_2-termination are also examined. In Section III, the [110]- and [100]-oriented SNW-MOSFETs are analyzed to compare with the results for Si-UTB MOSFETs. Performance comparison between SNW-MOSFETs and GNR-MOSFETs is presented in Section IV. The conclusion is drawn in Section V.

II. Si-UTB MOSFETs

A. Atomic Structures

As a benchmark device for the present comparative study, we first consider Si-UTB MOSFETs. Fig. 1 shows the atomic structures used in the Si-UTB simulations, where we employed three types of spatial confinement by using (a) β-cristobalite SiO_2 layers, (b) α-quartz SiO_2 layers and (c) hydrogen-termination of surface dangling bonds [13]. The SiO_2 layers were assumed to be crystalline and placed onto the Si (001) surfaces without any defects, that is, the Si/SiO_2 interfaces are geometrically abrupt. To apply the supercell technique, vacuum layers with a sufficient thickness are included above and below the structures. We refer to (a) and (b) as silicon-on-insulator (SOI) model, and (c) as H-terminated model, respectively. All bandstructure calculations in this paper were performed by using a first-principles simulation package based on the density-functional theory (DFT), VASP, where the electron-electron exchange and correlation interactions were treated within the generalized gradient approximation (GGA). The Kohn-Sham equation was solved by using a plane-wave basis set based on the ultra-soft pseudopotentials and projector-augmented-wave method [14]. To obtain stabilized structures, we performed structure optimization procedures after placing all atoms in a unit cell where a conjugate gradients minimization method was employed to relax all atomic coordinates and cell shape and size via total energy minimization.

B. Bandstructures

Fig. 2 shows the bandstructures along the Γ to X direction computed for (a) β-cristobalite SOI, (b)

α-quartz SOI and (c) H-terminated models, where the Si channels consist of five Si-atomic layers with 0.54nm thickness. Such an extremely-scaled SOI-MOSFET with five Si atomic layers was successfully fabricated and its fundamental device operation was also reported [15]. From Fig. 2, they are found to have a conduction band minimum at the Γ point, which results from the *k*-space projection of the two ellipsoidal bands onto the (001) plane of quantization [3, 13, 16]. There are four more valleys residing off-Γ states (two in the positive and two in the negative k_x axis), that result from the four off-plane ellipsoidal bands. The former Γ valleys appear at lower energies because of their heavier quantization mass than that of the off-Γ valleys. We further notice that the two equivalent valleys projected at the Γ point are split by the interactions [17, 18]. Such a valley splitting is known to affect carrier transport because the density-of-states at conduction band minimum decreases [19, 20, 21]. Here, it is noteworthy that the two SOI models predict significantly larger valley splitting than the H-terminated model. To examine the differences in their valley splitting behaviors, we calculated the valley splitting energies for the three confinement models as a function of the Si layer thickness as shown in Fig. 3 (a), where dependence of the valley splitting energy on applied electrostatic field [3] is not considered in this study. It is found that the two SOI models exhibit nearly identical splitting energies, and predict significantly larger splitting energy than the H-terminated model, especially when the Si layer thickness becomes smaller than 1nm. On the other hand, as shown in Fig. 3 (b), the effective mass of electron parallel to <110> direction at the conduction band minimum is approximately equal to the bulk transverse effective mass, m_t, even for the sub-1nm thickness. As we have previously reported in [13], the bandgap energies computed using the SOI models become smaller than that using the H-terminated model, due to the wavefunction penetration into transition regions formed at the Si/SiO_2 interfaces. Therefore, the spatial confinement using the SiO_2 layers affects valley splitting and bandgap energy, but not the effective mass of electron.

C. Electrical Characteristics

To examine the current-voltage characteristics of Si-UTB MOSFETs under ballistic transport, we employed a "top-of-the-barrier" MOSFET model [12], which is a simple model and can assess an upper limit performance of nanoscale MOSFETs. Quantum tunneling is not accounted for in this model, so the

model was shown to be valid for the MOSFET structure if the channel length is equal to or larger than 10nm [22, 23, 24]. Since the model provides significant insight into the importance of atomistic bandstructures with greatly reduced computational time compared to a full self-consistent quantum transport simulation, the model is suitable for systematic study comparing performance limits of atomistic transistors including carbon-based FETs [22, 23]. As illustrated in Fig. 4, mobile charge Q_{top} is computed directly from the E - k dispersion relations by filling the Fermi-Dirac function with positive velocity states according to the source Fermi energy E_{F1} and negative velocity states according to the drain Fermi energy E_{F2}, and by using the self-consistent potential at the top of the barrier U_{scf}. U_{scf} is controlled by the gate, drain and source potentials through the three capacitors, C_G , C_D and C_S, respectively [12]. In this paper, we assume a perfect electrostatic gate control over the channel, that is, $C_D / C_G, C_S / C_G = 0$. We incorporate a floating boundary condition to take into account the charge neutrality at the source electrode when the gate and drain voltages are sufficiently high.

In this paragraph, we use a single-gate Si-UTB MOSFET with Si layer thickness of 0.54nm and gate insulator thickness of T_{ox} = 0.5nm with dielectric constant of $\varepsilon = 3.9\varepsilon_0$. Fig. 5 shows the computed I_D - V_G characteristics by using the first-principles bandstructures presented in the previous paragraph, where the drain voltage is given by 0.4V. The channel orientation is set at <110>. The results for the three spatial confinement models are also compared with the one for the parabolic effective mass approximation (pEMA) method denoted by the dotted line, where the effective masses were taken as m_t = 0.19m_0 and m_l = 0.98m_0. To account for the difference in bandgap energies between the different confinement models, we fixed the OFF-current density to 0.06μA/μm by tuning the work function of gate electrode. This also renders moot a shortcoming of the DFT method, that is, the bandgap underestimation. First, it is found that the first-principles I_D - V_G curves are always below the pEMA curve, and their deviation from the pEMA theory becomes larger with gate voltage. This is due to an anisotropic and non-parabolic nature of the first-principles bandstructures as shown in Fig. 6, where (a) and (b) correspond to energy contours near the Γ point for the α-quartz SOI and the H-terminated models, respectively. A similar behavior has been observed for the β-cristobalite SOI model. As demonstrated in Fig. 6, the anisotropy and the non-parabolicity are more pronounced for higher

wavenumbers, and thus, the current densities of the first-principles approach decrease more as the gate voltage increases, because the carriers distribute into higher momenta. Furthermore, it is found in Fig. 5 that the H-terminated model predicts the current density slightly lower than the two SOI models, when the gate voltage is sufficiently high. This is due to the stronger nature of the anisotropy and non-parabolicity in the H-terminated model, as found by comparing Figs. 6 (a) and (b). Nevertheless, the H-terminated model is considered to work well for nanoscale confinement of electron waves, at least for low bias condition. Therefore, we employ hydrogen-termination of surface dangling bonds in the SNW and GNR first-principles simulations performed in the following sections.

III. Si Nanowire-MOSFETs

In this section, we investigate the [110]- and [100]-oriented SNW-MOSFETs and compare them with Si-UTB MOSFETs.

A. Atomic Structures

We use square-shaped SNWs with two different orientations, [110] and [100], as shown in Figs. 7 (a) and (b), respectively, since they exhibit better transport performances than other orientations [3]. Quantum confinement directions are indicated in each figure. Note that all surface dangling bonds are terminated by hydrogen atoms. Such square-shaped SNWs will be suitable for a comparative study with the pEMA simulations as discussed later. In the [110]-oriented SNWs, a characteristic wire width is defined as $W \equiv \sqrt{W_1 \times W_2}$, because the two directions have slightly different dimensions. All atoms including the hydrogen atoms have been relaxed by performing the structural optimization procedures.

B. Bandstructures

Fig. 8 shows the bandstructures computed for (a) [110]-SNW and (b) [100]-SNW with about 1nm wire width. They also have a conduction band minimum at the Γ point [3,16]. It is found that the valley splitting at the Γ point is significantly larger in the [110]-SNW than in the [100]-SNW, which is identical with the previous tight-binding results reported in [3]. Fig. 9 (a) shows how this effect varies with the spatial confinement, together with the Si-UTB results. Valley splitting in the [110]-SNWs can reach up

to several hundreds meV for sizes smaller than 2nm, which is much larger than the room temperature thermal energy (k_BT = 26meV), and thus are expected to have a significant influence on the transport properties. Furthermore, Fig. 9 (b) shows the effective masses at the conduction band minimum. It is found that the [110]-SNW effective mass is smaller than the bulk transverse effective mass for sizes smaller than 3nm, while the [100]-SNW effective mass increases with increase in quantization. The above effective mass variations in the SNWs are also identical with the previous tight-binding results [3], and therefore they can be explained using the anisotropy and the non-parabolicity in the Si conduction band Brillouin zone [16]. As discussed in the following paragraph, the effective mass variations mentioned above basically govern the device performance of SNW-MOSFETs.

C. Device Performance Metrics

Intrinsic device delay (τ) is an important performance metric that corresponds to intrinsic limitations on switching speed and ac operation of a transistor. In this study, the intrinsic device delay is calculated as $\tau = (Q_{ON} - Q_{OFF}) / I_{ON}$, where Q_{ON} and Q_{OFF} are the total charge in the channel at on-state and off-state, respectively, and I_{ON} is the on-current. In addition, it is important to compare SNW-MOSFET performance to Si-UTB MOSFETs, and a reasonable comparison must be made by considering both the on-state and the off-state at the same power supply voltage [25]. Fig. 10 uses a technique to compare the intrinsic delays versus the on-off current ratio computed for two SNW-MOSFETs with GAA electrode at the same power supply voltage (V_{DD}=0.4V), where (a) the first-principles bandstructures and (b) the pEMA theory were used. The curves were obtained by sweeping a constant V_{DD}-bias window along V_G axis in the I_D-V_G characteristics computed by using the ballistic top-of-the-barrier model. The details of the comparison technique are explained in [25]. The gate insulator thickness T_{ox} was fixed at 1.5nm with $\varepsilon = 3.9\varepsilon_0$, while the wire width was varied from sub-1nm to a few nm. The channel length L_{ch} was set at 10nm, which allows us to apply the top-of-the-barrier model. In Fig. 10 (a), the results for single-gate and double-gate Si-UTB MOSFETs (H-terminated model) with 0.54nm Si layer thickness are also plotted for comparison, which gives an upper limit performance of the conventional planar Si-MOSFETs under unstrained condition, because almost all electrons occupy the lowest subband with smaller transport mass. It is noteworthy that the

[110]-oriented SNW-MOSFETs indicates smaller intrinsic delays than the Si-UTB MOSFETs, in contrast to the [100]-orientation. It is also interesting to note that the [110]-orientation with W=1.55nm (■) shows the smallest intrinsic delay, while the [100]-orientation indicates the larger intrinsic delay with decreasing the wire width. The behavior in the [100]-orientation can be explained primarily in terms of the effective mass increase in the smaller nanowires as shown in Fig. 9 (b). On the other hand, the [110]-orientation exhibits complicated behavior to the wire width variation in spite of the size-independent effective mass as shown in Fig. 9 (b), which may be related to an increasing influence of quantum capacitance in ultrasmall nanowires.

At the end of this paragraph, we describe the importance of the first-principles approach in the performance projections of SNW-MOSFETs. Fig. 10 (b) shows the device performances of the [110]- and [100]-oriented SNW-MOSFETs computed by using the pEMA theory. In that theory, the transport effective mass at the lowest subband becomes $m_t = 0.19m_0$ for both orientations, and thus the orientation dependence is not observed in Fig. 10 (b). The above results mean that the pEMA method can mislead our understanding on nanowire device operations, and therefore, atomistic simulations such as first-principles or tight-binding methods will be inevitable to promote an efficient research and development of nanowire devices.

IV. GRAPHENE NANORIBBON-MOSFETS

In the final section, we investigate GNR-MOSFETs and compare them with SNW-MOSFETs presented in the previous section.

A. Atomic Structures

We examine armchair-edged GNR shown in Fig. 11, which is known to become semiconducting by the spatial confinement of the ribbons in its transverse direction [9]. In short, an armchair-edged GNR with N (the number of atoms in transverse direction) has bandgap when N=3m or 3m+1, where m is an integer [8,9]. Therefore, armchair-edged GNRs appear to be promising for FET applications. In this study, we focus on the armchair-edged GNRs with N=3m, since qualitative conclusions made with the N=3m group are also applicable to the N=3m+1 group [23, 26]. As in Sec. III, all surface dangling bonds

are terminated by hydrogen atoms, and all the atoms have been relaxed by the structural optimization procedures.

B. Bandstructures

Fig. 12 shows the bandstructures computed for (a) GNR with W=2.1nm (N=18) and (b) GNR with W=4.3nm (N=36). The GNRs have a conduction band minimum and a valence band maximum at the Γ point. We can recognize that as the GNR width W increases the effective mass for both electron and hole reduces and the dispersion curves transform into a linear dispersion, though the bandgap energy significantly decreases. Next, Fig. 13 shows the bandgap energy and the effective mass at the conduction band minimum as a function of GNR width. As reported in [9], the effective mass increases as the GNR width decreases, and therefore the increase in the GNR width will help to increase electron velocity due to the smaller effective mass. However, the GNR width should become below a few nanometers to make the bandgap energy acceptable for the FET operation [9]. The above results are basically consistent with the previous results based on tight-binding and first-principles electronic bandstructure calculations [9, 26], although the effective mass is larger than that in [9].

C. Device Performance Metrics

We consider double-gate GNR-MOSFETs with 1.5nm gate insulator ($3.9\varepsilon_0$), which is the same as in Sec III - C. The intrinsic device delays versus the on-off current ratio computed for five different ribbon widths are shown in Fig. 14, where L_{ch}=10nm and the same power supply voltage (V_{DD}=0.4V) is applied. The on-off ratio is limited so that the leakage current due to band-to-band tunneling is smaller than thermally-injected current from the source electrode. It is found that intrinsic delays decrease abruptly for nanoribbons wider than 3nm, and stop decreasing at 4.3nm ribbon width. Such an abrupt change basically follows the effective mass reduction with increasing ribbon width as shown in Fig. 13. Incidentally, the intrinsic device delay time obtained for the 1nm nanoribbon in this study (~ 0.05ps) corresponds well to the result reported by a full self-consistent quantum transport simulation based on the nonequilibrium Green's function formalism [27], where 1.35nm ribbon width was considered.

Furthermore, the results for the [110]-oriented SNW-MOSFETs are also plotted in Fig. 14, which indicates that GNR-MOSFETs with W > 4nm exhibit smaller intrinsic device delays than the

SNW-MOSFETs. Here, as you can see by comparing Figs. 9 (b) and 13, the [110] SNWs offer slightly smaller effective mass than the wide GNRs, that is, $m^* \approx 0.13m_0$ for the [110] SNWs and $0.14 \sim 0.18m_0$ for the wide (W=4.3, and 5.2nm) GNRs. Consequently, the linear dispersion nature in wide GNRs may contribute to provide the smaller intrinsic delays. To confirm it, dispersion curves for several GNR widths are compared in Fig. 15, together with the [110] SNW dispersion curve. It is found that the dispersion curve transforms from a parabolic dispersion (similar to SNW) to a linear dispersion (unique to graphene) in a few nanometers change in ribbon width, that is, between 2.1 to 4.3nm widths. At on-state, electrons can populate the higher momentum region and then the linear dispersion property in wide GNRs endows higher average velocity for electrons. In fact, as shown in Fig. 16 the wide ($W >$ 4nm) GNR-MOSFETs provide significantly higher average velocity than the [110] SNW-MOSFETs, and the maximum velocity reaches up to 5×10^7cm/s. Therefore, the appearance of a linear dispersion curve is an important factor to obtain superior device performance in GNR-MOSFETs.

V. CONCLUSION

We investigated the performance potentials of Si-UTB MOSFETs, SNW-MOSFETs and semiconducting GNR-MOSFETs by considering the first-principles bandstructures based on the DFT method. As a result, we found that the [110]-oriented SNW-MOSFETs exhibit superior device performances as digital switches, providing smaller intrinsic device delays than Si-UTB MOSFETs when the wire size is downscaled smaller than 3nm. We also verified that the parabolic effective mass approximation possibly misleads our understanding on nanowire device operations, and atomistic simulations such as first-principles or tight-binding methods are inevitable. Furthermore, we demonstrated that the GNR-MOSFETs can provide better device performance than the SNW-MOSFETs, if ribbon widths with larger than a few nanometers are achieved and the tunneling leakage current can be suppressed by establishing a finite bandgap.

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Takeshi Hara was born in Ishikawa, Japan, on July 7, 1984. He received the B. S. and M. S. degrees all in electrical and electronics engineering from Kobe University, Kobe, Japan, in 2007 and 2009, respectively. His research involves first principles simulation of ultrathin SOI channels, including high-*k* gate oxide.

Mr. Hara is a member of the Japan Society of Applied Physics.

Hironobu Yao Biography is not available.

Matsuto Ogawa (M'85–SM'09) received the B.E. in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1980, and the M.S. and Ph.D degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, 1n 1982, and 1985, respectively. In that year he became a research associate in the Department of Electronic Engineering, Kobe University, Kobe, Japan, where he is presently a full professor. He has been engaged in research of lightwave electronics and nano-scaled devices. His current research includes quantum transport modeling in nanostructures. From 1992 to the end of 1993, he was on leave at IBM T.J. Watson Research Center in New York as a visiting scientist.

Dr. Ogawa is a member of the IEEE, the Japan Society of Applied Physics and the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan. He received Electronics Society Award in 2006 from the IEICE and Project Research Award from the Semiconductor Technology Academic Research Center (STARC) in 2008.

FIGURE CAPTIONS

Fig. 1. Atomic structures used in the Si-UTB simulations, where we employed three types of spatial confinement by using (a) β-cristobalite SiO_2 layers, (b) α-quartz SiO_2 layers and (c) hydrogen-termination of surface dangling bonds. To apply the supercell technique, vacuum layers with a sufficient thickness are included above and below the structures. We refer to (a) and (b) as silicon-on-insulator (SOI) model, and (c) as H-terminated model.

Fig. 2. Bandstructures along Γ to X direction computed for (a) β-cristobalite SOI, (b) α-quartz SOI and (c) H-terminated models, where Si channels consist of five Si-atomic layers with W=0.54nm.

Fig. 3. (a) Valley splitting energies and (b) electron effective masses parallel to <110> direction at conduction band minimum for the three confinement models, computed as a function of Si layer thickness. The horizontal line in (b) represents the bulk transverse effective mass, m_t. Dependence of the valley splitting energy on applied electrostatic field is not considered in this study.

Fig. 4. Top-of-the-barrier ballistic MOSFET model.

Fig. 5. I_D - V_G characteristics of single-gate Si-UTB MOSFET by using the first-principles bandstructures, where Si layer thickness W is 0.54nm, gate insulator thickness T_{ox} 0.5nm, and dielectric constant $3.9\varepsilon_0$. The drain voltage is given by 0.4V. The channel orientation is set at <110>. The results for the three spatial confinement models are compared with the one for the parabolic effective mass approximation (pEMA) method, where effective masses were taken as $m_t = 0.19m_0$ and $m_l = 0.98m_0$. The simulations are performed at the same OFF-current density (I_{off} = 0.06μA/μm).

Fig. 6. Energy contours near the Γ point for (a) α-quartz SOI and (b) H-terminated models. The Si layer thickness W is 0.54nm.

Fig. 7. Atomic structures used in the SNW simulations, where we use square-shaped cross-section and two different orientations, [110] and [100]. Note that all surface dangling bonds are terminated by hydrogen atoms. In the [110]-oriented SNWs, a characteristic wire width is defined as $W \equiv \sqrt{W_1 \times W_2}$, because the two directions have slightly different dimensions.

Fig. 8. Bandstructures computed for (a) [110]-SNW and (b) [100]-SNW with about 1nm wire width.

Fig. 9. (a) Valley splitting energies and (b) electron effective masses at conduction band minimum for [110]- and [100]-oriented SNWs. The results for Si-UTB are also plotted.

Fig. 10. Intrinsic device delays versus on-off current ratio computed for SNW-MOSFETs with GAA electrode at the same power supply voltage (V_{DD}=0.4V), where (a) first-principles bandstructures and (b) pEMA theory were used. The channel length L_{ch} was set at 10nm. In (a), the results for single-gate and double-gate Si-UTB MOSFETs (H-terminated model) with 0.54nm Si layer thickness are also plotted for comparison, which gives an upper limit performance of the conventional planar Si-MOSFETs under unstrained condition.

Fig. 11. Atomic structures used in armchair-edged GNR simulation, where N represents the number of atoms in its transverse direction. All surface dangling bonds are terminated by hydrogen atoms.

Fig. 12. Bandstructures computed for (a) narrow GNR with W=2.1nm (N=18) and (b) wide GNR with W=4.3nm (N=36).

Fig. 13. Bandgap energy and effective mass at conduction band minimum as a function of GNR width W, where data for N=3m are plotted.

Fig. 14. Comparisons of intrinsic device delays between [110]-GAA-SNW-MOSFETs and double-gate GNR-MOSFETs for five different ribbon widths, where gate insulator thickness is 1.5nm and dielectric constant 3.9 ε_0 . L_{ch} =10nm and the same power supply voltage (V_{DD}=0.4V) was applied.

Fig. 15. Comparison of conduction band dispersion curves near Γ point for GNRs with several ribbon widths. The dispersion curve for the smallest [110] SNW is also plotted for comparison. Note that energies at the conduction band minimum were set at zero for all curves.

Fig. 16. Comparison of average electron velocities between [110]-GAA-SNW-MOSFETs and double-gate GNR-MOSFETs at V_{DD}=0.4V.

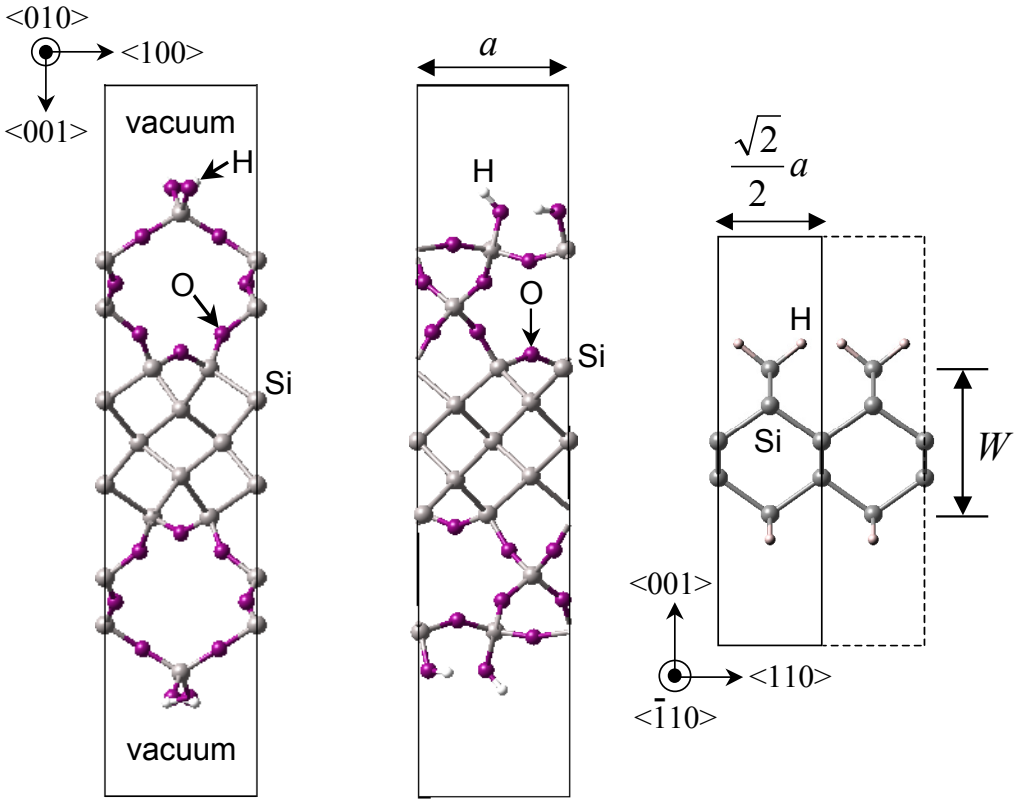


FIGURE 1

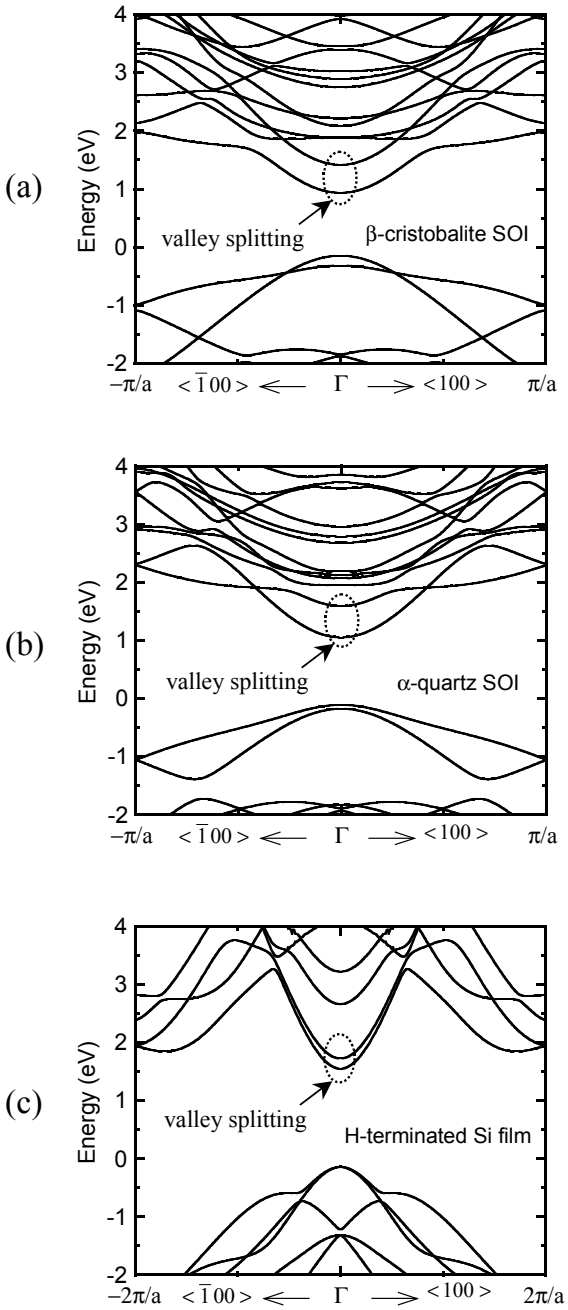
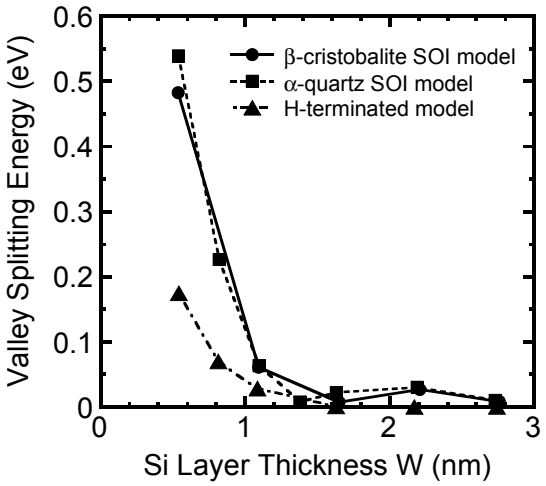

(a)
Energy (eV)
valley splitting
β-cristobalite SOI
−π/a
< $\bar{1}$00 >
Γ
< 100 >
π/a
(b)
Energy (eV)
valley splitting
α-quartz SOI
−π/a
< $\bar{1}$00 >
Γ
< 100 >
π/a
(c)
Energy (eV)
valley splitting
H-terminated Si film
−2π/a
< $\bar{1}$00 >
Γ
< 100 >
2π/a

FIGURE 2

(a)


Valley Splitting Energy (eV)
0.6
0.5
0.4
0.3
0.2
0.1
0
0
1
2
3
Si Layer Thickness W (nm)
β-cristobalite SOI model
α-quartz SOI model
H-terminated model

(b)

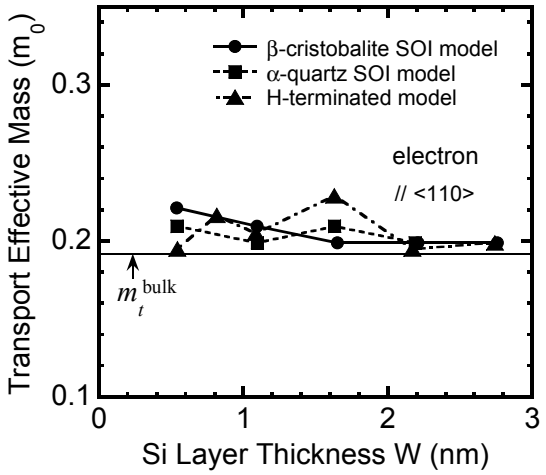

Transport Effective Mass (m0)
0.3
0.2
0.1
0
1
2
3
Si Layer Thickness W (nm)
β-cristobalite SOI model
α-quartz SOI model
H-terminated model
electron
// <110>
m_t^bulk

FIGURE 3

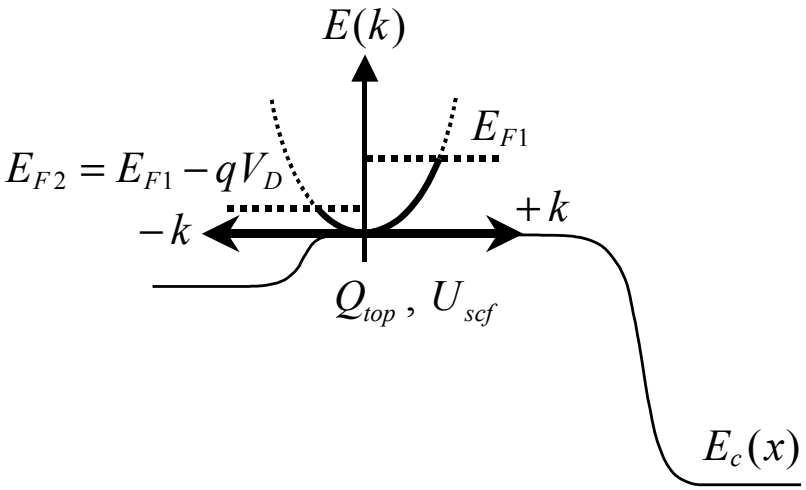


FIGURE 4

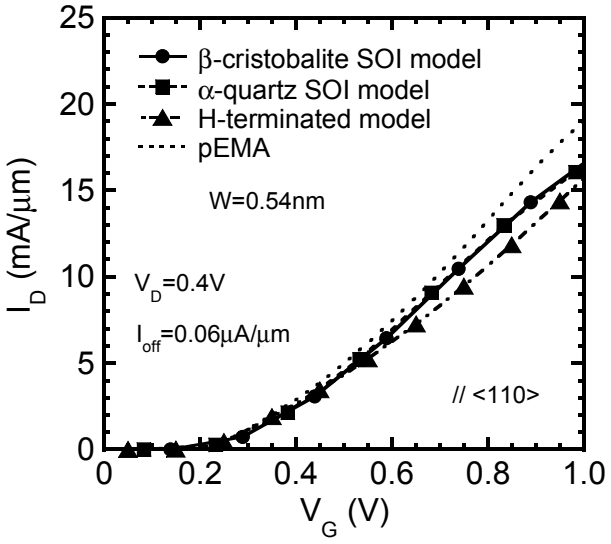

β-cristobalite SOI model
α-quartz SOI model
H-terminated model
pEMA
W=0.54nm
V_D=0.4V
I_off=0.06μA/μm
// <110>
I_D (mA/μm)
V_G (V)
0
5
10
15
20
25
0
0.2
0.4
0.6
0.8
1.0

FIGURE 5

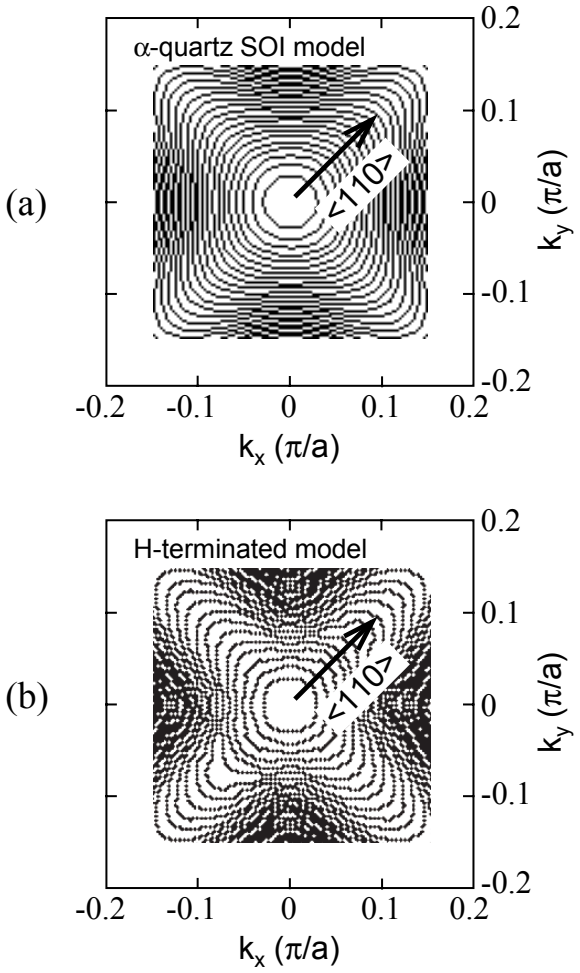

(a)
α-quartz SOI model
<110>
0.2
0.1
0
-0.1
-0.2
-0.2
-0.1
0
0.1
0.2
k_x (π/a)
k_y (π/a)
(b)
H-terminated model
<110>
0.2
0.1
0
-0.1
-0.2
-0.2
-0.1
0
0.1
0.2
k_x (π/a)
k_y (π/a)

FIGURE 6

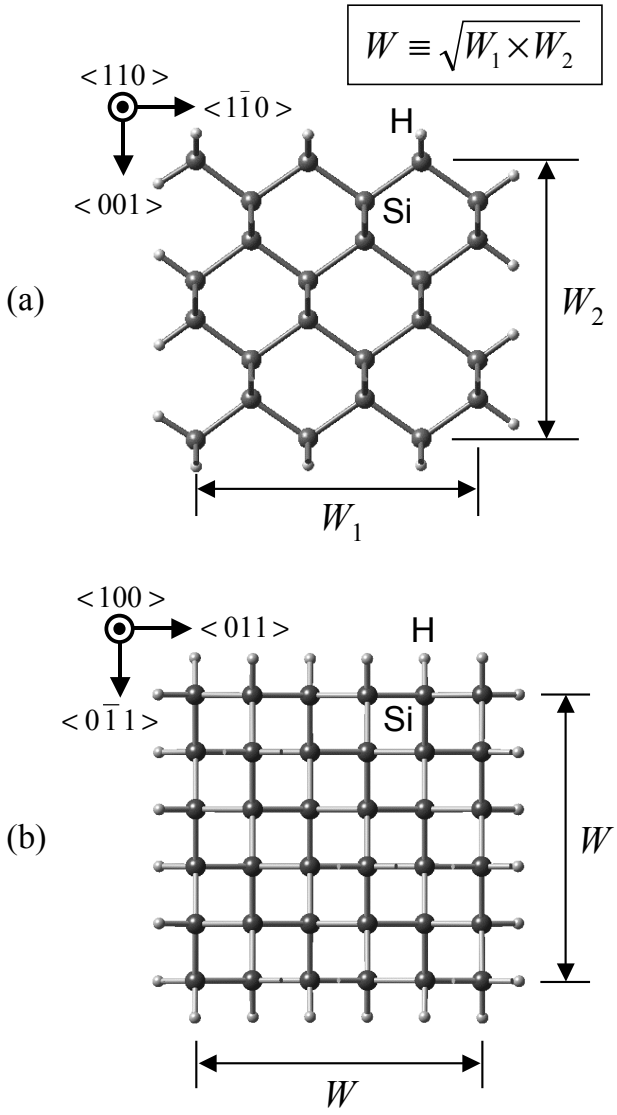
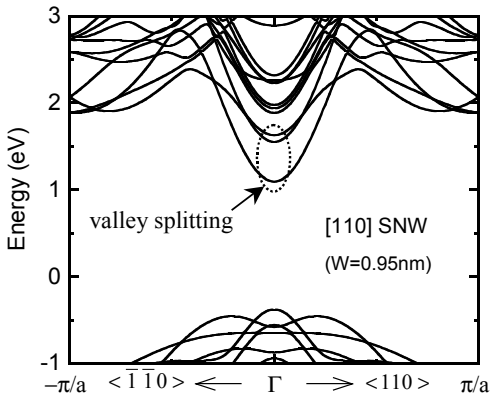

$W \equiv \sqrt{W_1 \times W_2}$
<110>
<1$\bar{1}$0>
<001>
H
Si
W_2
W_1
(a)
<100>
<011>
<0$\bar{1}$1>
H
Si
W
W
(b)

FIGURE 7

(a)


3
2
1
0
-1
Energy (eV)
valley splitting
[110] SNW
(W=0.95nm)
–π/a
< $\bar{1}\,\bar{1}$ 0 >
Γ
< 110 >
π/a

(b)

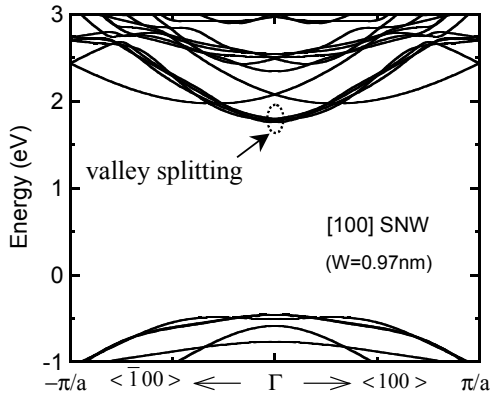
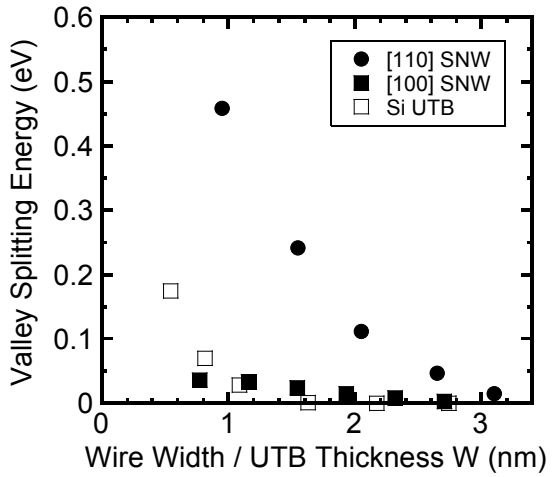

3
2
1
0
-1
Energy (eV)
valley splitting
[100] SNW
(W=0.97nm)
–π/a
< $\bar{1}$00 >
Γ
< 100 >
π/a

FIGURE 8

(a)


Valley Splitting Energy (eV)
0.6
0.5
0.4
0.3
0.2
0.1
0
0
1
2
3
Wire Width / UTB Thickness W (nm)
[110] SNW
[100] SNW
Si UTB

(b)

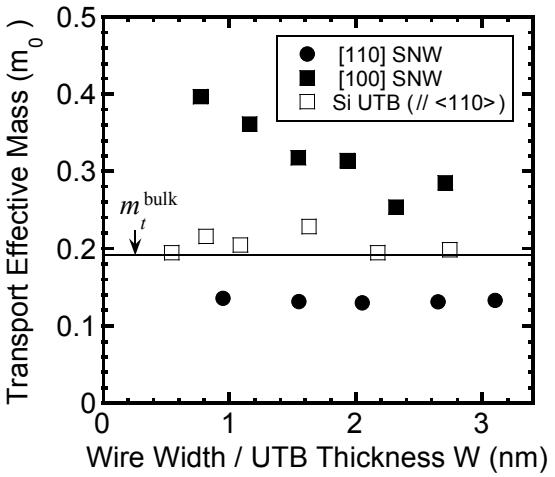

Transport Effective Mass (m0)
0.5
0.4
0.3
0.2
0.1
0
0
1
2
3
Wire Width / UTB Thickness W (nm)
[110] SNW
[100] SNW
Si UTB (// <110>)
m_t^bulk

FIGURE 9

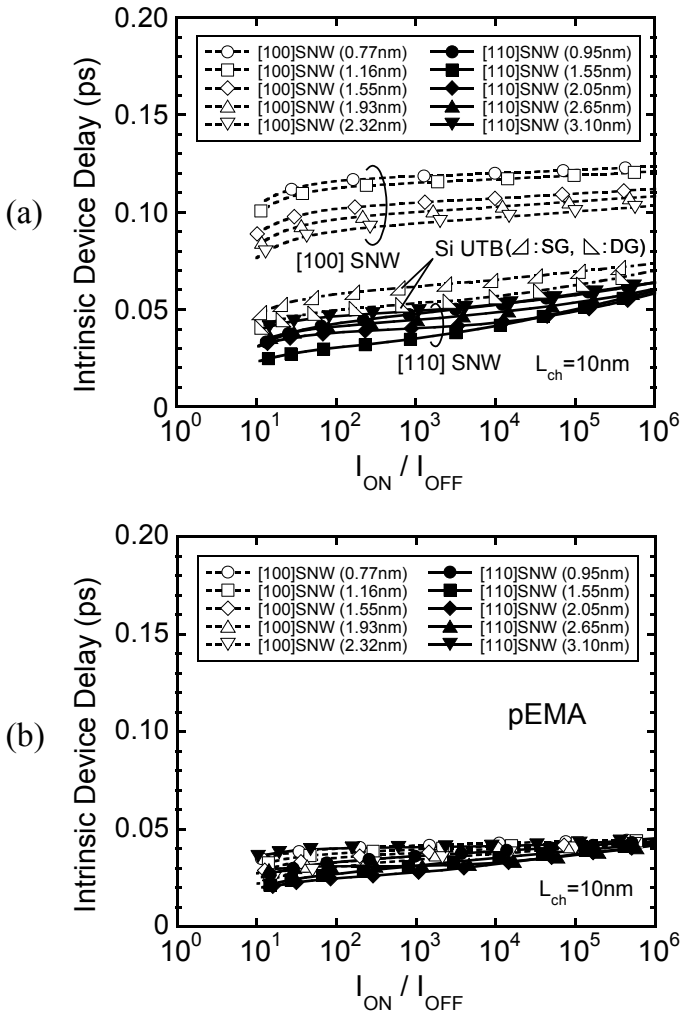

(a)
Intrinsic Device Delay (ps)
0.20
0.15
0.10
0.05
0
[100]SNW (0.77nm)
[100]SNW (1.16nm)
[100]SNW (1.55nm)
[100]SNW (1.93nm)
[100]SNW (2.32nm)
[110]SNW (0.95nm)
[110]SNW (1.55nm)
[110]SNW (2.05nm)
[110]SNW (2.65nm)
[110]SNW (3.10nm)
[100] SNW
Si UTB(◿:SG, ◺:DG)
[110] SNW
L_ch=10nm
10^0 10^1 10^2 10^3 10^4 10^5 10^6
I_ON / I_OFF
(b)
Intrinsic Device Delay (ps)
pEMA
L_ch=10nm
I_ON / I_OFF

FIGURE 10

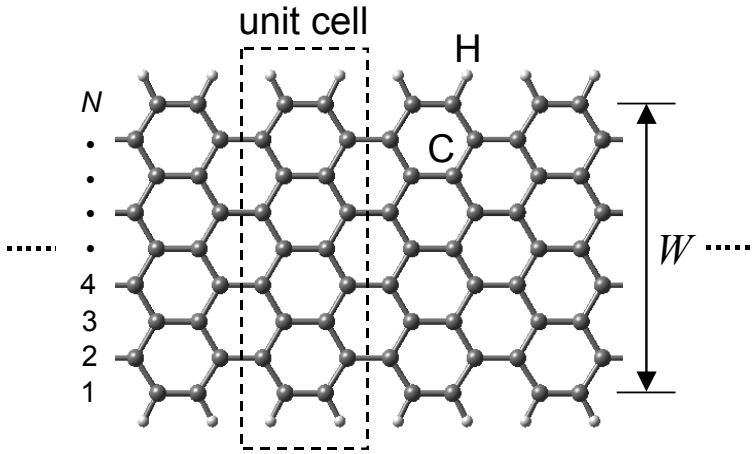

unit cell
H
C
N
4
3
2
1
W
N: number of atoms in transverse direction

FIGURE 11

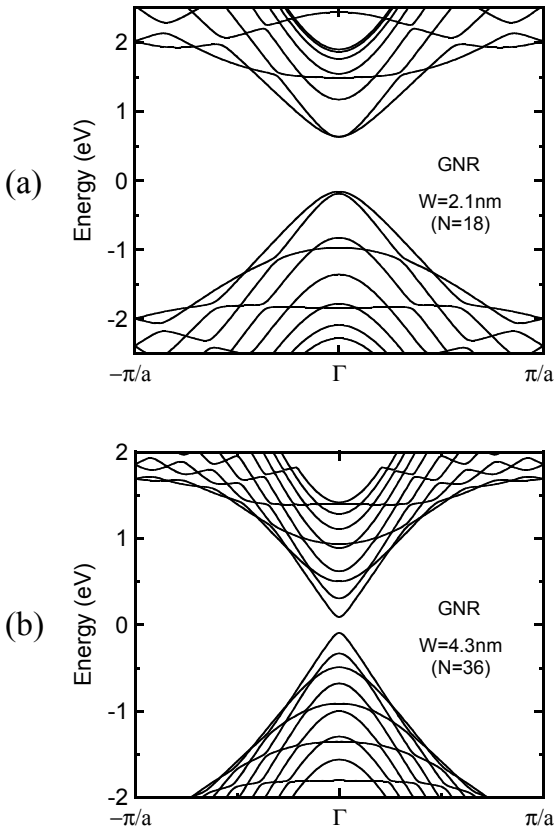

(a)
Energy (eV)
2
1
0
-1
-2
GNR
W=2.1nm
(N=18)
−π/a
Γ
π/a
(b)
Energy (eV)
2
1
0
-1
-2
GNR
W=4.3nm
(N=36)
−π/a
Γ
π/a

FIGURE 12

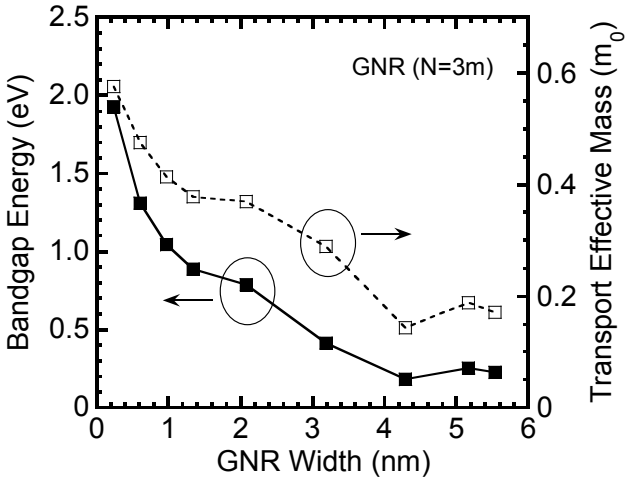

GNR (N=3m)
Bandgap Energy (eV)
Transport Effective Mass (m_0)
GNR Width (nm)
0
0.5
1.0
1.5
2.0
2.5
0.2
0.4
0.6
1
2
3
4
5
6

FIGURE 13

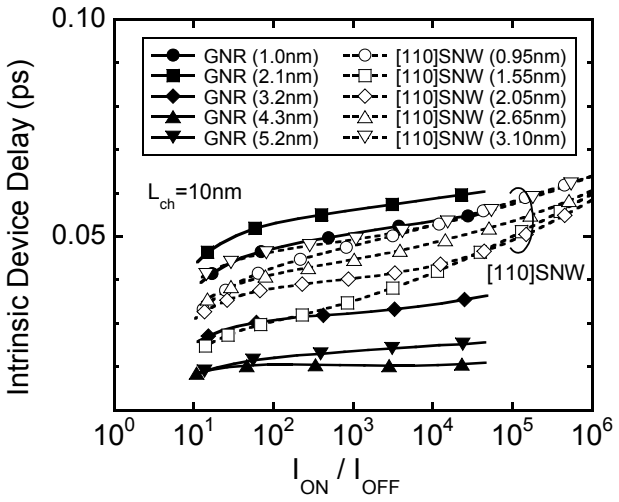

0.10
0.05
Intrinsic Device Delay (ps)
GNR (1.0nm)
GNR (2.1nm)
GNR (3.2nm)
GNR (4.3nm)
GNR (5.2nm)
[110]SNW (0.95nm)
[110]SNW (1.55nm)
[110]SNW (2.05nm)
[110]SNW (2.65nm)
[110]SNW (3.10nm)
L_ch=10nm
[110]SNW
10^0 10^1 10^2 10^3 10^4 10^5 10^6
I_ON / I_OFF

FIGURE 14

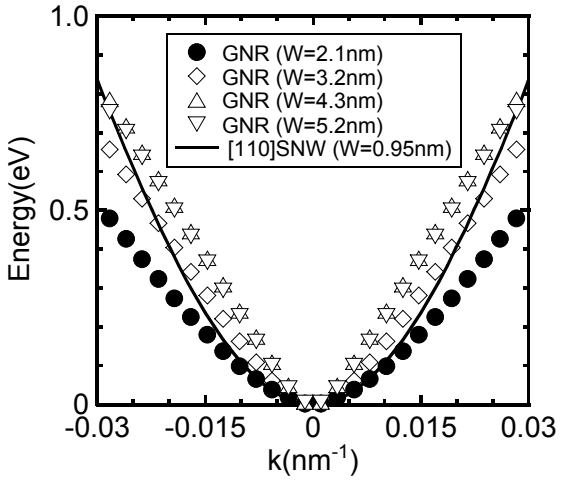

1.0
0.5
0
Energy(eV)
-0.03
-0.015
0
0.015
0.03
k(nm-1)
GNR (W=2.1nm)
GNR (W=3.2nm)
GNR (W=4.3nm)
GNR (W=5.2nm)
[110]SNW (W=0.95nm)

FIGURE 15

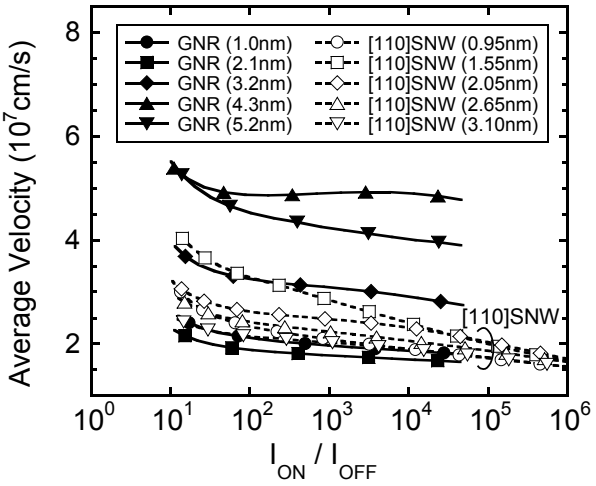

GNR (1.0nm)
GNR (2.1nm)
GNR (3.2nm)
GNR (4.3nm)
GNR (5.2nm)
[110]SNW (0.95nm)
[110]SNW (1.55nm)
[110]SNW (2.05nm)
[110]SNW (2.65nm)
[110]SNW (3.10nm)
[110]SNW
Average Velocity (10^7cm/s)
I_ON / I_OFF

FIGURE 16