

PDF issue: 2025-12-05

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(Citation)
Applied Physics Express, 4(8):084301-084301(3)

(Issue Date)
2011-08-25
(Resource Type)
journal article
(Version)
Accepted Manuscript
(Rights)
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(URL)
https://hdl.handle.net/20.500.14094/90001633
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## Influence of Source/Drain Parasitic Resistance on Device Performance of Ultrathin Body III-V Channel Metal-Oxide-Semiconductor Field-Effect Transistors

Yōsuke Maegawa<sup>1</sup>, Shunsuke Koba<sup>1</sup>, Hideaki Tsuchiya<sup>1,2</sup>, and Matsuto Ogawa<sup>1</sup>

Abstract—The influence of source/drain (S/D) parasitic resistance in ultrathin body (UTB) III-V channel metal-oxide-semiconductor field-effect transistor (MOSFET) was investigated based on Monte Carlo simulation. We found that heavily doped S/D improves source starvation and suppresses carrier's backscattering from drain to channel, owing to increased electron-electron scattering. As a result, the heavily doped S/D was shown to be effective to enhance the current drive and transconductance of UTB III-V channel MOSFET. In addition, we demonstrated that the heavily doped S/D has the advantage to provide unsaturated drain current characteristics.

<sup>&</sup>lt;sup>1</sup>Department of Electrical and Electronic Engineering, Graduate School of Engineering, Kobe University, Kobe 657-8501, Japan

<sup>&</sup>lt;sup>2</sup>Japan Science and Technology Agency, CREST, Chiyoda, Tokyo 102-0075, Japan

III-V compound semiconductors are promising candidates for channel materials in future high-performance metal-oxide-semiconductor field-effect transistors (MOSFETs), because they have higher electron mobility and lower effective mass than Si. Recently, the high performance of InGaAs MOSFETs with high-k gate dielectrics fabricated by atomic layer deposition (ALD) has been demonstrated [1-4]. On the other hand, due to the low dopant solubility inherent to III-V materials, reducing source/drain (S/D) parasitic resistance  $R_{\rm SD}$  is recognized as one of the most critical and difficult challenges to realize high current drivability, particularly under the quasi-ballistic transport [5,6]. Thus, the use of self-aligned metal S/D [7] and regrown S/D structures [8] is a promising way to overcome this limitation.

According to previous simulation studies [5,6], the source doping concentration  $N_{\rm SD}$  is required to be around  $10^{20}$  cm<sup>-3</sup> for high injection current without source starvation in III-V MOSFETs. However, the maximum doping concentration with ion implantation is around  $10^{19}$  cm<sup>-3</sup> in InGaAs [9]; therefore, the reduction in  $R_{\rm SD}$  due to alternative approaches, such as raised S/D and thicker channel, is one of the candidates [5]. In this paper, to clarify the roles of S/D doping concentration and its related electron-electron scattering, we perform electron transport simulation in III-V MOSFETs with different levels of S/D doping concentration by considering plasmon scattering. Then, their relevance to the source starvation and the device performance is discussed.

Since ultrathin body (UTB) III-V channel on Si platform is desirable for future MOSFETs, we adopted UTB III-V-on-insulator MOSFETs as shown in Fig. 1. The channel of 30 nm length is assumed to be intrinsic, and both the channel and S/D electrodes are composed of InP with thickness of 5 nm. For InP, the high doping concentration up to  $10^{20}$  cm<sup>-3</sup> has been reported to be possible [10,11]. Hence, we considered two different doping concentrations in the S/D electrodes of  $N_{\rm SD} = 2 \times 10^{19}$  cm<sup>-3</sup> and  $1 \times 10^{20}$  cm<sup>-3</sup>. The former is called normally doped SD and the latter heavily doped SD. The gate and buried oxides are SiO<sub>2</sub>. A thicker channel is not considered in this study, because it will not be suitable for ultrashort-channel MOSFETs.

The electrical characteristics were computed by using a quantum-corrected Monte Carlo (MC) device simulator developed in our laboratory [12,13]. The quantum-corrected MC simulation is a suitable tool for the present objective, because it has been proven to be adequate to describe quantization effects in the direction normal to the transport direction [12,13]. We simulated electron transport in  $\Gamma$  and L valleys of InP, where the energy difference between them,  $\Delta E_{\Gamma L}$ , was taken as 0.832 eV [6]. We considered phonon and impurity scatterings, while roughness scattering is ignored to directly characterize the influence of  $R_{SD}$ . Furthermore, to investigate the role of electron-electron scattering in the S/D electrode, plasmon scattering was

taken into account in the S/D regions, where a plasmon scattering rate for three-dimensional electron gas was used [13,14]. For impurity scattering, we considered Fermi–Dirac statistics to calculate the screening length [6,15]. Here, note that the plasmon scattering rate and the impurity scattering rate depend on carrier concentration and/or S/D doping concentration. In other words, these two scattering processes make greater influence on electron transport as the S/D doping concentration increases. Therefore, the source starvation resulting from ballistic transport may be eliminated by increasing S/D doping concentration. The present simulation will demonstrate how plasmon scattering and impurity scattering are responsible for improving the source starvation problem.

First, we computed the drain current versus gate voltage ( $I_D - V_G$ ) characteristics and the transconductance versus gate voltage ( $g_m - V_G$ ) characteristics as shown in Fig. 2, where (a) and (b) represent the results without and with plasmon scattering in the S/D regions, respectively. The drain voltage is given as 0.5 V and the threshold voltage  $V_{th}$  is all set at 0.3 V. It is found that in the presence or absence of plasmon scattering, the drain current and transconductance increase by employing the heavily doped SD. This means that the reduction in  $R_{SD}$  due to the heavy doping prevails over the co-occurring scattering increment. Here, we point out that the normally doped SD MOSFET indicates pronounced saturation behavior in the  $I_D - V_G$  characteristics. This is due to relatively small Fermi energy in the normally doped source, not due to the electron transfer to L valleys with heavier transport mass. In other words, as shown in Fig. 3, the normally doped source has smaller Fermi energy and thus promptly reaches saturation in source-injected electrons with a small gate bias swing. On the other hand, the heavily doped source with larger Fermi energy continues to supply electrons until the bottleneck potential drops below the source potential. In this regard, the heavily doped SD has the advantage to provide a wide gate bias range of operation with higher transconductance.

Next, we discuss the influence of plasmon scattering in detail. By comparing Figs. 2(a) and 2(b), the drain current and transconductance significantly degrade for both doping concentrations due to the plasmon scattering. To explain such performance degradation, the averaged electron velocity and the sheet electron density profiles are plotted in Fig. 4, where  $V_G$  -  $V_{th} = 0.4$  V. First of all, it is found that the source starvation is mitigated in the heavily doped SD with plasmon scattering as shown in Fig. 4(b). This means that the source starvation is not improved by the enhanced impurity scattering, but by the enhanced plasmon scattering due to the heavy doping. Namely, in the heavily doped SD, the plasmon quantum energy is about 0.37 eV and thus electrons lose sufficient amount of energy to restore a thermal equilibrium state due to plasmon emission processes. On the other hand, in the normally doped SD, the plasmon

quantum energy reduces to about 0.16 eV, and since this is not sufficient to restore the thermal equilibrium state, the source starvation still remains in the normally doped SD even if the plasmon scattering processes are considered.

As for the averaged electron velocity, it is found to decrease in the S/D regions due to the plasmon scattering, by comparing the profiles between Figs. 4(a) and 4(b). Further, by closely looking at the channel region, we notice that the averaged velocity in the heavily doped SD slightly increases by considering the plasmon scattering. This is due to the fact that electrons after suffering plasmon emission processes in the heavily doped drain have less chance to go back to the channel, because they lose a large kinetic energy of ~0.37 eV. Through these effects by increased plasmon scattering, which are the suppression of backscattered electrons into the channel and the improvement of the source starvation, the heavily doped SD MOSFET still exhibits superior device performances over the normally doped SD MOSFET, as shown in Fig. 2(b).

In conclusion, we have investigated the roles of S/D doping concentration and its electron-electron scattering in UTB III-V channel MOSFETs based on the Monte Carlo simulation. We found that the heavily doped SD not only reduces parasitic resistance, but also improves source starvation and suppresses carrier's backscattering from drain to channel owing to increased plasmon scattering. As a result, heavily doped SD is effective to enhance the current drive and transconductance even when plasmon scattering happens in the S/D regions. Another advantage of heavily doped SD, that is, unsaturated  $I_D$  -  $V_G$  and  $g_m$  -  $V_G$  characteristics, was also demonstrated.

## Acknowledgement

This research was supported by Grant-in-Aid for Scientific Research from the Japan Society for the Promotion of Science (JSPS), and the Japan Science and Technology Agency (JST)/CREST.

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## FIGURE CAPTIONS

- **Fig. 1**. UTB III-V-on-insulator MOSFETs with two different S/D doping concentrations are considered:  $N_{\rm SD} = 2 \times 10^{19}$  cm<sup>-3</sup> and  $1 \times 10^{20}$  cm<sup>-3</sup>. The former is called normally doped SD and the latter heavily doped SD. The channel of 30 nm length is assumed to be intrinsic, and both the channel and SD electrodes are composed of InP with thickness of 5 nm.
- <u>Fig. 2</u>.  $I_D$   $V_G$  and  $g_m$   $V_G$  characteristics computed for the two S/D doping concentrations, where (a) and (b) represent the results without and with plasmon scattering in the S/D regions, respectively.  $V_D = 0.5 \text{ V}$  and  $V_{th} = 0.3 \text{ V}$ .  $L_{ch} = 30 \text{ nm}$ .
- **Fig. 3**. Schematic diagrams representing variations in potential distribution along channel direction due to gate bias swing, where (a) and (b) represent normally doped and heavily doped SD electrodes, respectively. Actual values of the source Fermi energy are indicated.
- **Fig. 4**. Averaged electron velocity and sheet electron density profiles computed for the two S/D doping concentrations, where (a) and (b) represent the results without and with plasmon scattering in the S/D regions, respectively.  $V_G$   $V_{th}$  = 0.4 V and  $V_D$  = 0.5 V. The arrows in the right figures represent the degrees of source starvation (source-electron deficiency).

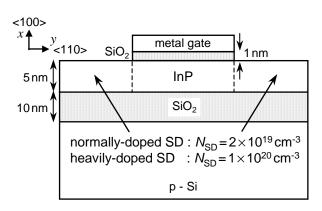


FIGURE 1

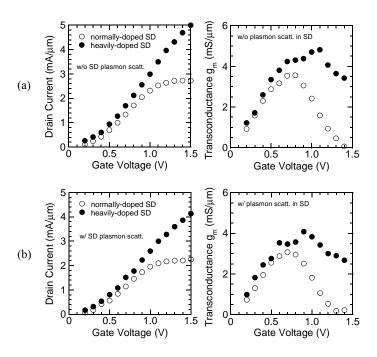


FIGURE 2

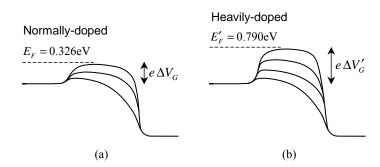


FIGURE 3

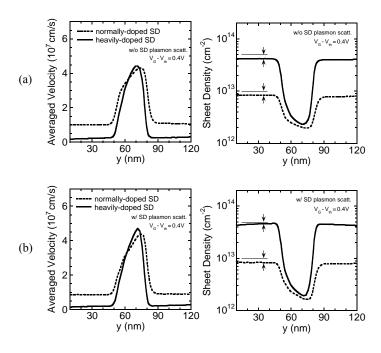


Figure 4