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A 58-μW Single-Chip Sensor Node Processor with Communication Centric Design*

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SUMMARY This paper presents an ultra-low-power single-chip sensor-node VLSI for wireless-sensor-network applications. A communication centric design approach has been introduced to reduce the power consumption of the RF circuits and the entire sensor network system, through a vertical cooperative design among circuits, architecture, and communication protocols. The sensor-node LSI features a synchronous media access control (MAC) protocol and integrates a transceiver, i8051 microcontroller, and dedicated MAC processor. The test chip occupies $3 \times 3\,\mathrm{mm}^2$ in a 180-nm CMOS process, including 1.38 M transistors. It dissipates 58.0 μW under a network environment.

key words: *cross-layer design, sensor networks, sensor node, MAC protocol, time synchronization, low power*

1. Introduction

A Recent advances in micro-sensors, integrated circuits, and wireless communication technologies realize wireless sensor networks (WSNs). Applications of sensor networks comprising numerous such sensor nodes include remote environmental monitoring, smart spaces, military surveillance, and precision agriculture.

A WSN consists of many wireless sensor nodes, each of which is driven by a small battery. The sensor nodes obtain environmental information and send it to a base station with a multi-hopping scheme, under the severe energy constraint. As the number of sensor nodes increases to hundreds or to thousands, the persistent necessity of changing batteries would be a considerable burden. For that reason, the most important issues on the WSNs are to extend an available period, say, network lifetime as long as possible. On the other words, it is highly desirable to reduce the power being used by each sensor node.

In this paper, we propose a single-chip ultralow-power sensor node processor with a synchronous media access control (MAC) protocol. For the power of the sensor node and its cost, it is necessary to be implemented on an LSI, so that we can extend the lifetime and achieve low cost in the entire system.

A low-power transceiver and a wireless SoC for a WSN have been reported [1], [2]. However, those main purposes are the power reduction of RF circuit or processors. Note that [2] implements TICER [3] as a dedicated processor, but the chip is not integrated with an RF transceiver.

In contrast, we have paid attention to the communication centric design. The feature of our design approach is a communication centric design. According to Moore's law, a power of digital portions is scaled down with the progress of process technology. On the other hand, the power consumption of analog RF circuits will not scale at the same rate. In the entire system of the sensor networks, the power consumption of the RF circuits depends on the amount of its communications. Thus, the communication centric design is strongly requested to reduce the power consumption of the RF circuits.

The rest of this paper is organized as follows: The communication protocol and its implementation are explained in Sect. 2. The architecture of proposal sensor node LSI is addressed in Sect. 3. Section 4 describes VLSI implementation and performance comparison. Finally, conclusions are drawn in Sect. 5.

2. Communication Protocols

To achieve communication centric design, the cross layer design between the hardware (node processor architecture) and the algorithm (communication protocol) is indispensable. In this work, especially we focus on MAC protocol which is a communication protocol of the data link layer. While a node communicates, MAC protocol is always executed since the function of MAC protocol is establishing communication links for data transfer, the active time of the RF circuit mainly depends on the MAC protocol.

- For the above reason, our proposed sensor node processor is designed by the "MAC protocol oriented" vertical integration among circuits, architecture, and communication protocols. The salient features on the proposed sensor node are as follows:
- Isochronous-MAC (I-MAC) protocol [4] is introduced, which has a periodic wakeup time synchronized with the Flooding Time Synchronization Protocol (FTSP). This reduces the active time of the RF circuits.
- The dedicated MAC processor. This reduces the communication power.

The power management module (PMM) based on the MAC state transition. This reduces the total power on the

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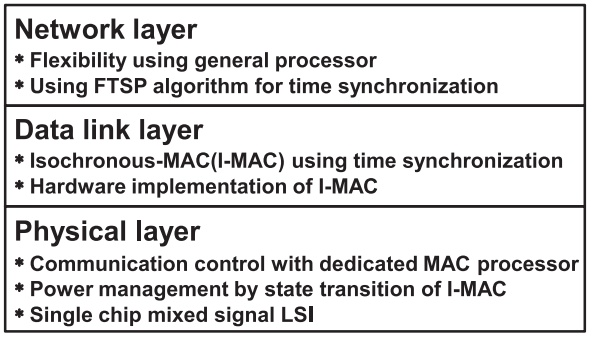

Fig. 1 Cross-layer design for communication centric sensor node.

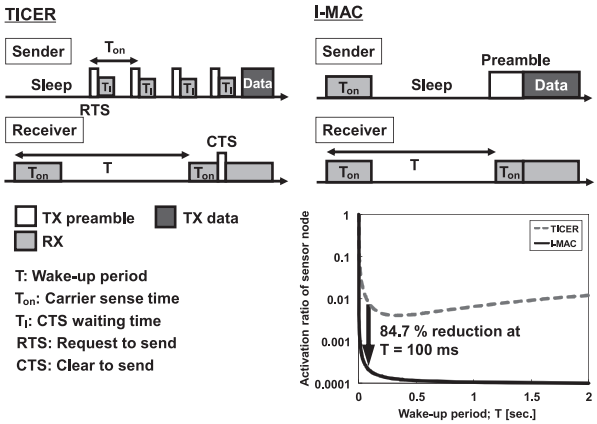

Fig. 2 Comparison of the TICER and the I-MAC.

chip including digital circuits.

Figure 1 illustrates the scope of this paper in the protocol stack. The features of the cross-layer design in the proposed sensor node are as follows:

- Active-time reduction of the RF circuits that consume large power, by improving communication protocols
- Efficient power management that reflects the state transition on the media access control.

In this section, we describe the I-MAC protocol with the FTSP and how the communication protocols are implemented. The I-MAC is used as an MAC protocol because of its low-power characteristics. The FTSP is utilized in order to realize time synchronization for the I-MAC. Also the communication control processor is designed for the low power implementation of the above protocols.

2.1 Isochronous-MAC (I-MAC)

Since MAC protocol is always executed when a node communicates, simplicity and low power characteristics are required in the sensor networks. Also, MAC protocol has to establish communication links as much as possible at short time.

An effective way to reduce the energy in MAC is shorten the idle listening, in which the receiver is activated, even when no packet is received. To reduce the power of this idle listening, a type of MAC named Cycled Receiver MAC, which includes S-MAC [5], Low Power Listening (LPL) [6] and WiseMAC [7], has been developed. Using Cycled Receiver MAC, each node enters a receiving mode only during a specific wakeup duration time that occurs in every wakeup period. Reducing the duty cycle ratio, the power used for idle listening is also decreasing. In general, with a cycled receiver MAC, the longer the wakeup period, the longer the delay time for connection establishment. Therefore, under the condition of the same duty cycle ratio, the shorter wakeup period, the more advantageous it can be in terms of the delayed time.

Our proposed Isochronous-MAC (I-MAC) [4], [8] is based on LPL that has a periodic wakeup time. I-MAC also has a periodic wakeup time, but it is synchronized on each node with the actual time, using the Long-Wave Standard Time Code (so called "wave clock"). Since a sender can predicts a next wakeup time of an intended receiver with high accuracy, we can minimize the duration of a preamble on the sender. As well as on the receiver side, the receiving time for the preamble can be reduced thanks to the short duration of the preamble.

In [2], TICER [3] is implemented as a MAC, in which a sender node periodically repeats wakeups and sleeps in a preamble operation when establishing communication with receiver nodes (Fig. 2). In the figure, T is a receiver's wakeup period, and T_{on} is a carrier sense time; as T becomes larger, the power of TICER becomes larger, since a number of preambles must be tried.

Refer to [4] for more detail on the I-MAC.

2.2 Time Synchronization

In [8], the time on sensor nodes are adjusted to the actual time using the Long-Wave Standard Time Code. However, external hardware is required for this method, and it does not work indoors. Therefore, in this paper, we examine another time synchronization technique.

The time synchronization methods in wireless sensor networks are classified into two types: using an external signal and exchanging the synchronous packets.

- The type using an external signal such as GPS and the wave clock is easily adopted, and nodes can be synchronized by itself. This type of method, however, cannot be utilized in a place where the synchronous signal cannot be received (e.g. indoor). Moreover, this implementation needs external hardware to receive external signal.
- In contrast, packet exchanging method methods do not require external hardware or signal. Reference Broadcast Synchronization (RBS) [9], Timing-sync Protocol for Sensor Networks (TPSN) [10], Flooding Time Synchronization Protocol (FTSP) [11] are classified in the packet exchanging method. They correct the time by using time stamp packet communication, although a communication overhead is required.

Table 1 Time synchronization techniques in the sensor network.

		Additional hardware	Sync packet	Accuracy	Power
Using external signal	Wave clock	Need	No need	Low	Small
	GPS	Need	No need	High	Large
Using packet exchange	RBS	No need	Bidirectional	Low	Large
	TPSN	No need	Bidirectional	High	Medium
	FTSP	No need	Unidirectional	High	Small

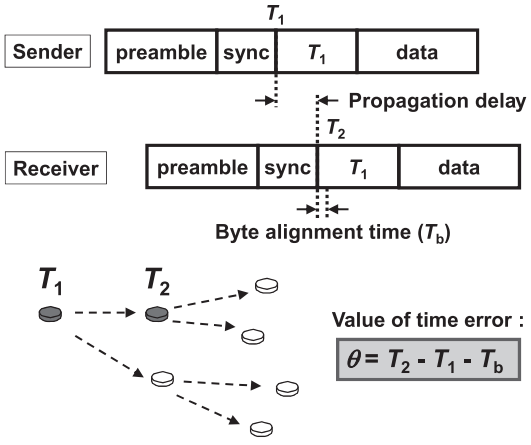

Fig. 3 Synchronization method of the FTSP.

The characteristic of various methods is summarized in Table 1.

As the time synchronous technique of the sensor node LSI, we chose FTSP in consideration of the balance of hardware and power overhead. Figure 3 shows the synchronization method of the FTSP algorithm. First, the synchronous packet is flooding from the root node. At this time, the time stamp of T1 is send to the receiver node. Next, the receiver node records the time stamp of T2 at the end of the synchronous packet. Then T2-T1 means the sum of the propagation delay and the difference of the timers between a sender and a receiver. However, note that, until the synchronous packet is recognized by a system, there is a time of Tb as a byte alignment time. This can be calculated by the data rate, and after that, the time error is corrected with T2-T1-Tb in the receiver node.

When the synchronous process of the FTSP is completed, the time lag among sensor nodes is from 1 μ second to 10 μ seconds, and this value does not depend on the propagation delay [11]. Moreover, from [8], the maximum time lag is 240 μ seconds when executing 50 times synchronization on a day with the 32.768 kHz real time clock (TG-3530SA; EPSON TOYOCOM [12]). Therefore, the total time lag among sensor nodes is suppressed by 250 μ seconds at maximum. From [4], time lag of 250 μ seconds is sufficiently small value in order to operate I-MAC.

In addition to the above, there are two other reasons why we chose the FTSP for our system.

The first reason is that the I-MAC does not need to synchronize the time of the entire network. In the multi-hop sensor networks, it is difficult to synchronize the time of the entire network with high precision. Since FTSP uses flooding, it is hard to avoid the error by data relay. Nevertheless, only by synchronizing the time between a node and its one-hop neighbor, the I-MAC can organize communication. Moreover, although the power consumption of the I-MAC is dependent on a preamble length, its length can be determined only by the time drift over a one-hop neighbor.

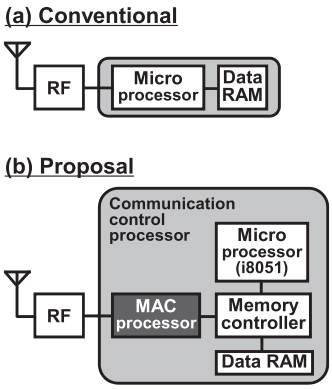

Fig. 4 Communication processing method of a conventional sensor node (a), and proposal sensor node (b).

The second reason is that we assume data collection type application in this research. In order to collect sensing data, it is necessary to construct routes from a base station to each node in the network. In many routing protocols, the route is constructed by using flooding. (e.g. Directed Diffusion [13] and Tiny Diffusion [14]). Therefore, since the time synchronization by using FTSP and the construction of a route can be executed simultaneously, the flooding operation does not become overhead.

2.3 Communication Control Processor

In the conventional sensor nodes [15]–[17], all of the communication protocol (e.g. MAC layer, network layer, and application layer) is processed by micro controller (Fig. 4(a)). However, the micro controller is dealing with the process of the MAC layer in most of the time, because the sensor networks usually use a simple transmission method and a lower data rate to reduce power consumption of the RF circuits. Hence the processing power during data communication becomes relatively high.

To overcome the above problem, we propose a communication control processor which consists of a MAC processor, i8051 microcontroller, and data memory (Fig. 4(b)). The MAC processor is a dedicated hardware for the communication processing in the I-MAC. Then i8051 deals with only upper layers than the MAC layer (e.g. time synchronization, rooting, and sensor input).

Figure 5 is the state transition diagram of the I-MAC.

- In "Sampling preamble," the node transits from the "Sleep" state to "RX" state periodically for carrier sense.
- If a sender exists in the surroundings, the node will re-

ceive data after the carrier sense. After the data reception is completed, the node transits in the "TX" state to return the ACK ("Receiving data" in Fig. 5).

- On the other hand, if the node stores data to transmit, it will be transmitted after carrier sense and the ACK will be received ("Transmitting data" in Fig. 5).

This state transition can be simplified because all nodes are synchronized and thus can predict their operations. Hence, a simple processor for the I-MAC can be implemented as dedicated hardware.

Figure 6 illustrates the communication scheme of I-MAC. This process is repeated whenever communication occurs between nodes. In the figure, Preamble is composed of data of continuous "1," STX (Start of TeXt) and ETX (End of TeXt) are the octet sequence "01111110."

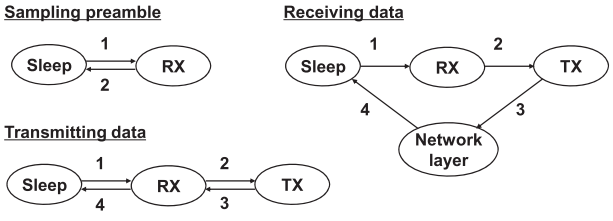

Fig. 5 State transition of I-MAC.

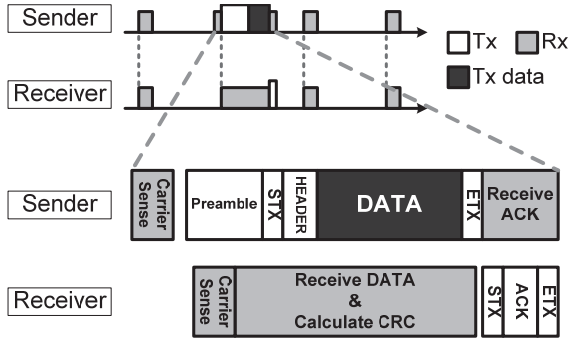

Fig. 6 The communicate scheme of I-MAC.

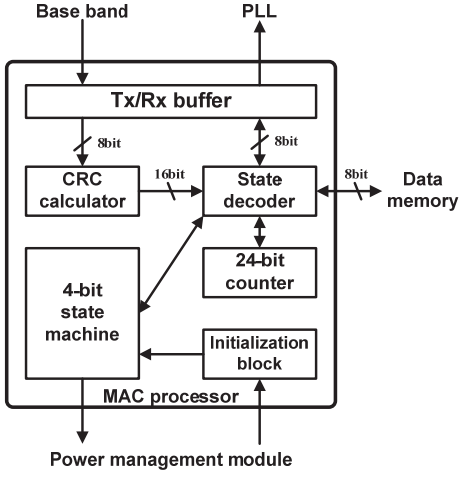

Fig. 7 Block diagram of the MAC processor.

HEADER consists of 16 bits of sender node ID, 16 bits of receiver node ID, 8 bits of control flags, and data comprised of 8-bit blocks. The minimum size of Data is 8 bytes and the maximum size is 1 kbyte. A CRC-16 is attached to the last of a data frame.

Figure 7 illustrates the block diagram of MAC processor. The MAC processor is constituted by 4-bit state machine, decoder, TX/RX buffer, CRC calculator, 24-bit counter, and initialization block. The state machine realizes the communication scheme in Fig. 6. The initialization block initializes the node in the power-on sequence. This is because the MAC processor is a core of the power supply control mechanism which will be described in Sect. 3. Although the main part of the state machine of I-MAC operates at 1MHz, and the clock to the TX/RX buffer and the CRC calculator is power-gated according to the state.

3. Sensor Node Architecture and Implementation

In this section we describe the architecture of the sensor node LSI, and power reduction techniques in it. Figure 8 shows the overall view of the proposed sensor node LSI that includes a transceiver (TX/RX), microcontroller, and power management module (PMM). The compositions of the transceiver and the PMM are shown in the figure.

3.1 Transceiver

In Fig. 8, the TX is comprised of a PLL and power amplifier (PA). Generally, it is difficult to increase output efficiency of a PA because transmitting power is small in a WSN. In [1], the output power efficiency is 16.5% at 1.46 dBm. We propose a higher-efficiency PA using an oscillator with multi-phase outputs. Figure 9 shows the schematics of the proposed oscillator and combination with the PA. The multi-phase oscillator has four five-stage ring oscillators, connected by interpolators; 20-phase square waves are output at every 18 degrees. The PA has ten phase-modulated class-D amplifiers in parallel. Each class-D amplifier is controlled by other phases, which reduces short current through the PA in an active mode. Figure 10 shows the relationship between the conduction angle and power efficiency. The maximum power efficiency achieves 17.9% at 1.45 dBm without any

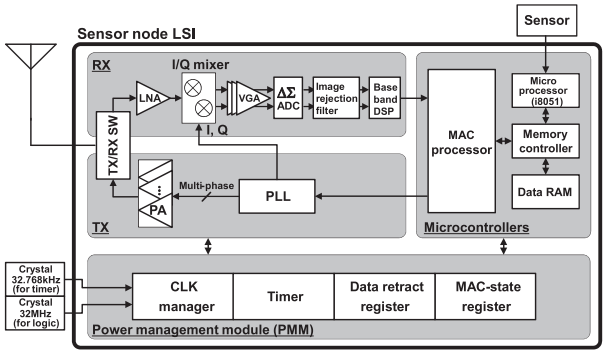

Fig. 8 Block diagram of the sensor node LSI.

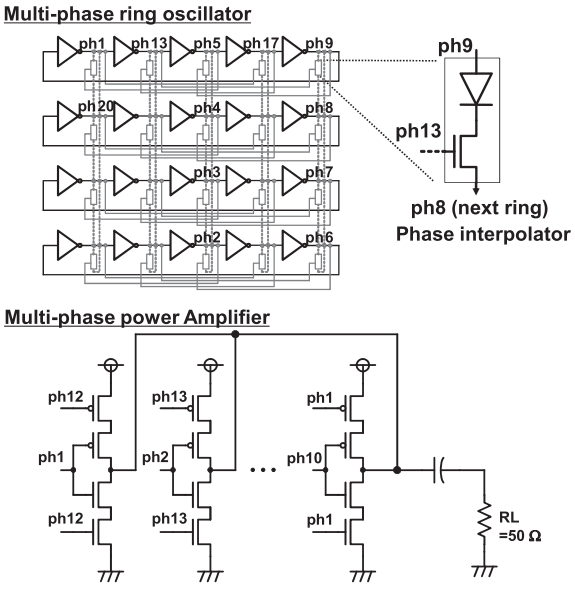

Fig. 9 Multi-phase oscillator and power amplifier.

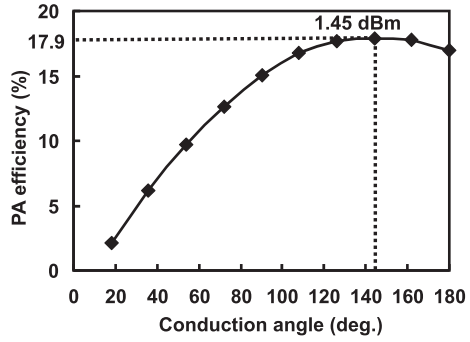

Fig. 10 PA efficiency.

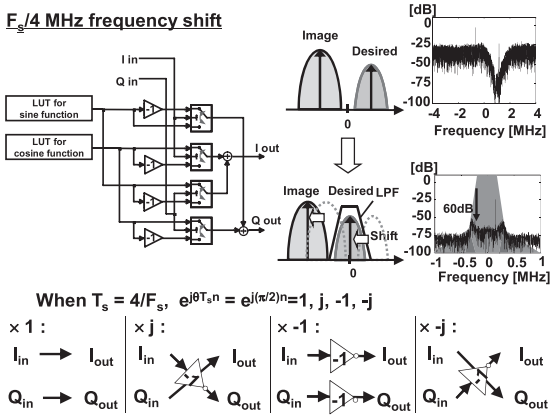

Fig. 11 Digital image rejection scheme using frequency shift.

MEMS or inductors.

In the RX part, we adopted a low-IF architecture. The I/Q mixer also exploits the multi phases for I/Q separation. A complex band-pass delta-sigma ADC converts the I/Q signals to quantized signals. Then, a digital image rejection filter selects a desired bandwidth. The image signal rejection is digitally-assisted without analog circuits. Figure 11 shows the basis of the digital image rejection. Fs/4 frequency shifting is carried out by multiplying the 1, −1, j, −j by the I/Q signals; considering the I/Q signals in a discrete time domain, it equals multiplying by $e^{j(\pi/2)n}$ when n = 1/4. The manipulation can be achieved only by forwarding, inverting or changing the I/Q signals. This frequency shifting technique does not incur additional image signals in principle. Once the desired bandwidth is shifted, it can be filtered out by a low-pass filter (decimation filter); the decimation filter is concurrently used for decimation and image rejection. The image rejection ratio is 60 dB when the frequency shifting is set to 1 MHz. The digital image rejection filters can remove conventional SAW filters. As the final stage of the RX, the baseband DSP demodulates FSK. The RX achieves a bit error rate below 10^{-5} at a data rate of 60 kbps and at an SNR of 7.8 dB.

3.2 Power Management

Generally a sensor node has a low duty cycle (less than 1%, [18]) to reduce power consumption. The purpose of communication centric design is the active time reduction of RF circuits, and this also equivalent to the increase in sleep time. Therefore, it is important for the life time of a sensor node to reduce the power consumption during sleep period. The power gating is the effective way.

The proposed sensor node has the PMM which controls the power supplies of the components, based on the state transition of MAC processor. The state of the power supply in each functional block depends on the state transition of I-MAC. For this reason, the sequencer only for power supply management has been designed so that efficient power supply management can be realized.

The PMM consists of a clock manager, timer, data retract register, and MAC state register (see Fig. 8). The state of the MAC processor is stored in the MAC-state register. According to this state register, a clock and a power supply of each block are cut off. Table 3 shows the condition of the power supply and the clock of each module for every state of the I-MAC (Fig. 5). The timer is operated at 32.768 kHz and counts up the internal time. In a sleep state, only the timer is activated. By receiving a interrupt signal from the timer, the node moves to the RX state.

4. VLSI Measurement

Table 2 shows the specifications of the sensor nodes. Figure 12 depicts the chip micrograph. The test chip was fabricated in a 180-nm CMOS process and the area is $3 \times 3\,\mathrm{mm}^2$. The power of each component is shown in Table 3.

We verified the average energy in data-gathering operation on a network level using network simulator: QualNet [19]. Network simulation is very important to estimate power because nodes' powers are not uniform; a node near a base station consumes more power to process gath-

Table 2 The specification of the sensor node VLSI.

System	
Process	CMOS 180nm
Supply voltage	1.8V
Communication range	0.1-20m
Carrier frequency	433.67 - 434.17MHz
Bitrate	10 - 60kbps
Channel bandwidth	150kHz
Clock	32.768kHz, 32MHz
Frequency tolerance	+/- 20ppm
Modulation	FSK
Transceiver	
Transceiver	Low-IF
Transmitter power	9.00mW
Receiver power	12.05mW
Output power	-4dBm
RX sensibility	-72.8dBm (For 1E-5 BER)

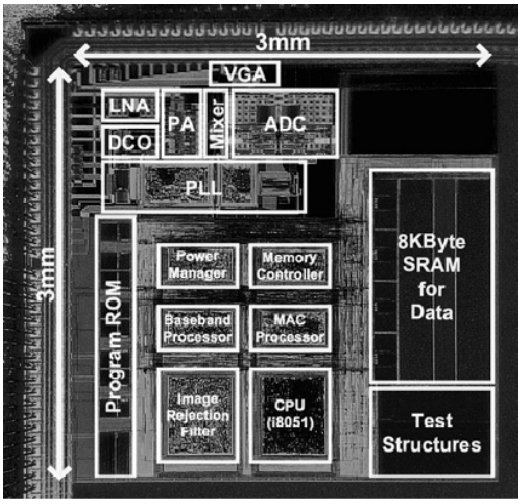

Fig. 12 Chip micrograph.

Table 3 Block power of each module and total power in each state.

		Block power	State of a sensor node			
		Dynamic/Leak	Sleep	TX	RX	Network layer
LNA		1.17mW/-	OFF	OFF	ON	OFF
PA		4.26mW/-	OFF	ON	OFF	OFF
PLL		3.28mW/-	OFF	ON	ON	OFF
VGA		955μW/-	OFF	OFF	ON	OFF
ADC		999μW/-	OFF	OFF	ON	OFF
Image rejection filter		2.75mW/1.02μW	OFF	OFF	ON	OFF
Baseband		1.34mW/1.4μW	OFF	OFF	ON	OFF
MAC processor		11.7μW/135nW	OFF	ON	ON	ON
Memory controller		14.4μW/88.3nW	clk gating	ON	ON	ON
Data RAM		710μW/11μW	clk gating	read	write	read/write
i8051		787μW/8.2μW	OFF	OFF	OFF	ON
PMM		3.97μW/156nW	ON	ON	ON	ON
Crystal oscillator	32.768kHz	3.6μW/-	ON	ON	ON	ON
	32MHz	2.88mW/-	OFF	ON	ON	ON
Total power			18.8μW	11.16mW	14.12mW	4.41mW

ered data whereas a peripheral node that merely sends small data results in lower power. In the network simulation, the transmission range of the node is 20 m, and the data rate is 20 kbps. The wake-up period which means wake-up interval time of each node in the network is set to 100 ms. Randomly-deployed 100 nodes in the area of $100 \times 100\,\mathrm{m}^2$ collect data to a base station at the center. Other simulation conditions are shown in Table 4.

Table 4 Simulation conditions.

Simulator	QualNet 3.8
Number of simulation	50
Application layer	Data gathering
Network layer	Tiny Diffusion [13]
Location of the base station	Center of the network area
Number of nodes	100
Node deployment	Random
Network size	100 m x 100 m
Connection range	20 m
Data rate	20 kbps
Data length	6 bytes
Average hop counts	3.07
Wake-up period	100 ms

Table 5 Average operation time.

Total time [ms]	84767.8
TX active time [ms]	22.5
RX active time [ms]	213.5
Network time [ms]	4.5
Sleep time [ms]	84527.0
Wake-up ratio [%]	0.3

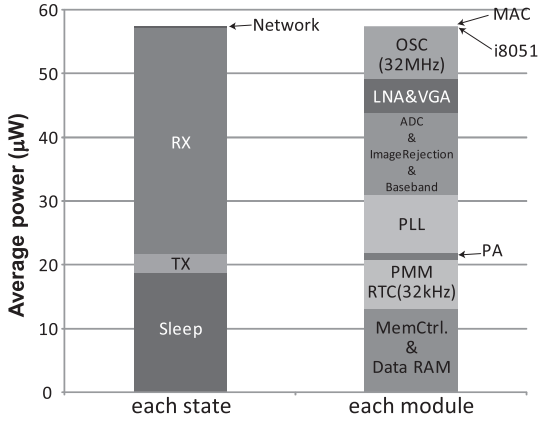

Fig. 13 Power budget of the sensor node LSI.

The average operation time of each component in collecting the data is shown in Table 5. Herein, the "total time" means time required to gather sensing data to a base station through all the nodes in the network. The wake-up ratio is 0.284%, and the proposed sensor node processor achieves a power of 58.0 μW on average. Figure 13 illustrates the power budget of the sensor node LSI.

Figure 14 compares the average power of the sensor node LSI and conventional one ([2] with TICER [3] and [1]). As for the conventional LSI, the receiver active power was 3.6 mW according to [1]. The transmitter active power is set to 8.4 mW assuming that the output power is 1.6 dBm with 17% output efficiency. As digital parts, the MAC processing active power, the network processing power, and the power consumption of the real time clock were 766 μW, 527 μW, and 10 μW, respectively in [2]. With these RF

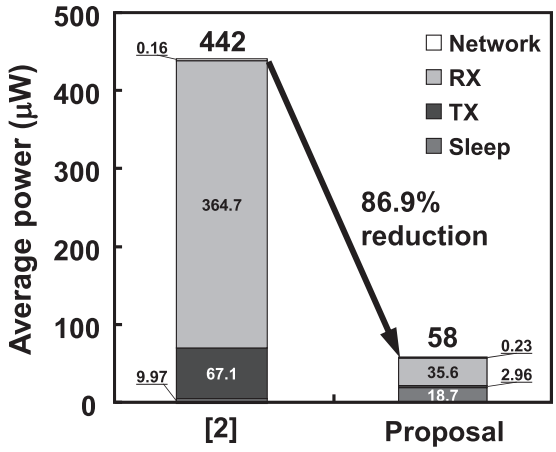

Fig. 14 Power evaluation.

and digital-part active powers, Fig. 14 illustrates the average power of the conventional LSI, considering Table 5 and the numbers of transmission and reception in a node obtained from the simulation. The RTS/CTS size and T_{on} which are the characteristic parameter of the TICER are set to 4 bytes and 6.4 ms, respectively. The sensor node LSI can reduce 86.9% of the average power.

5. Conclusion

We proposed a single-chip ultralow-power sensor node VLSI with a synchronous media access control (MAC). The communication centric design has been adopted with cross-layer techniques. The VLSI is comprised of a transceiver, i8051 micro controller, and dedicated MAC processor. The test chip occupies $3 \times 3\,\mathrm{mm}^2$ in a 180-nm CMOS process, including 1.38 M transistors. The power is 58.0 μW under a network environment.

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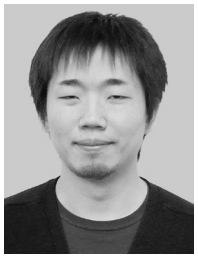

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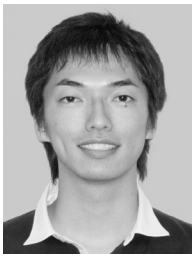

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