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A 0.15-μm FD-SOI Substrate Bias Control SRAM with Inter-Die Variability Compensation Scheme*

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SUMMARY We propose a novel substrate-bias control scheme for an FD-SOI SRAM that suppresses inter-die variability. The proposed circuits detect inter-die threshold-voltage variation automatically, and then maximize read/write margins of memory cells to supply the substrate bias. We confirmed that a 486-kb 6T SRAM operates at 0.42 V, in which an FS corner can be compared as much as 0.14 V or more.

key words: *SRAM, FD-SOI, Inter-die variation*

1. Introduction

According to the ITRS Roadmap [1], the capacity of SRAM is becoming larger on an LSI using advanced CMOS processing. The SRAM operating margin, however, is degraded by variation of a threshold voltage ($V_{\rm th}$), which implies that the SRAM is the most sensitive part to the threshold variation and that it therefore dominates operating margins on a whole chip. It is important to prevent operating errors caused by the $V_{\rm th}$ variability and to maintain operating margins.

To suppress inter-die variation, a body-bias control scheme was proposed in a classical bulk process [2]. In the bulk process, however, the body bias is limited to around 0.6 V because of forward junction leakage; the threshold-voltage compensation turns out in a small range. To make matters worse, a reverse bias incurs gate-induced drain lowering (GIDL) in a short-channel bulk process. Another bac kgate-bias control scheme in an FD-SOI process adaptively changes the bac kgate bias of memory cells in read and write operations [3]; this scheme, however, has a cycle-time penalty because the bac kgate bias control must be made in every read and write operation. Furthermore, bac kgate contacts pay an area overhead in a bitcell array because the bac kgate bias is controlled on a block basis in such a scheme.

In this paper, we propose an FD-SOI SRAM with substrate bias control to compensate inter-die variation. The proposed scheme detects the inter-die threshold voltage variation (systematic variation) automatically, and compensates the threshold voltage using substrate bias control.

In the next section, we describe the proposed inter-die variation compensation techniques. In Sect. 3, we explain the proposed substrate bias control scheme. In Sect. 4, we introduce the measurement results of the test chip, which is a 486-kb 6T SRAM with the proposed substrate bias scheme. The final section summarizes this paper.

2. Substrate Bias Control for Inter-Die Variation Compensation

In this section, we describe the relation between the systematic variation and SRAM margins. Figure 1 shows a schematic of an FD-SOI device structure and a 6T bitcell. The 6T bitcell comprises access transistors (A0, A1), drive transistors (D0, D1), and load transistors (L0, L1). Applying a bias through the substrate to the FD-SOI device, the substrate nodes of all transistors are controlled collectively.

In a 6T SRAM, the respective FS and SF corners determine minimum read and write operating voltages [4]. Because an FD-SOI has smaller intra-die variation than a bulk

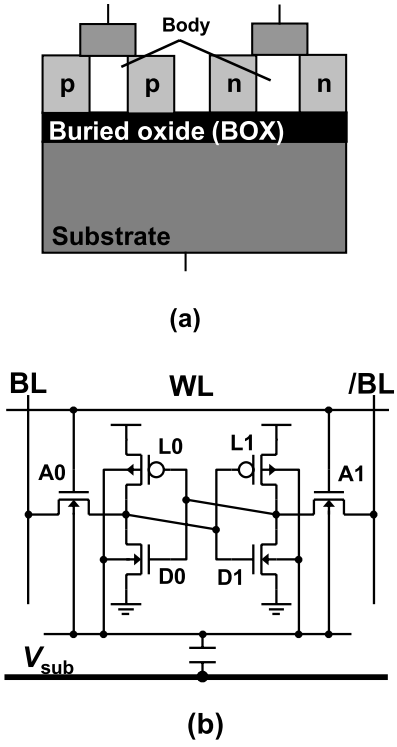

Fig. 1 (a) FD-SOI device structure and (b) 6T bitcell.

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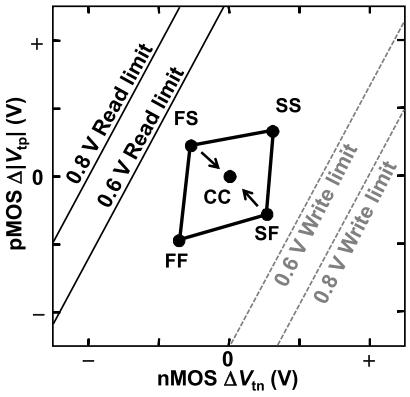


Fig. 2 Read/write margins in Yamaoka plot.

process [5], the systematic variation from the FS to SF corners affects the yield of SRAM more directly. Figure 2 shows a Yamaoka plot [4] illustrating the relation between the process corners and read/write margins when a supply voltage (V_{dd}) is changed. Both the read margin at the FS corner and the write margin at the SF corner must be regarded as achieving stable operation.

To sustain the SRAM operating margin, the inter-die variations must be suppressed. As Fig. 2 shows, the FS/SF corner can converge on the CC corner with an FD-SOI substrate bias (this mechanism is explained in the next section), which means that the inter-die variation suppression enhances the operating margin.

3. Proposed Substrate Bias Control Scheme

3.1 Substrate Bias Effect

Figure 3 shows measured I_d–V_{gs} curves of an FD-SOI nMOS and pMOS, respectively, when a substrate bias (V_{sub}) is applied from a substrate (see Fig. 1(a)). The forward bias increases an nMOS threshold voltage (V_{tn}) and decreases the pMOS threshold voltage ($|V_{tp}|$), whereas their reverse bias exhibits the opposite characteristics. In other words, the FS and SF corners can converge on the CC corner after applying an appropriate substrate bias, as shown in Fig. 2. This substrate bias control changes the threshold voltages of all nMOSes and pMOSes on the substrate. Therefore in the proposed scheme, no area overhead exists in the bitcell itself for the substrate bias control (Fig. 1(b)). In a future advanced process, the substrate bias can be lowered because the buried oxide is thinning.

3.2 Circuitry

Figure 4 depicts a block diagram of the proposed substrate-bias control circuits. The proposed circuit consists of a V_{th} detector, half-V_{dd} generator, comparator, and substrate bias generator.

The schematic of the V_{th} detector is shown in Fig. 5. The V_{th} detector outputs information on the inter-die variation as a "Detect" signal. N0 and P0 are diode-connected,

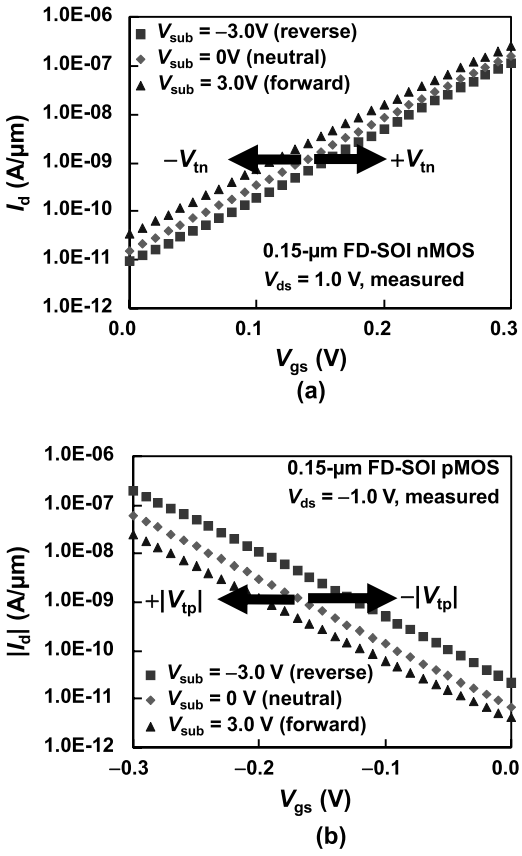


Fig. 3 I_d–V_{gs} characteristics of (a) nMOS and (b) pMOS.

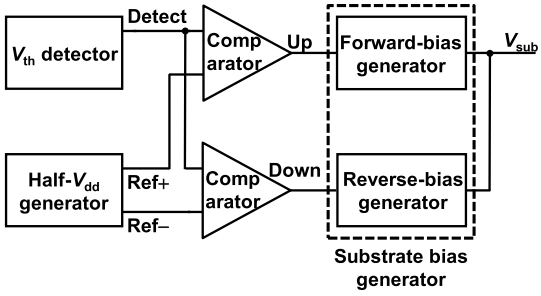


Fig. 4 Proposed substrate bias control circuits block diagram.

whose source nodes output $V_{dd} - V_{tn}$ and $|V_{tp}|$ (so called "V_{th} drop voltages"), respectively. Thus, the gate biases with P1 and N1 result in V_{tn} and $|V_{tp}|$, respectively. At the CC corner, P1 and N1 are sized so that $V_{dd}/2$ is output as the "Detect" signal; thereby, at the FS corner, "Detect" goes down because V_{tn} and $|V_{tp}|$ become smaller and larger, respectively. On the other hand, at the SF corner, the situation is the opposite; "Detect" goes up. Figure 6 shows the simulation result of the V_{th} detector. At the SS or FF corner, "Detect" is around $V_{dd}/2$ because the mismatch between V_{tn} and $|V_{tp}|$ is relatively small. To sense the process corner, we compare "Detect" with $V_{dd}/2$ in our proposed scheme.

The half-V_{dd} generator using body-tie transistors in Fig. 7 provides slightly higher and lower voltages than $V_{dd}/2$

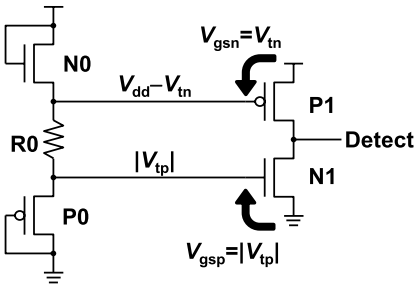


Fig. 5 V_{th} detector.

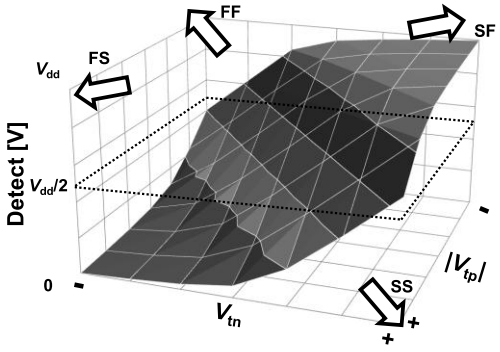


Fig. 6 Simulated "Detect" voltage of V_{th} detector.

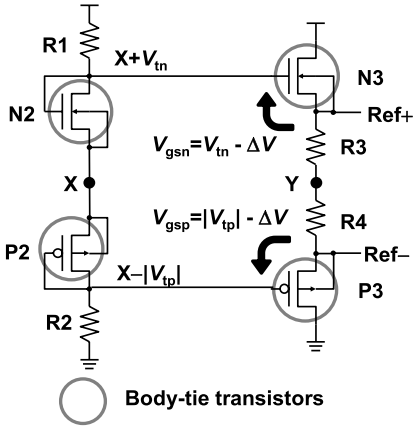


Fig. 7 Half-V_{dd} generator.

("Ref+" and "Ref−"), irrespective of process variation, which are to be compared with "Detect" in the comparators. The half-V_{dd} generator is based on the circuit in [6]. R1 and R2 have high enough resistances. At the CC corner, N2 and P2 are sized so that the node X is kept at $V_{dd}/2$. As well, N3 and P3 are sized so that the node Y is kept at $V_{dd}/2$ at the CC corner. In this case, N3 and P3 have gate biases of $V_{tn} - \Delta V$ and $|V_{tp}| - \Delta V$, respectively (where ΔV is a voltage drop by R3 or R4). Consequently, both of N3 and P3 are weakly turned on; small subthreshold current merely flows through them. At the skewed (SF or FS) corner, V_{tn} and $|V_{tp}|$ becomes unbalanced; the node X's voltage is not, however, changed very much because R1 and R2 are high enough. Thereby, the node Y's voltage stays at around

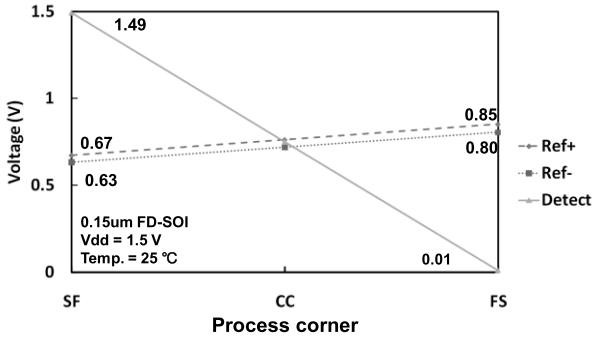


Fig. 8 Simulated output voltages of V_{th} detector and half-V_{dd} generator.

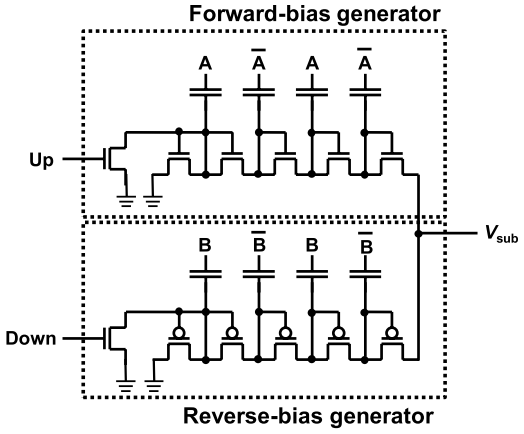


Fig. 9 Substrate bias generator.

$V_{dd}/2$; so "Ref+" and "Ref−" do. Figure 8 shows simulated outputs of the V_{th} detector and the half-V_{dd} generator. At the SF and FS corners, "Ref+" ("Ref−") voltages are 0.67 V (0.63 V) and 0.85 V (0.80 V), respectively. At the SS and FF corners, the output voltages' changes are smaller than those at the SF and FS corners; they are 0.74 V (0.71 V) and 0.79 V (0.73 V), respectively. According to the comparators' outputs, the substrate bias is controlled so that "Detect" is always between "Ref+" and "Ref−". In this way, the FS and SF corners converge on the CC corner. For the reason mentioned above, at the SS and FF corners, the V_{th} detector and the half-V_{dd} generator act like at the CC corner; the substrate bias control needs not be applied for improving the operating margin.

The substrate bias generator, including a forward-bias generator and reverse-bias generator, consists of two Dickson-type charge pump circuits [7]. Figure 9 portrays a schematic of the substrate bias generator. The forward-bias generator and the reverse-bias generator respectively include nMOSes and pMOSes. To prevent a gate oxide breakdown cause by a higher (lower) voltage than a nominal supply voltage, these transistors in the charge pump circuits use high-voltage I/O transistors. The bias generator can charge/discharge the output voltage (V_{sub}) by non-overlap clock signals (A and /A, B and /B). The forward bias gets started with an "Up" signal, whereas the negative bias does

so by a "Down" signal. Figure 10 shows simulation waveforms of the bias generators. The forward bias generator and the reverse bias generator output up to 4.3 V and down to −4.2 V, respectively. In a future FD-SOI process technology, smaller-voltage substrate control might be achieved with low-voltage core transistors because the buried oxide will become thinner.

If a die is at the CC corner, then the comparators output neither an "Up" nor "Down" signal. Therefore, the substrate bias is retained by a substrate capacitance.

Figure 11 presents the simulation waveforms of the proposed substrate-bias generator block in dynamic operation. Assuming that V_{tn} and $|V_{tp}|$ are respectively high and low by the inter-die variation (namely, the SF corner), the V_{th} detector outputs the "Detect" signal higher than $V_{dd}/2$ at first. Then, "Up" makes the substrate bias forward and V_{sub} increases to converge on the CC corner, which lowers V_{tn} and raises $|V_{tp}|$. Because V_{tn} and $|V_{tp}|$ are close to the CC corner, "Detect" decreases and becomes lower than "Ref+"; at that time, "Up" is deactivated and V_{sub} is retained. However, V_{sub} is changed gradually because of leakage current of the substrate bias generator, which again locks "Detect" out. In turn, "Detect" is locked on and out at a very low frequency, V_{sub} is finally stabilized. In the proposed substrate control circuits, the power consumption is 117 μW:

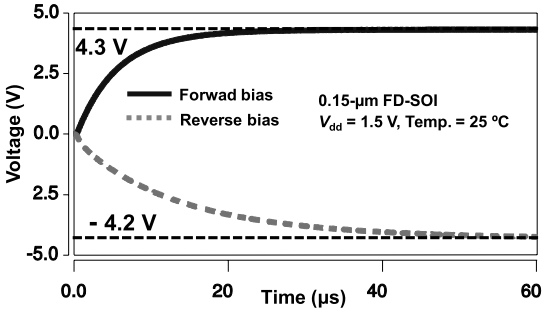


Fig. 10 Simulated waveforms of substrate bias generator.

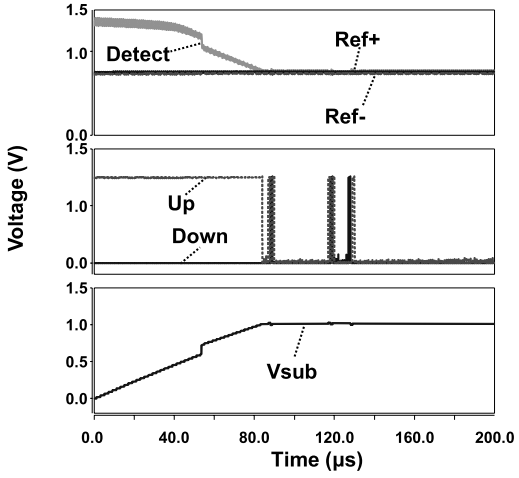


Fig. 11 Simulated waveforms of the proposed substrate bias control scheme (dynamic operation).

The half-V_{dd} generator, and V_{th} detector, and substrate bias generator respectively consume 23 μW, 22 μW, and 72 μW.

4. Measurement Results

Figure 12 presents a test chip micrograph. The test chip is fabricated with a 0.15-μm FD-SOI process technology. The test chip is a 486-kb (512 rows × 8 columns × 14 bits/word × 9 blocks) 6T FD-SOI SRAM with substrate bias control.

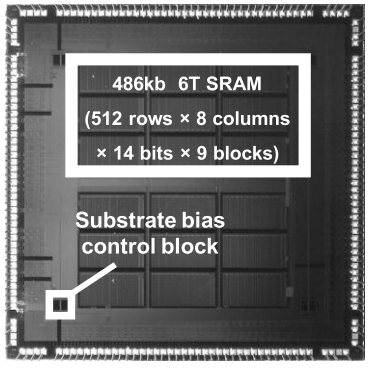
4.1 Bit Error Rates of 6T SRAM

Figure 13 shows the measured bit error rates (BERs) at the FS corner. Figure 13(a) is a case of read operation; the minimum read operating voltage (V_{min_r}) is 0.56 V when V_{sub} = 0 V. By applying the reverse bias (−4 V), V_{min_r} is imposed to 0.42 V. In contrast, the forward bias degrades the read margin.

Figure 13(b) shows a retention case. The retention voltage is 0.36 V at neutral bias. It is improved at the reverse bias as well as the read operation.

Figure 13(c) is the BER in the write operation. At neutral bias, the minimum write operating voltage (V_{min_w}) is 0.36 V. Although V_{min_w} must be degraded with the reverse bias physically, it is improved when $V_{sub} = -2$ V because the retention voltage governs the write margin on this condition. As the reverse bias deepens to less than −2 V, V_{min_w} worsens again, which is physically reasonable.

If the test chip was at the SF corner, the minimum operating voltage could be improved by applying the opposite substrate bias. As mentioned in Sect. 2, the write margin determines the minimum operating voltage at the SF corner; V_{min_w} would be improved by applying a forward bias.



Process	0.15 μm
Process corner	FS corner
SRAM cell	6T bitcell
Capacity	486 kb (512 rows ×8 columns × 14 bits ×9blocks)

Fig. 12 486-kb 6T SRAM in 0.15-μm FD-SOI process.

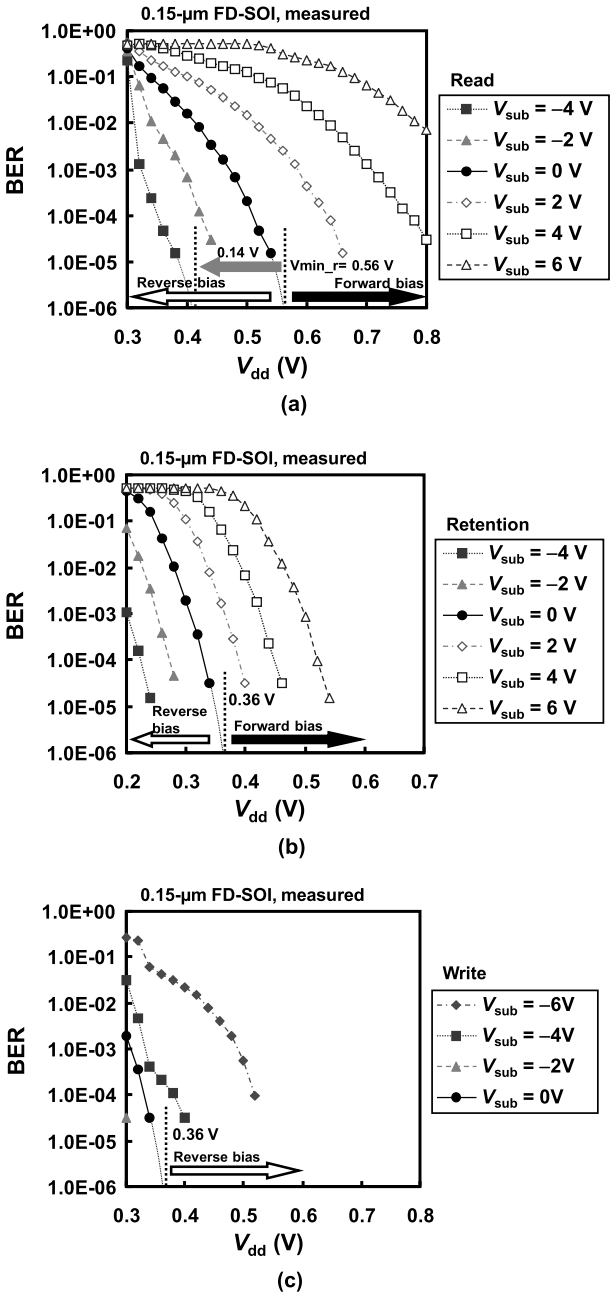


Fig. 13 Measured BERs: (a) read, (b) retain, and (c) write.

4.2 Leakage Reduction

We measured leakage power on the test chip. When V_{sub} = −4 V, we confirmed that the 486-kb SRAM functions well at 0.42 V. In this case, V_{min_r} is compensated as much as 0.14 V. It is noteworthy that the low-voltage operation is also effective for gate leakage and NBTI in the future process.

Figure 14 exhibits the leakage power reduction by 40% in the SRAM itself. In reality, the proposed scheme has to incorporate the substrate bias control circuits that consume certain power. In our design, the total leakage power with the proposed inter-die compensation scheme turns out larger because the substrate bias circuits dissipate 117 μW. In an advanced process, the power overhead will, however, become relatively smaller; the SRAM's leakage power is increasing due to a large capacity and a low V_{th}. The power of the substrate bias circuit will be reduced in the advanced process because the substrate bias will be lowered due to the thinning buried oxide, as mentioned in Sect. 3.1.

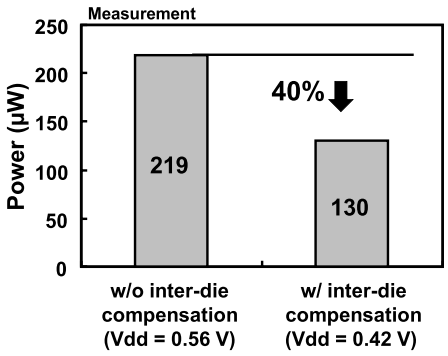


Fig. 14 Measured leakage powers.

5. Conclusion and Discussion

We proposed a novel substrate-bias control scheme for FD-SOI SRAM. We implemented a test chip fabricated using the 0.15-μm FD-SOI process. We confirmed that the 486-kb 6T SRAM operates at 0.56 V in a read operation when V_{sub} = 0 V. By applying the reverse bias (−4 V), V_{min_r} is imposed to 0.42 V.

As a future direction, we can consider that the proposed scheme is able to be combined with other techniques that suppress intra-die variation [8]–[12]; the combination will minimize both inter-die and intra-die variation.

Acknowledgments

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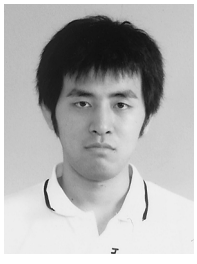

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