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Bit-Error and Soft-Error Resilient 7T/14T SRAM with 150-nm FD-SOI Process*

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SUMMARY This paper presents measurement results of bit error rate (BER) and soft error rate (SER) improvement on 150-nm FD-SOI 7T/14T (7-transistor/14-transistor) SRAM test chips. The reliability of the 7T/14T SRAM can be dynamically changed by a control signal depending on an operating condition and application. The 14T dependable mode allocates one bit in a 14T cell and improves the BER in a read operation and SER in a retention state, simultaneously. We investigate its error rate mitigating mechanisms using Synopsys TCAD simulator. In our measurements, the minimum operating voltage was improved by 100 mV, the alpha-induced SER was suppressed by 80.0%, and the neutron-induced SER was decreased by 34.4% in the 14T dependable mode over the 7T normal mode.

key words: *SRAM, single-event upset (SEU), bit error rate (BER), soft error rate (SER), neutron particle, alpha particle*

1. Introduction

Static random access memory (SRAM) is compatible with CMOS process technology. It is used as on-chip cache and embedded memory in processors and system-on-a-chip (SoC) applications. These days, SRAM occupies an area of 90% or more of a silicon die [1], meaning that SRAM is the device that is most sensitive to process variation and soft error. An SRAM on a silicon-on-insulator (SOI) substrate has one-half the threshold voltage (Vth) variation and one-third to one-fifth soft error rate (SER) of a bulk CMOS [2], [3], but it has still crucial problems to the SER and bit error rate (BER):

- BER: The variation in process parameters hinders low-voltage operation. Disturbance to a static noise margin (SNM) in read operations particularly degrades the BER.

- SER: The critical charge (Qcrit) decreases with process scaling [4]. An ionizing particle passing through a Si (silicon) substrate generates electron-hole pairs, which possibly flip a datum in SRAM. A neutron does not ionize Si directly, but generates electron-hole pairs via secondary ions as nuclear reactions [5]. The SOI SRAM collects a lesser electron charge by the funnel effect, but the collected charge is amplified by the parasitic bipolar effect, which causes a single event upset (SEU) [6]. The SEU is suppressed by an error correction code (ECC) [7] or triple modular redundancy (TMR) [8]. However, the ECC and TMR have large area overheads and access time penalties.

Many types of SRAM cells have been proposed to overcome these problems. References [9], [10] introduce a 10T or 8T cell which eliminates the disturbance to read/write operations. Other papers present SER-improved SRAM using a self-feedback mechanism [11], [12]. However, these SRAM cells cannot address the bit error and soft error problems, simultaneously.

We have proposed a 7T/14T (7-transistor/14-transistor) SRAM with a dependable mode for low-voltage operation [13]. Figure 1 portrays the 7T/14T SRAM structure. As well as the conventional 6T cell, the normal mode allocates one bit in a 7T cell while the dependable mode does so in a 14T cell by enabling a CTRL signal (CP0 and CP1 are activated). In the 14T dependable mode, either wordline, WLA or WLB, is asserted, which enlarges an SNM because a β ratio (a ratio of the driver transistor's size to the access transistor's size) is doubled. Thus, the reliability of the proposed cell can be dynamically changed depending on an operating condition. For instance, the 7T/14T SRAM is able to be

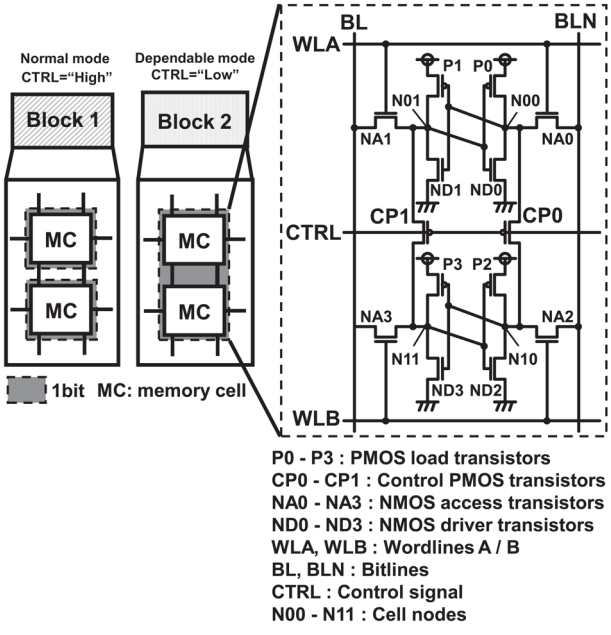

Fig. 1 Structure of 7T/14T SRAM cell [13].

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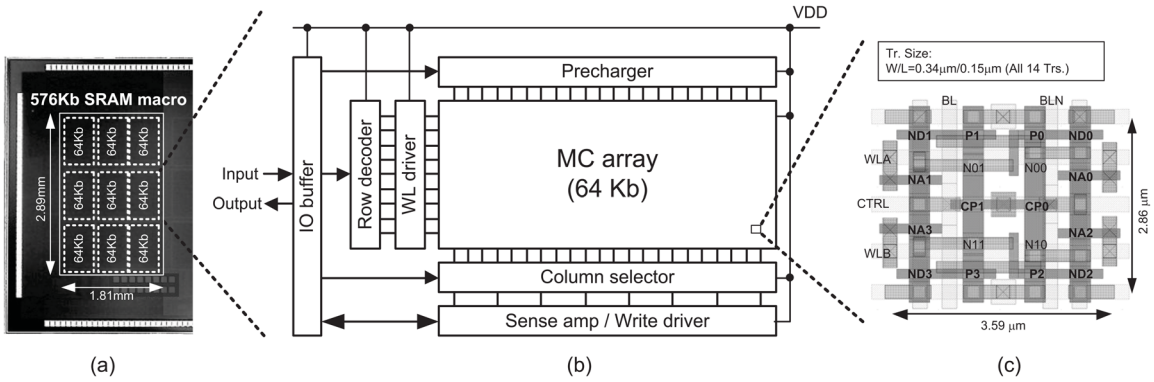

Fig. 2 (a) Chip micrograph, (b) block diagram of 64-Kb bank, and (c) 7T/14T SRAM cell layout (based on logic rule).

implemented as on-chip cache memory on a processor with dynamic voltage and frequency scaling (DVFS) [14].

In this paper, with 150-nm FD-SOI 7T/14T SRAM test chips, we present not only a BER improvement but also mitigating alpha- and neutron-induced SER. We will show experimental results that the 14T dependable mode is superior to ECC and TMR in terms of BER. The respective alpha- and neutron-induced SERs in the 14T dependable mode are suppressed by 80.0% and 34.4% over the 7T normal mode because Qcrit in the 14T mode is increased by 70%, at a supply voltage of 0.3 V. Namely, the proposed 7T/14T SRAM is a dynamically hardenable device. This paper reports measurement results of a specific 150-nm FD-SOI memory; however, they will be useful for FD-SOI designers.

2. SRAM Structure

We designed and fabricated a 576-Kb SRAM macro (512 rows × 128 columns × 9 banks) with a nominal supply voltage of 1.5 V in a 150-nm FD-SOI process. Figure 2 illustrates the implemented chip micrograph, a block diagram of a 64-Kb bank, and 7T/14T SRAM cell layout. The SRAM adopts bit-interleaving technique for preventing multiple-cell upset (MCU) [15]. The 7T/14T cells are accessed by bitlines (BL/BLN), wordlines (WLA/WLB), and control signal (CTRL). Since the SRAM cell is inter connected by layer-1 metal, the bitlines vertically tracks with layer-2 metals; then the wordlines and control signal are horizontally connected using layer-3 metals. The layout is based on a logic rule; the area overheads are 9.5% and 119% in the 7T and 14T cells, respectively, over the 6T cell [16]. In contrast, the power of the 14T cell is reduced by 40% because its minimum operating voltage is lower than that of the 6T cell [16]. The double area overhead of the 14T cell might affect manufacturing defects; however, in this paper, we will focus on the investigations of the BER and SER.

Figure 3 shows operating waveforms of the 7T/14T SRAM in the write, read, and standby cycles. When the CTRL signal is disabled (CTRL is "high"), the SRAM acts as the 7T normal mode. In this case, the SNM and Qcrit

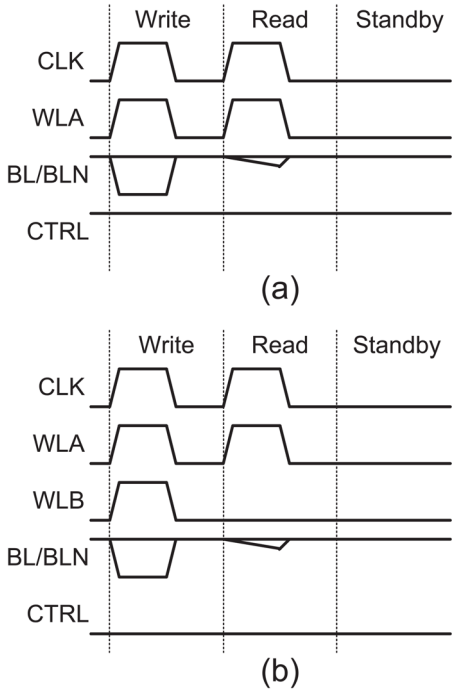

Fig. 3 Operating waveformes of (a) 7T normal mode and (b) 14T dependable mode.

are quite similar to those in the conventional 6T cell. In the 14T dependable mode, the both wordline, WLA and WLB, are simultaneously activated in the write cycle, and a single wordline, WLA, is enabled in the read cycle; thus, the write margin and SNM are enlarged, compared to the 7T mode. The CTRL signal is kept active (= "low") during a standby state in the 14T dependable mode, which improves a retention margin.

3. Simulation Results

In this section, we will present mixed-mode simulation results that the 14T dependable mode is superior to the 7T normal mode at SEU tolerance. Figure 4(a) portrays a Synopsys TCAD model [17] of ND1. The other transistors in

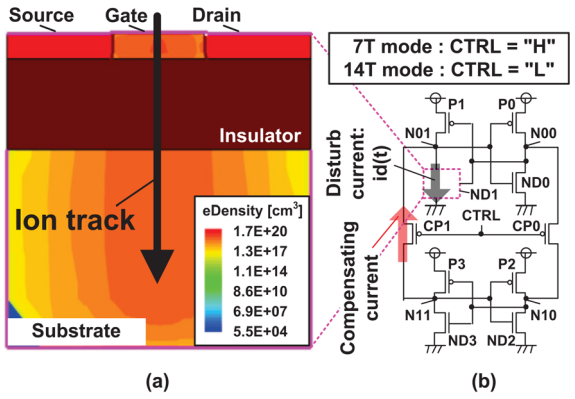

Fig. 4 (a) Cross section of nMOS (ND1) TCAD model, and (b) 7T/14T SRAM cell circuit for mixed-mode simulation using tool suite of Synopsys Sentaurus package [17].

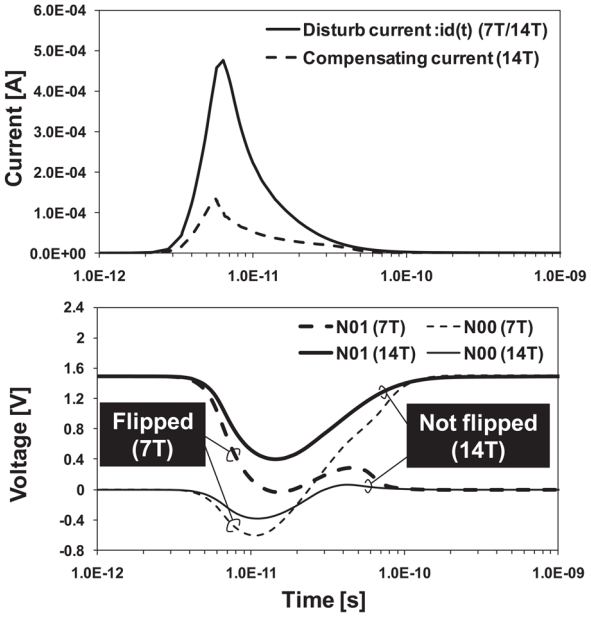

Fig. 5 Mixed-mode simultion results on the structure presented in Fig. 4. The 14T dependable cell is not flipped due to compensating current flowing through CP1. The heavy ion's LET is 0.1 pC/μm.

SRAM latches (P0, P1, P2, P3, ND0, ND2, ND3, CP0, and CP1) are based on FD-SOI SPICE models. In other words, the simulation runs in the mixed mode (TCAD model plus SPICE models). It is well known that an nMOS driver transistor connected to an "H" internal node is the most sensitive one to an SEU [18]. In this simulation, ND1 corresponds to it when N01 is "H", on which the TCAD simulation should be carried out to evaluate its nucleus reaction and secondary-ion particle transportation. The device profile and the SPICE models are provided by a foundry.

We simulate that an alpha particle whose LET is 0.1 pC/μm perpendicularly strikes the channel center of ND1. Figure 5 shows waveforms of internal nodes (N00 and N01) in the 7T/14T SRAM cell. When N01 (N00) is high (low), the ND1 transistor that has the N01 node is the

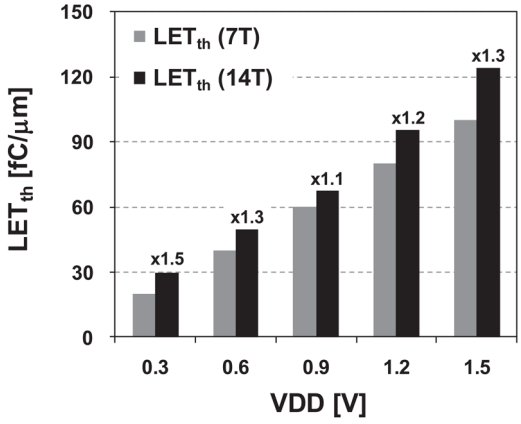

Fig. 6 Simulated LET_{th} when VDD is varied. LET_{th} in the 14T dependable mode is improved by 10–50% over the 7T normal mode.

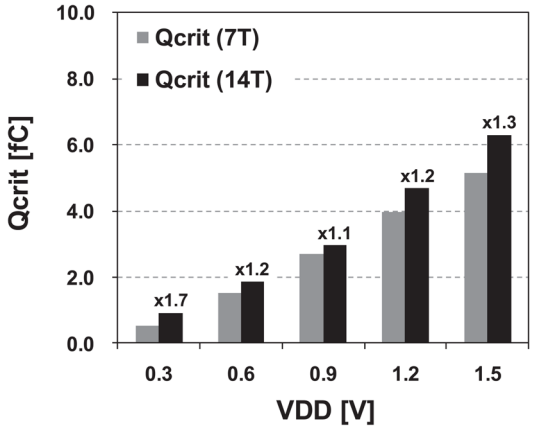

Fig. 7 Simulated Qcrit when VDD is varied. Qcrit in the 14T dependable mode is improved by 10–70% over the 7T normal mode.

most sensitive to the SEU; it is pulled down to the ground if a heavy ion strikes the ND1 transistor. The datum in the 7T cell (7T per bit) is possibly flipped by this disturb current. However, that in the 14T dependable cell can be sustained by compensating current flowing through the connecting pMOS, CP1.

We investigated the LET threshold (LET_{th}) and Qcrit; they were calculated by the following equations (1–4). LETth is a minimum LET in which a SRAM cell is flipped. Qcrit is defined as a deposited charge which is an integral of the disturb current:

$$LET_{th} = \min(LET|_{\text{SEU happens}}) \quad (1)$$

$$Qcrit = \min(\text{Deposited charge (LET)}|_{\text{SEU happens}}) \quad (2)$$

$$\text{Deposited charge (LET)} = \int_0^{10e-9} id(t, LET)dt \quad (3)$$

$$LET = 10k\ [fC/\mu m]\ (1 \le k \le 15, k \subset N) \quad (4)$$

We simulate the SEU effect over a LET range of 10–150 fC/μm. Figures 6 and 7 portray the simulated LET_{th} and Qcrit under 0.3–1.5 V operating voltages (VDD). The LET_{th} is improved by 10–50% and the Qcrit is increased by

10–70%. Because an alpha and neutron SERs are logarithmically proportional to Qcrit when Qcrit is small [4], the SERs is expected to be rapidly decreased on that condition.

In reality, the 14T cell is twice larger than the 7T cell; thus, in the 14T cell, the probability of crossing particles to the nodes turns out double. In the next section, we will compare total SERs between the 7T and 14T cells by experiment.

4. Experimental Results

4.1 Bit Error Rate (BER) Measurement

Figure 8 portrays the measured BERs in the 7T normal and 14T dependable modes. We took three steps: 1) normal write operation at 1.5 V, 2) dummy read operation for disturbance to SNM at low voltage (VDD < 1.5 V), and 3) read operation at 1.5 V. We confirmed that the BERs in the write and retention modes have much margins than that in the read disturb. So, the read operation is critical. The curves of the 7T with ECC and 7T with TMR can be calculated according (5) and (6), and shown as well in the figure.

$$\mathrm{BER}_{\mathrm{ECC}} = \mathrm{BER}_{7\mathrm{T}} \times \left[1 - (1 - \mathrm{BER}_{7\mathrm{T}})^{37}\right] \quad (5)$$

$$\mathrm{BER}_{\mathrm{TMR}} = 3 \times (\mathrm{BER}_{7\mathrm{T}})^2 - 2 \times (\mathrm{BER}_{7\mathrm{T}})^3 \quad (6)$$

The minimum operating voltages are 0.66 V, 0.60 V, 0.58 V, and 0.52 V in the 7T normal, 7T with ECC, 7T with TMR, and 14T dependable modes, respectively. The 14T dependable mode reduces the minimum operating voltage by 0.14 V, compared to the 7T normal mode.

Figure 9 illustrates overviews of 1-bit correct ECC and TMR configurations when a word width is 32 bits. The ECC includes a syndrome generator, decoder, and error correction, which needs 158% speed penalty and 18% area overhead [19]. Because the TMR simply decides its outputs by majority voting, the speed penalty is less than that in ECC. However, the area overhead is 200% due to the triple redundancy. Note that the proposed 7T/14T SRAM can also adopt these classic methods. The combination with the proposed 14T dependable mode will realize higher reliability.

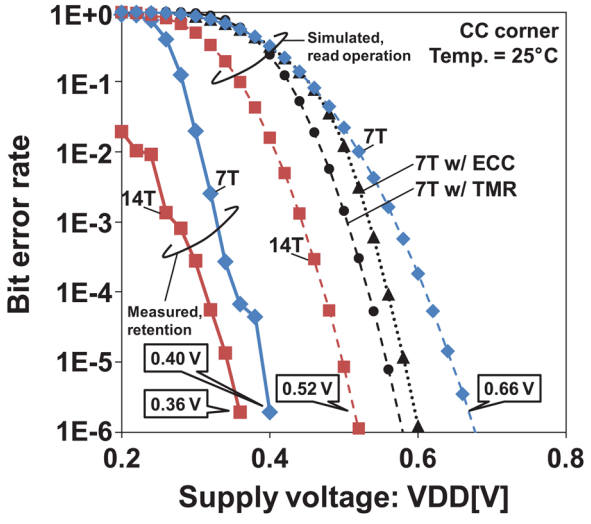

Fig. 8 BER curves: The 14T dependable mode has the smallest BER.

4.2 Soft Error Rate (SER) Measurements

Figures 10 and 11 show diagrams of the alpha and neutron accelerated tests. For an alpha particle source, Am-241 foil was used; its flux was 9×10^9 cm^{-2}h^{-1}. The foil was placed above the package [20]. A neutron irradiation experiment for SER verification was conducted at the Research Center for Nuclear Physics (RCNP), Osaka University. A neutron white beam generated by a 400-MeV proton beam irradiates a measurement board for six hours, on which three sample chips were placed (Fig. 12). The neutron flux was normalized to 3.6×10^{-3} N/cm^2-s at the ground level in New York City.

Figures 13 and 14 illustrate the alpha and neutron SERs, respectively. In these experiments, any MCU did not occur. The supply voltage was fixed to 1.5 V according to the specification of the measurement board. The alpha-induced SER is improved by 80% although the 14T cell

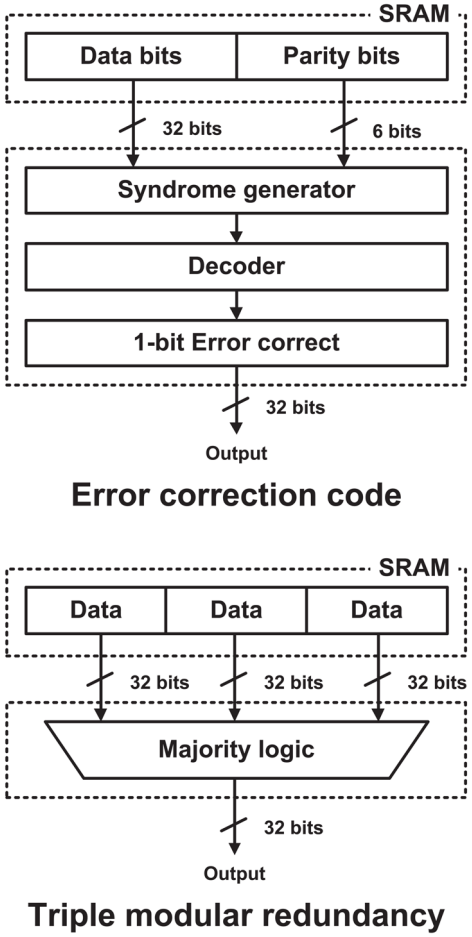

Fig. 9 Error correction code (ECC) and triple modular redundancy (TMR).

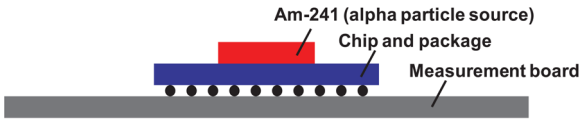

Fig. 10 Experiment diagram of alpha accelerated test.

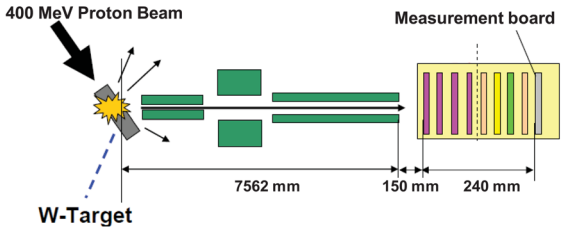

Fig. 11 Experiment diagram of neutron accelerated test.

Fig. 12 Photograph of neutron accelerated test.

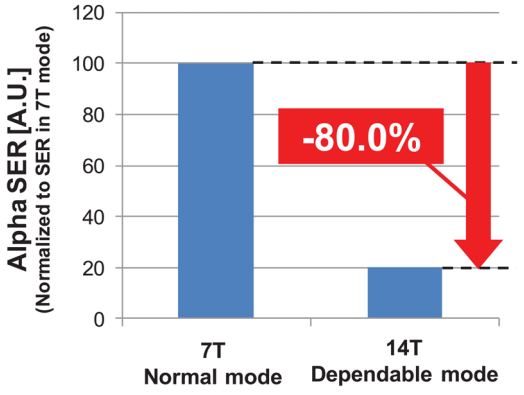

Fig. 13 Measured alpha-induced SERs in the 7T/14T SRAM.

has two sensitive nodes per cell. This is because Qcrit is increased in the 14T dependable mode. The average neutron SERs in the three samples are 131 FIT/Mb and 86 FIT/Mb in the 7T normal and 14T dependable modes, respectively (34.4% reduction). The standard deviation is decreased from 9.06 FIT/Mb to 5.87 FIT/Mb. The 14T dependable mode has a double area but achieves a less SER than to the 7T normal mode.

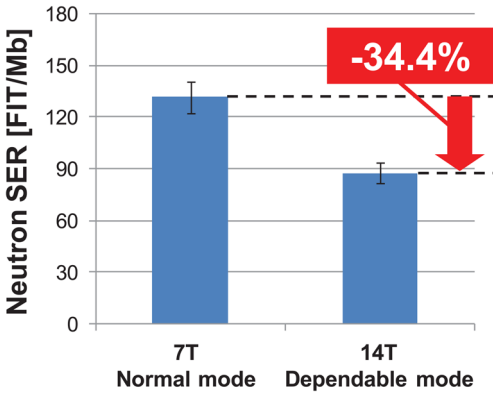

Fig. 14 Measured neutron-induced SERs in the 7T/14T SRAM.

5. Conclusion

We measured BERs and alpha-particle/neutron accelerated SERs using a 150-nm 576-Kb 7T/14T FD-SOI SRAM. We confirmed that the 14T dependable mode improves the minimum operating voltage to 0.52 V from 0.66 V in the 7T normal mode. The BER in the 14T dependable mode is superior to those in the TMR and ECC. The respective alpha- and neutron-induced SERs in the 14T dependable mode are 80.0% and 34.4% less than that in the 7T normal mode. We observed 10–70% increase of the 14T mode's Qcrit in a range of 0.3–1.5 V, by using Synopsys TCAD tool.

The proposed 7T cell has the intrinsic area overhead of 9.5% over the 6T cell. Users can, however, boost the BER and SER reliability if paying more area overhead (14T cell = 119%). This feature demonstrates that the proposed 7T/14T SRAM can dynamically change its BER and SER; the users can take a tradeoff between the reliability and area (cost), which is useful and effective to various applications.

Acknowledgments

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References

[1] International Technology Roadmap for Semiconductors (ITRS) Report. (http://www.itrs.net/Links/2010ITRS/Home2010.htm)
[2] A.V.-Y. Thean, Z.-H. Shi, L. Mathew, T. Stephens, H. Desjardin, C. Parker, T. White, M. Stoker, L. Prabhu, R. Garcia, B.-Y. Nguyen, S. Murphy, R. Rai, J. Conner, B.E. White, and S. Venkatesan, "Performance and variability comparisons between Multi-Gate FETs and planar SOI transistors," IEEE International Electron Devices Meeting (IEDM), pp.1–4, 2006.
[3] E.H. Cannon, D.D. Reinhardt, M.S. Gordon, and P.S. Makowenskyj, "SRAM SER in 90, 130 and 180 nm bulk and SOI technologies,"

IEEE International Reliability Phisics Symposium (IRPS), pp.300–304, 2004.
[4] D.F. Heidel, K.P. Rodbell, P. Oldiges, M.S. Gordon, H.H.K. Tang, E.H. Cannon, and C. Plettner, "Single-event-upset critical charge measurements and modeling of 65 nm latches and memory cells," IEEE Trans. Nucl. Sci., vol.53, pp.3512–3517, 2006.
[5] F. Wrobel, J.M. Palau, M.C. Calvet, O. Bersillon, and H. Duarte, "Incidence of multi-particle events on soft error rates caused by n-Si nuclear reactions," IEEE Trans. Nucl. Sci., vol.47, pp.2580–2585, 2000.
[6] J.R. Schwank, V. Ferlet-Cavrois, M.R. Shaneyfelt, and P.E. Dodd, "Radiation effects in SOI technologies," IEEE Trans. Nucl. Sci., vol.50, no.3, pp.522–538, 2003.
[7] R. Baumann, "The impact of technology scaling on Soft Error Rate performance and limits to the efficacy of error correction," IEEE International Electron Devices Meeting (IEDM), pp.329–332, 2002.
[8] C.H. Chen and A.K. Somani, "Fault-containment in cache memories for TMR redundant processor systems," IEEE Trans. Comput., vol.48, no.4, pp.386–397, 1999.
[9] L. Chang, D.M. Fried, J. Hergenrother, J.W. Sleight, R.H. Dennard, R.K. Montoye, L. Sekaric, S.J. McNab, A.W. Topol, C.D. Adams, K.W. Guarini, and W. Haensch, "Stable SRAM cell design for the 32 nm node and beyond," IEEE Symp. VLSI Technology, Dig. Tech. Papers, pp.128–129, 2005.
[10] I.J. Chang, J.J. Kim, S.P. Park, and K. Roy, "A 32 kb 10T subthreshold SRAM array with bit-interleaving and differential read scheme in 90 nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC), pp.398–399, 2008.
[11] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," IEEE Trans. Nucl. Sci., vol.43, no.6, pp.2874–2878, 1996.
[12] S.M. Jahinuzzaman, D.J. Rennie, and M. Sachdev, "A Soft error tolerant 10T SRAM bit-Cell with differential read capability," IEEE Trans. Nucl. Sci., vol.56, no.6, pp.3768–3773, 2009.
[13] H. Fujiwara, S. Okumura, Y. Iguchi, H. Noguchi, Y. Morita, H. Kawaguchi, and M. Yoshimoto, "Quality of a bit (QoB): A new concept in dependable SRAM," IEEE International Symposium on Quality Electronic Design (ISQED), pp.98–102, 2008.
[14] Y. Nakata, S. Okumura, H. Kawaguchi, and M. Yoshimoto, "0.5-V operation variation-Aware word-enhancing cache architecture using 7T/14T hybrid SRAM," ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), pp.219–224, 2010.
[15] G. Gasiot, D. Giot, and P. Roche, "Multiple Cell upsets as the key contribution to the total SER of 65 nm CMOS SRAMs and its dependence on well engineering," IEEE Trans. Nucl. Sci., vol.54, no.6, pp.2468–2473, 2007.
[16] H. Fujiwara, S. Okumura, Y. Iguchi, H. Noguchi, H. Kawaguchi, and M. Yoshimoto, "A dependable SRAM with 7T/14T memory cells," IEICE Trans. Electron., vol.E92-C, no.4, pp.423–432, April 2009.
[17] (2010) Synopsys Sentaurus TCAD tools. [Online], Available: http://www.synopsys.com/Tools/TCAD/DeviceSimulation/Pages/default.aspx
[18] P.E. Dodd and F.W. Sexton, "Critical charge concepts for CMOS SRAMs," IEEE Trans. Nucl. Sci., vol.42, no.6, pp.1764–1771, 1995.
[19] T. Suzuki, Y. Yamagami, I. Hatanaka, A. Shibayama, H. Akamatsu, and H. Yamauchi, "A sub-0.5-V operating embedded SRAM featuring a multi-bit-error-immune hidden-ECC scheme," IEEE Trans. J. Solid-State Circuit, vol.41, no.1, pp.152–160, 2006.
[20] JEDEC standard JESD89, "Measurement and reporting of alpha particles and terrestrial cosmic ray-induced soft errors in semiconductor devices."
[21] S. Yoshimoto, T. Amashita, S. Okumura, K. Yamaguchi, M. Yoshimoto, and H. Kawaguchi, "Bit error and soft error hardenable 7T/14T SRAM with 150-nm FD-SOI process," IEEE International Reliability Phisics Symposium (IRPS), pp.876–881, 2011.

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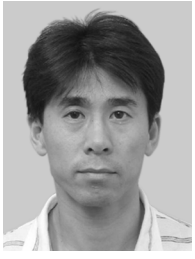

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