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PAPER

Multiple-Cell-Upset Tolerant 6T SRAM Using NMOS-Centered Cell Layout*

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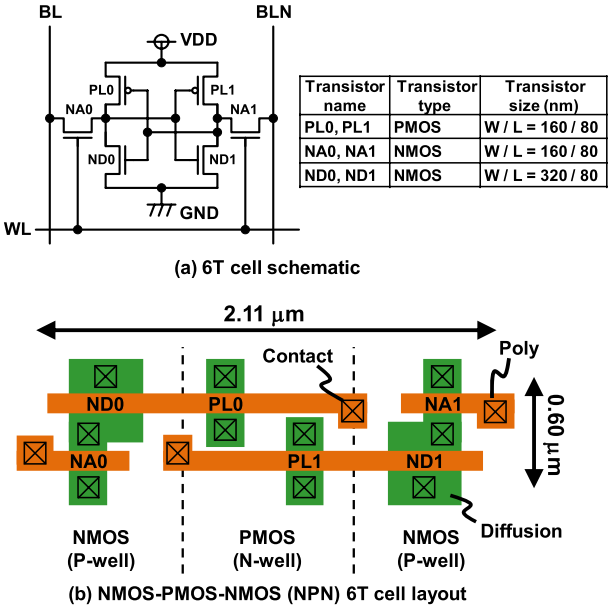
SUMMARY This paper presents a proposed NMOS-centered 6T SRAM cell layout that reduces a neutron-induced multiple-cell-upset (MCU) SER on a same wordline. We implemented an 1-Mb SRAM macro in a 65-nm CMOS process and irradiated neutrons as a neutron-accelerated test to evaluate the MCU SER. The proposed 6T SRAM macro improves the horizontal MCU SER by 67–98% compared with a general macro that has PMOS-centered 6T SRAM cells.

key words: *SRAM, soft error rate (SER), multiple cell upset (MCU), neutron particle, twin well, triple well*

1. Introduction

Nano-scaled integrated circuits are susceptible to particle-induced single event effect (SEE) because of their low signal charge and noise margin [1]–[3]. Particularly multiple cell upsets (MCUs), which are defined as simultaneous errors in more than one memory cell induced by a single event, have been closely investigated. The MCUs are caused by a collection of charges produced by secondary ions in neutron-induced nuclear reaction. The ratio of the MCUs to single-event upsets (SEUs) is predicted to increase drastically in nano-scaled SRAMs [4]–[6]. Process-scaling causes multiple MCU modes: charge sharing among memory storage nodes, bipolar effect in a P-well, and multi-coupled bipolar interaction (MCBI) [7]. In the literature, fail bits are spread over about a 1000×1000 bit area in 22-nm SRAM design; it is apparently impossible to correct multiple bit upsets (MBUs = MCUs in the same word) merely by error correction coding (ECC) [8].

Respective Figs. 1(a) and 1(b) show a schematic and a layout of a general 6T SRAM cell with a 65-nm CMOS logic rule. In the design, the sizes of the transistors are relaxed to suppress threshold voltage variation so that the cell area is about twice as large as a commercial 65-nm 6T cell [9]. The 6T cell consists of PMOS load transistors (PL0, PL1), NMOS driver transistors (ND0, ND1) and access transistors (NA0, NA1). A wordline (WL) and two bitlines (BL, BLN) are horizontally and vertically connected among cells, respectively. In the layout of the general 6T cell, the PMOS transistors are centered in the memory cell; this structure is called an NMOS-PMOS-NMOS (NPN) layout in this paper.



Transistor name	Transistor type	Transistor size (nm)
PL0, PL1	PMOS	W / L = 160 / 80
NA0, NA1	NMOS	W / L = 160 / 80
ND0, ND1	NMOS	W / L = 320 / 80

Fig. 1 (a) Schematic and (b) NMOS-PMOS-NMOS (NPN) layout of a general 6T SRAM cell.

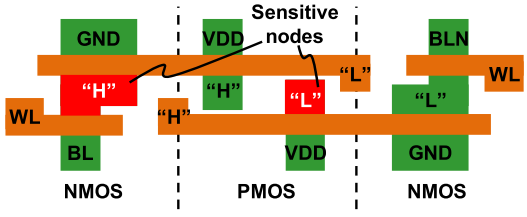


Fig. 2 Sensitive nodes in a general NPN 6T SRAM cell.

Figure 2 shows sensitive nodes in the general 6T cell layout: a low-state ("L") PMOS diffusion and a high-state ("H") NMOS diffusion. We have observed that the NMOS has a four-times larger SEU cross section than a PMOS for a wide range of supply voltages (see Fig. 3) [10], [11]. The simulation results come from an iRoC TFIT soft-error simulator using database of a generic 65-nm bulk CMOS process [11]. Figure 4 shows an SRAM cell array using the general NPN 6T layout. In the conventional 6T SRAM, the sen-

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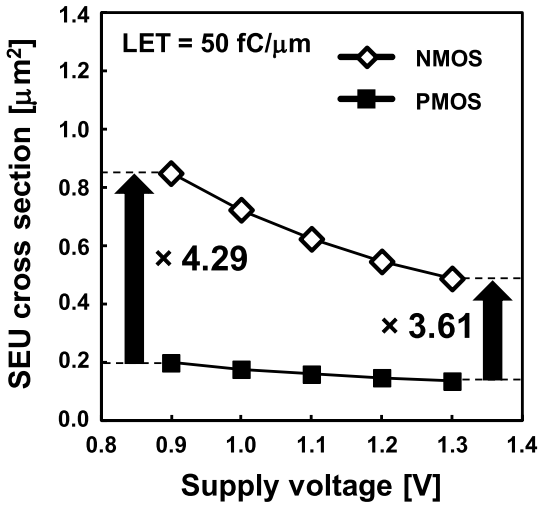

Fig. 3 SEU cross sections of NMOS and PMOS with a twin-well 65-nm process calculated using the iRoC TFIT simulator [10], [11].

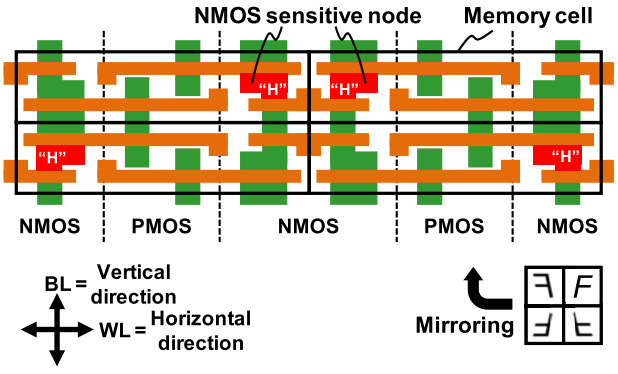

Fig. 4 SRAM cell array using the general NPN 6T cell layout.

sitive NMOS nodes are in a same P-well in the horizontal direction; horizontal upsets can be easily incurred.

In this paper, we present horizontal MCU improvement of a PMOS-NMOS-PMOS (PNP) 6T layout with 65-nm SRAM test chips. The SRAMs are designed in both of twin-well and triple-well structures because well engineering drastically affects the MCU SER [12], [13]. We will show experimental results at the Research Center for Nuclear Physics (RCNP), Osaka University; the proposed layout improves the horizontal MCU SER by 67–98% in the both of the twin- and triple-well structures. The proposed layout enhances effectiveness of single error correcting — double error detecting ECC (SEC-DED ECC).

2. Proposed NMOS-Centered 6T SRAM Cell and Macro Design

2.1 NMOS-Centered 6T SRAM Cell Layout

The proposed 6T cell is designed as a PMOS-NMOS-PMOS (PNP) layout in Fig. 5. The NMOS-centered 6T layout has the same transistors as the general one. The WL and the BLs are respectively assigned in horizontal and vertical direction.

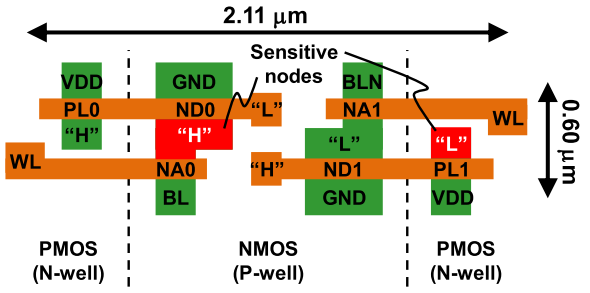

Fig. 5 Layout of a proposed PMOS-NMOS-PMOS (PNP) 6T cell.

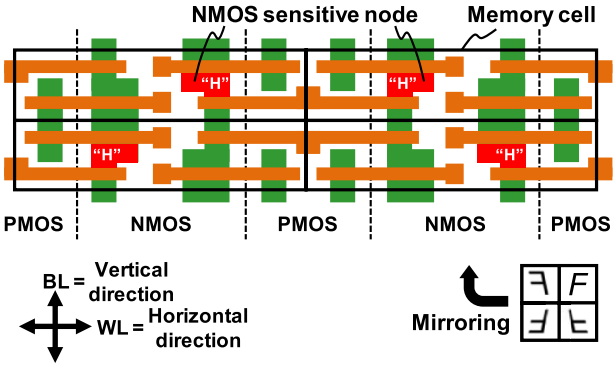

Fig. 6 SRAM cell arrays using the proposed PNP 6T cell layout.

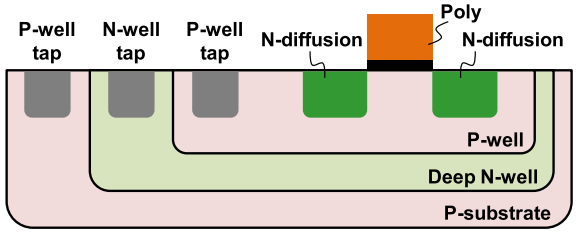

Fig. 7 Cross section of NMOS when using triple well.

The PNP 6T cell can lower a horizontal MCU rate because the NMOS-centered layout can separate the horizontally adjacent NMOS sensitive nodes with the N-well as shown in Fig. 6. The proposed layout has the same schematics and the cell area on the 65-nm logic rule basis, so that the proposed design can be implemented only by replacing its cell layout. Note that shared contacts, which are commonly used in an industrial SRAM rule, cannot be applied to the proposed 6T cell layout. This drawback incurs a certain area overhead in the SRAM rule basis design.

2.2 SRAM Macro Design

We designed and fabricated an 1-Mb SRAM test chip consisting of 256-Kb macros of four types (NPN layout with twin well, PNP layout with twin well, NPN layout with triple well (Fig. 7), and PNP layout with triple well), as presented in Fig. 8(a). Additionally, Fig. 8(b) illustrates the block diagram of a 16-Kb block (128 columns × 128 rows: 16 bits/word × 1 K words). The 16 bits in a same word are

aligned in a bit-interleaving manner. The SRAM macros using the four-type 6T cells occupy same areas so that the SRAM macros share same peripheral circuits. In the two macros with the triple-well structures, the memory cells are merely fabricated in the triple well; the peripheral circuits are on the twin well. In the memory cells on the triple-well structure, the deep N-well narrows the depth of the P-well; thereby the parasitic bipolar effect increases the MCU SER. This paper also investigates the dependency on the well structuring.

Figure 9 presents a layout of the implemented SRAM cell arrays and well taps. The NPN and PNP 6T cells designed by the 65-nm logic rule have $2.11 \times 0.60\,\mu m^2$ area (see Figs. 1(b) and 5; the gate length is relaxed to 80 nm to suppress variation). The well taps are inserted every 32 cells (= 19.2 μm) in the vertical direction; hence, a tap density is 1/32 of memory cells. Since the memory cell assigns the Metal-1 layer as internal connections, the vertical Metal-2 and horizontal Metal-3 layers are assigned as BLs and WLs.

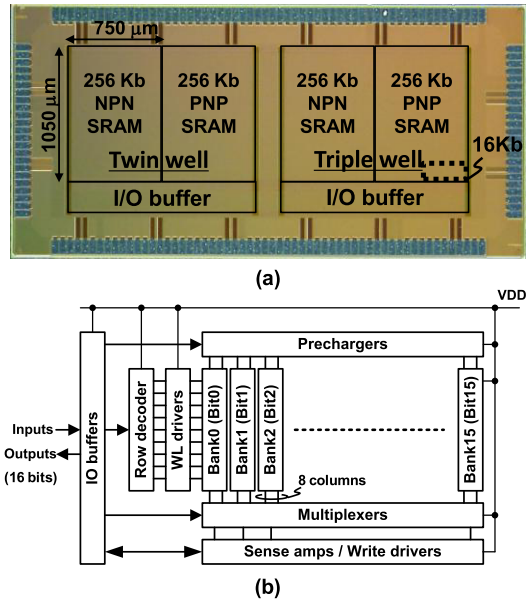

Fig. 8 (a) Micrograph of a 1-Mb SRAM test chip including NPN and PNP SRAMs with twin and triple wells. (b) Block diagram of a 16-Kb block.

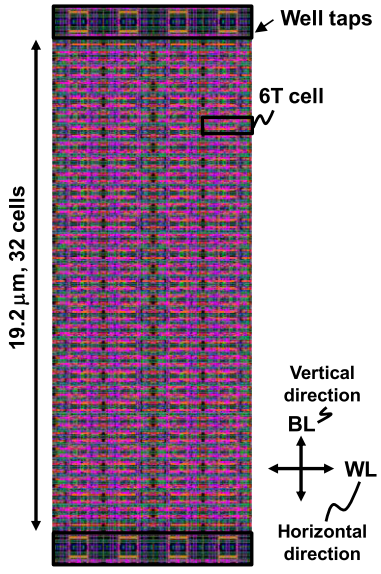

Fig. 9 Layout of memory cell array and well taps.

3. Experimental Results

Figure 10 presents an experimental setup for a neutron-accelerated test. The neutron irradiation experiment is conducted at The Research Center for Nuclear Physics (RCNP), Osaka University. Spallation neutron beam generated by the 400-MeV proton beam irradiates a board under test (BUT) 7892-mm far from a tungsten target, on which three sample chips are placed in a BUT, for 30 hrs. The neutron flux is normalized to 13 cph /cm^2 above 10 MeV at ground level in New York City [14], which incorporates scattering effect [15], attenuation effect [16], and board screening effect [17]. Figure 11 shows a timeline on the BUT. The FPGA automatically generates input data pattern to the SRAM macro before the irradiation and finally outputs addresses of the fail bits. The FPGA is placed apart from an irradiation area (10 cm diameter) so that the FPGA properly works even in this irradiation test.

Figures 12(a) and 12(b) illustrate measurement results of single-bit-upset (SBU) SERs when a checkerboard (CKB) pattern and all-zero (ALL0) pattern are used. The supply voltage is applied to the four macros from 0.6 V to

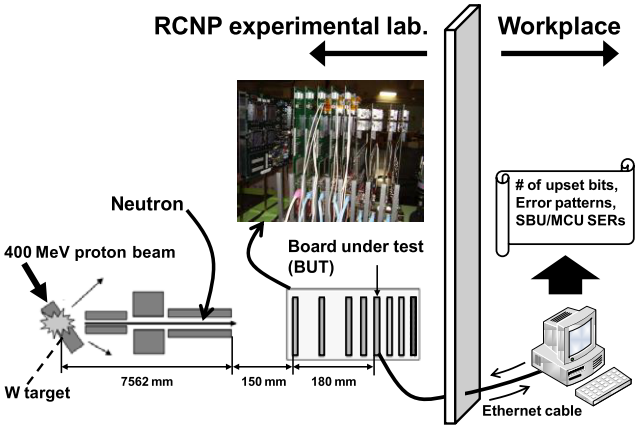

Fig. 10 Setup for neutron-accelerated test.

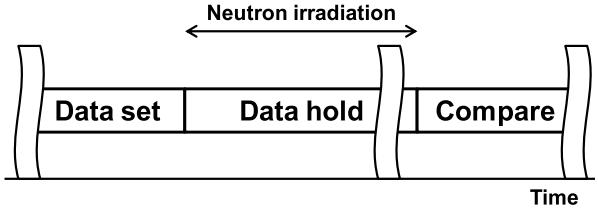

Fig. 11 Timeline in the neutron-accelerated test.

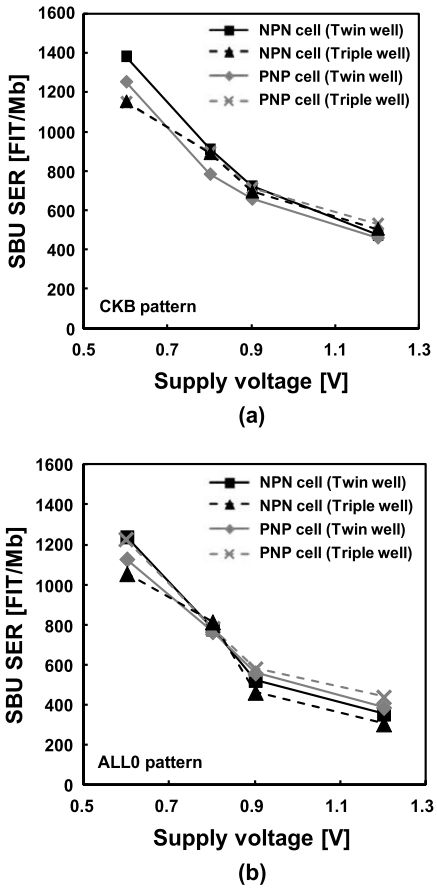

Fig. 12 Measured neutron-induced SBU SERs in the (a) CKB pattern and (b) ALL0 pattern at 0.6-1.2 V (four types).

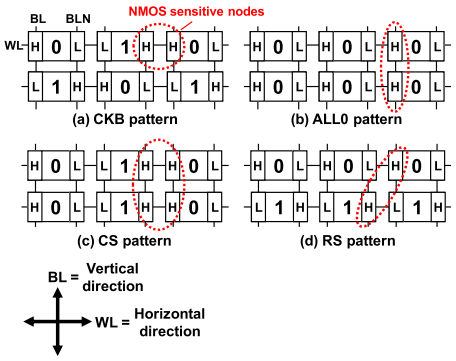

Fig. 13 Data patterns: (a) checker-board (CKB), (b) all zero (ALL0), (c) column stripe (CS), and (d) row stripe (RS).

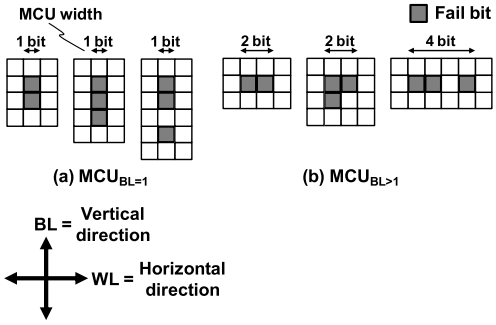

Fig. 14 Multiple-cell-upset patterns: (a) $MCU_{BL=1}$ and (b) $MCU_{BL>1}$ are defined respectively by vertical fail bits in a same column and by horizontal fail bits in two or more columns.

1.2 V to assess the dependence of the SERs on the supply voltage. Results show that the SBU SERs were ranging from 500 FIT/Mb to 1400 FIT/Mb depending on the supply voltage, but no apparent difference on the SBU SER is observed among the four types. The SBU SER of the CKB pattern is slightly larger than that of the ALL0 pattern. Figures 13(a) and 13(b) show NMOS sensitive nodes in the CKB and ALL0 patterns; they are aligned in the horizontal and vertical directions, respectively. The distance between the sensitive nodes in the CKB pattern is, however, longer than that in the ALL0 pattern (see Fig. 6); this feature possibly yields a more SBU SER in the CKB pattern even if a large-energy ion hits the sensitive nodes. On the other hand, MBUs tend to be incurred in the ALL0 patterns at the same ion energy.

In addition to the SBU SER, we measured MCU SER using four data patterns presented in Fig. 13: (a) CKB, (b) ALL0, (c) column stripe (CS), and (d) row stripe (RS), in which sensitive node patterns differ.

As presented in Fig. 14, an MCU SER in the vertical direction is called $MCU_{BL=1}$ in this paper, and an MCU SER in the horizontal direction is called $MCU_{BL>1}$. The $MCU_{BL>1}$ is more important for designers to adopt the interleaving and/or ECC strategy.

Figures 15(a)–(d) illustrate measured MCU SER in the four data patterns at the supply voltage of 1.2 V. When using the CKB, CS, and RS patterns, the $MCU_{BL>1}$ in the PNP 6T SRAM can be suppressed by 86–98% compared to the general NPN layout. The proposed PNP layout separates NMOSes from adjacent ones in the horizontal direction, which reduces the $MCU_{BL>1}$ SER. In the ALL0 pattern, the $MCU_{BL>1}$ even in the general NPN cells is low in nature because the sensitive nodes are not horizontally adjacent in a single bitline. As a result, only 67% improvement is observed in the MCU SER. The proposed PNP layout with the twin-well structure achieves $MCU_{BL>1}$ SERs of 5.78, 4.58, 9.48, and 4.70 FIT/Mb in the CKB, ALL0, CS and RS patterns and the PNP layout with the triple-well structure achieves $MCU_{BL>1}$ SERs of 5.78, 4.58, 18.96 and 3.13 FIT/Mb. Table 1 summarizes the data of the MCU SERs.

4. Conclusion

Reducing the horizontal $MCU_{BL>1}$ SER is more crucial than the vertical one, which can be suppressed by SEC-DEC ECC. This paper presented a proposed PNP (NMOS-centered) 6T SRAM that makes a neutron-induced $MCU_{BL>1}$ SER lower than the general NPN 6T SRAM in the horizontal direction. We designed a 65-nm 1-Mb SRAM test chips including the NPN and PNP SRAM macros. The

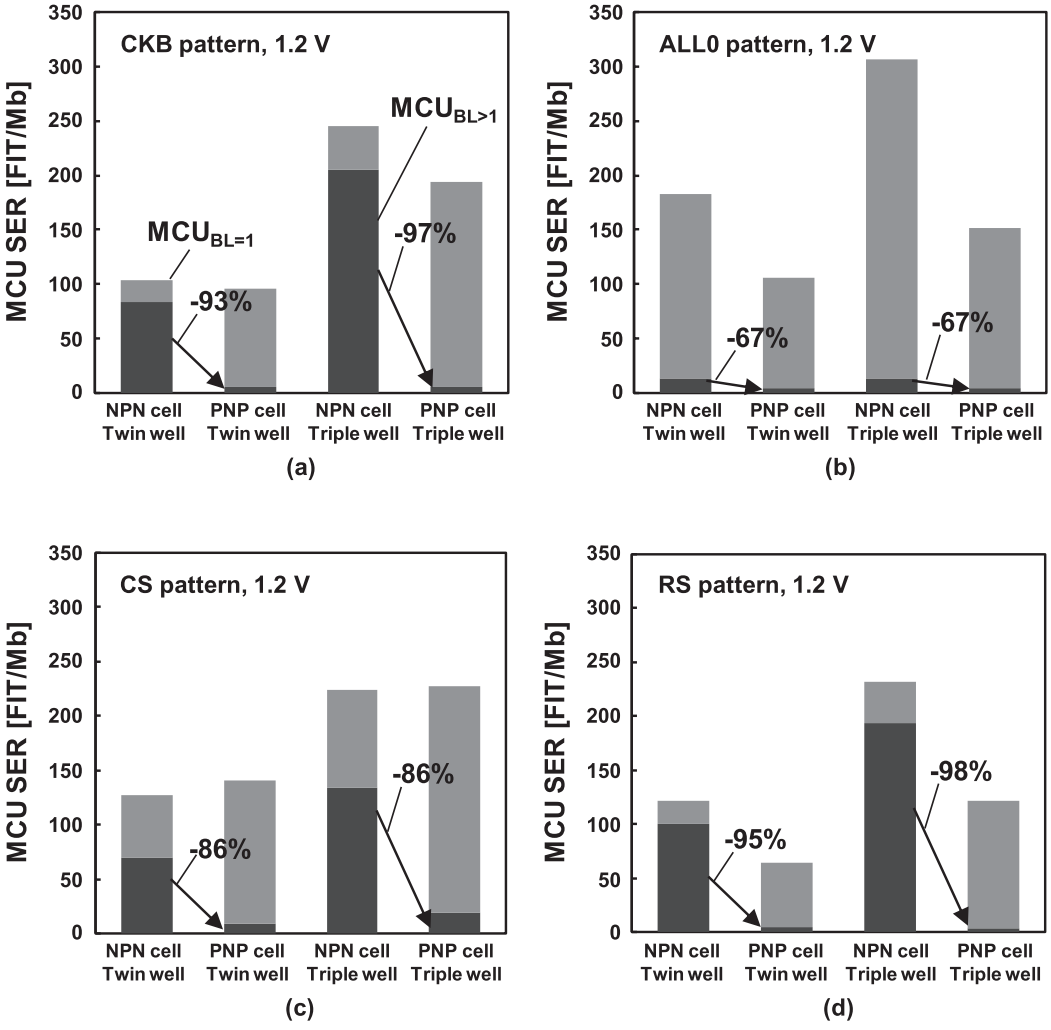

Fig. 15 Data patterns: (a) checker-board (CKB), (b) all zero (ALL0), (c) column stripe (CS), and (d) row stripe (RS).

Table 1 Summary of the neutron-induced MCU SERs.

VDD [V]	Data pattern	Well type	Cell type	$MCU_{BL=1}$ SER [FIT/Mb]	$MCU_{BL>1}$ SER [FIT/Mb]	Total MCU SER [FIT/Mb]
1.2	CKB	Twin	NPN	20.23	83.83	104.06
			PNP	89.61	5.78	95.39
		Triple	NPN	40.47	205.23	245.70
			PNP	187.89	5.78	193.67
	ALL0	Twin	NPN	169.51	13.74	183.25
			PNP	100.79	4.58	105.37
		Triple	NPN	293.21	13.74	306.95
			PNP	146.60	4.58	151.19
	CS	Twin	NPN	56.89	69.93	126.82
			PNP	131.56	9.48	141.04
		Triple	NPN	90.08	133.93	224.01
			PNP	208.60	18.96	227.57
	RS	Twin	NPN	21.91	100.18	122.09
			PNP	59.48	4.70	64.18
		Triple	NPN	37.57	194.10	231.66
			PNP	118.96	3.13	122.09

measurement results demonstrate that the PNP layout suppresses the horizontal $MCU_{BL>1}$ SER by 67–98% in the CKB, ALL0, CS and RS patterns with the twin-well and triple-well structure in which the tap density is 1/32 of memory cells.

Acknowledgments

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