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A 40-nm Resilient Cache Memory for Dynamic Variation Tolerance Delivering ×91 Failure Rate Improvement under 35% Supply Voltage Fluctuation

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SUMMARY This paper presents a resilient cache memory for dynamic variation tolerance in a 40-nm CMOS. The cache can perform sustained operations under a large-amplitude voltage droop. To realize sustained operation, the resilient cache exploits 7T/14T bit-enhancing SRAM and on-chip voltage/temperature monitoring circuit. 7T/14T bit-enhancing SRAM can reconfigure itself dynamically to a reliable bit-enhancing mode. The on-chip voltage/temperature monitoring circuit can sense a precise supply voltage level of a power rail of the cache. The proposed cache can dynamically change its operation mode using the voltage/temperature monitoring result and can operate reliably under a large-amplitude voltage droop. Experimental result shows that it does not fail with 25% and 30% droop of V_{dd} and it provides 91 times better failure rate with a 35% droop of V_{dd} compared with the conventional design.

key words: *design for robustness, cache, variation tolerance, 7T/14T SRAM*

1. Introduction

Technology scaling increases the threshold-voltage (V_{th}) variation of MOS transistors mainly because of random dopant fluctuation, NBTI and RTN. The minimum operating voltage (V_{min}) of SRAM cell increases as the V_{th} variation increases with technology scaling, which degrades operating margin of a processor. A processor with a shrinking operating margin is more susceptible to power supply noise, IR drops, and temperature fluctuations. Especially, electric control units in electric vehicles suffer large temperature fluctuation and large voltage fluctuation/droop caused by motor noise, EMIs, voltage surges, and sudden interruptions in wiring harness connections. A sudden interruption, for example, can cause disconnection of the ECU to the power supply for several milliseconds. Power supply circuits implemented in the ECU have large capacitors to improve tolerance against sudden interruptions. If the capacitance is hundreds of microfarads, then the voltage droops caused by the sudden interruptions are reduced to less than 20% droop, with droop duration in the milliseconds. But the use of a large capacitor for the ECU should be avoided for reason of reliability, cost, and size. Consequently, voltage-variation (the voltage droops of 20% V_{dd}) and temperature-variation tolerant processors are needed for ECUs in electric vehicles.

Earlier designs [1]–[3] have addressed timing errors caused by a high-frequency (ca. 100 MHz) voltage droop. A tunable replica scheme [4] can reduce V_{min} of SRAM by 9% under 13% voltage droop. However, they cannot mitigate embedded SRAM margin failures caused by large amplitude (ca. 20% of V_{dd}) voltage droops. An SRAM block in a processor with high integration and minimum-size transistors determine the V_{min} of the entire processor. For dynamic variation tolerant processors, a fault-tolerance cache is necessary.

A common fault-tolerant cache architecture uses redundant columns/rows [5]. The architecture requires many redundant columns/rows to accommodate the large number of faults. The columns/rows are inefficient in low failure rate situations. The PADed cache proposed in [6] uses a programmable decoder to remap faulty cache lines to non-faulty ones. As another solution, the error correction code (ECC) has been applied to caches [7]–[9]. Two-dimensional ECC proposed in [8] combines vertical and horizontal error coding. In [9], 1-bit ECC is applied to cache blocks uniformly. Blocks containing two or more defective cells are protected selectively with multi-bit ECC. The Multi-bit ECC check bits and the block locations are stored in a small dedicated cache. These techniques are not effective for large amplitude voltage droops that cause many faults.

Herein, we present a resilient cache memory that can perform sustained operations under a large-amplitude voltage droop. To realize sustainable operation, the resilient cache exploits 7T/14T bit-enhancing SRAM, which has a more reliable operation mode and on-chip voltage monitoring circuit.

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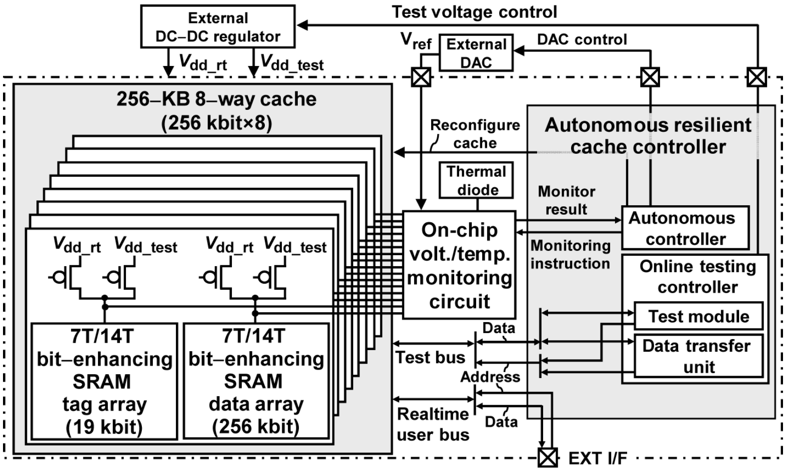


Fig. 1 Block diagram of the resilient cache.

2. Proposed Resilient Cache

The resilient cache (Fig. 1) is a 256 KB 8-way cache memory array with 7T/14T bit-enhancing (BE) SRAM bitcell structure [10], voltage and temperature monitoring circuits [11], and an autonomous resilient cache controller. Each memory block can be switched individually its power supply to the power supply for runtime operation ($V_{\mathrm{dd\_rt}}$) or the power supply for testing ($V_{\mathrm{dd\_test}}$). The power supply of the monitoring circuits and the power supply of the controller are separated from the power supply of the memory blocks. The local power rails of the memory blocks are monitored by voltage monitoring circuits, which can obtain a precise supply voltage level at a testing time and monitor a voltage fluctuation during runtime. Furthermore, a temperature monitoring circuit can sense the on-chip temperature. The temperature information recorded at a testing time is used in a temperature correction of the V_{min}. The autonomous resilient cache controller comprises an autonomous controller and an online testing controller with a test module and data transfer unit. The online testing controller can execute memory testing that is completely transparent to user accesses. The controller obtains an operating margin and V_{min} of the memory block. The autonomous controller controls a probing point of the voltage monitor and reference voltage (V_{ref}) using the external DAC. It receives results from the monitoring circuits. The results are used for voltage droop detection and block-basis voltage droop control, as described reminder of the paper.

2.1 7T/14T bit-Enhancing SRAM Bitcell

Each SRAM cell in the proposed resilient cache comprises 7T/14T BE SRAM cell structure [10]. The 7T/14T BE SRAM cell has a pair of conventional 6T SRAM bitcells. The internal nodes of the pair are connected directly by two additional PMOS transistors as presented in Fig. 2. This structure of 7T/14T BE SRAM provides an additional operation mode designated as the enhancing mode along with the normal mode. The two modes of 7T/14T BE SRAM are presented in Table 1. Figure 3 shows bit error rates in 7T/14T BE SRAM and in the other scheme. In enhancing mode, the added transistors are activated and BE SRAM features reliable operations especially at low voltages by combining two bitcells.

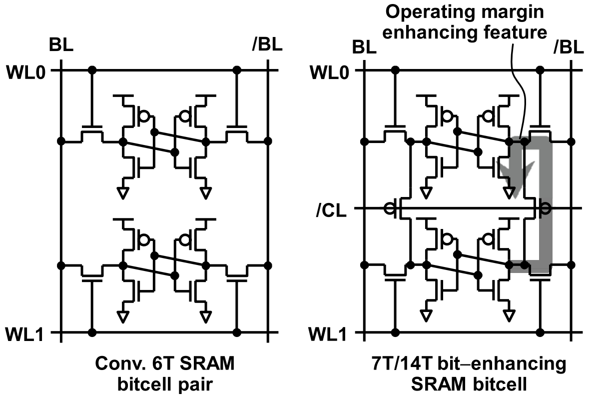


Fig. 2 Schematics showing a conventional 6T SRAM bitcell pair and 7T/14T SRAM bitcell.

Table 1 Two operation modes of 7T/14T bit-enhancing bitcell.

	# of memory cells comprising 1 bit	# of WL drives	CL
Normal	1 (7T/bit)	1	Off (“H”)
Enhancing (read)	2 (14T/bit)	1	On (“L”)
Enhancing (write)	2 (14T/bit)	2	On (“L”)

2.2 On-Chip Monitoring Circuits

On-chip monitoring circuits, presented in Fig. 4, comprise a source follower (SF) and a latch comparator (LC) [11]. Supply voltage monitoring circuits measure the supply voltage fluctuation on power rails of each SRAM array. Temperature monitoring circuits sense thermal diodes placed near the center of the cache macro.

Voltages on the probing point and thermal diode are level-shifted by the SFs. The level-shifted voltage (V_{sfo}) is compared with the reference voltage (V_{ref}) by the LC in synchronization with a sampling clock. The LC outputs “1” or “0” corresponding to the comparison result.

The on-chip monitoring circuits are area efficient and sense accurate voltage level of the SRAM array, in addition to the cache temperature. Therefore, they are suitable for use in online built-in self-tests (BISTs) and voltage droop detection.

2.3 Block Basis Online Testing

Figure 5 shows the block basis online testing scheme for the proposed resilient cache. The online test controller conducts memory testing on each memory block in order of the physical block address. The supply voltage of the testing block is decreasing gradually during the testing time. The controller records the testing voltage and temperature from the on-chip monitoring circuits with respect to each operation mode of BE SRAM at which the first failure is detected. The resilient cache still has cache lines to which data can be allocated even if memory testing is working because it is block-basis testing. The memory blocks, except the current memory under test (MUT) block, are still accessible. Thereby they can operate as runtime (RT) blocks.

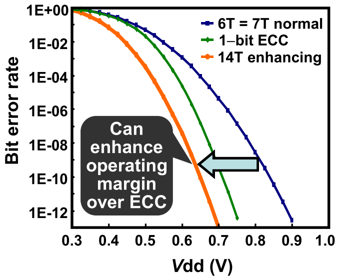


Fig. 3 Bit error rates (BERs): “6T”, “1-bit ECC” and “7T normal” and “14T enhancing” using 7T/14T Bit-enhancing SRAM.

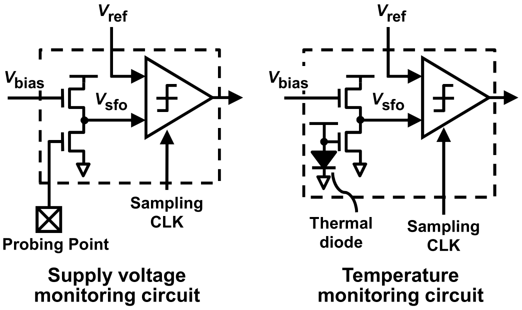


Fig. 4 Supply voltage/temperature monitoring circuit.

The testing controller uses the test bus separated from the user bus. The proposed testing scheme is transparent to the processor operation. Although one cache way cannot be used during the testing, the IPC performance degradation in the SPEC 2006 [12] benchmarks is less than 1%. The test is conducted periodically. The testing cycle can be regulated outside the cache (e.g. a cycle responding to a control period of the software). The IPC degradation is 1% at most, although it depends on the testing cycle.

The flowchart in Fig. 6 depicts the online testing flow. At the beginning of memory testing on each block, the data transfer unit transfers data from the MUT block to the previous MUT block. The MUT block power supply is switched to testing voltage ($V_{\mathrm{dd\_test}}$). After switching, a testing is executed to evaluate whether the failure is detected or not. If not detected, then $V_{\mathrm{dd\_test}}$ is decreased by one step and the testing is executed again. If detected, then the voltage at that time is recorded with temperature. Having completed the testing on one block, the online test controller sets $V_{\mathrm{dd\_test}}$ to a nominal V_{dd} and changes next block into MUT. This flow continues until all blocks have been tested.

Operation of the data transfer unit is depicted in Fig. 7. First, physical block 0 is tested. Physical blocks of 1–7 operate as runtime blocks. Next, the data transfer unit transfer data from physical block 1 (next MUT block) to physical block 0 (previous MUT block). After the transfer, physical block 1 is tested. Physical block 0 and physical blocks 2–7 operate as runtime blocks. In this way, the MUT block moves among 8 blocks without losing the memory contents.

An example of test results is presented in Fig. 8. The online testing controller has a test result table to record V_{min} corresponding to temperature. The recorded testing volt-

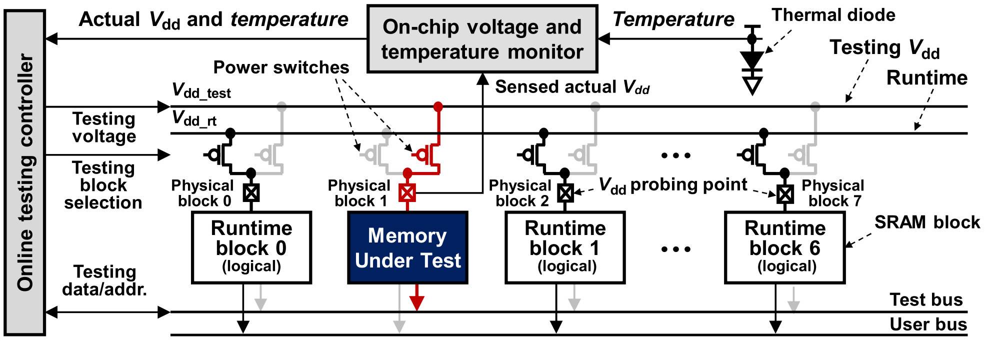


Fig. 5 Online testing architecture.

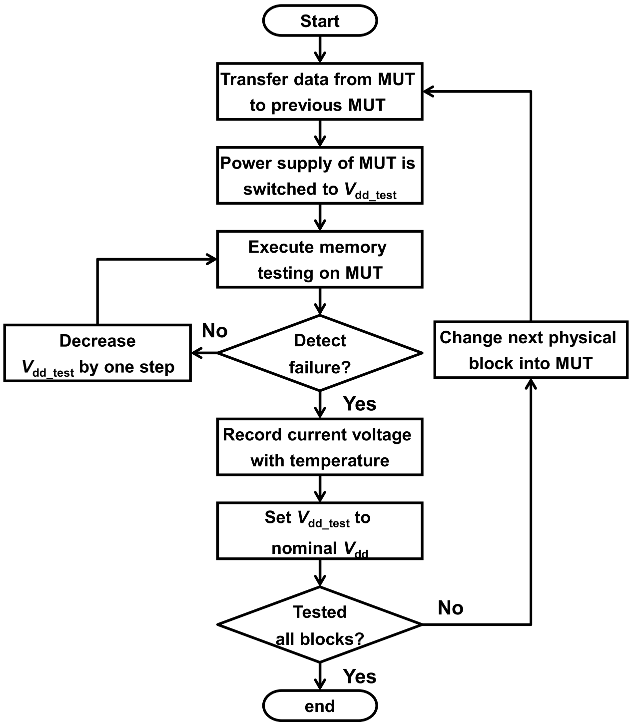


Fig. 6 Flowchart of the online testing.

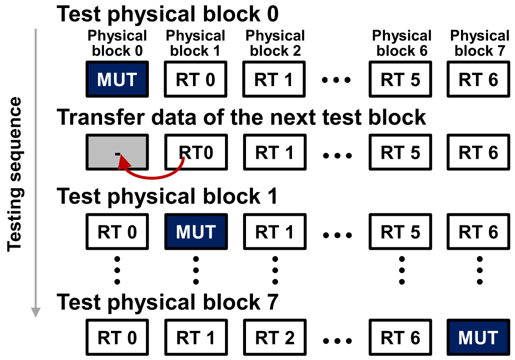
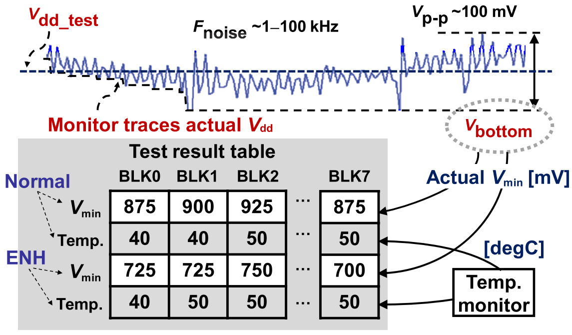


Fig. 7 Block basis online testing scheme.



		BLK0	BLK1	BLK2	…	BLK7
Normal	V_{min}	875	900	925	…	875
	Temp.	40	40	50	…	50
ENH	V_{min}	725	725	750	…	700
	Temp.	40	50	50	…	50

Fig. 8 Block basis actual V_{min} and temperature recording.

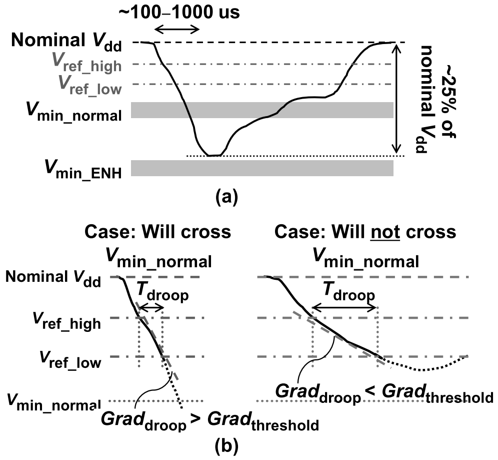
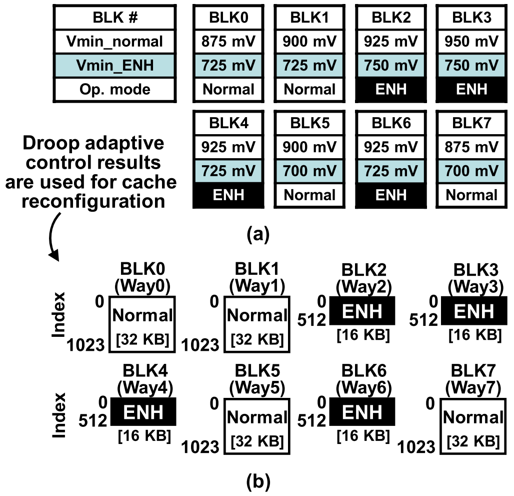


Fig. 9 (a) Example of voltage waveform. (b) Voltage droop detection scheme.



BLK #	BLK0	BLK1	BLK2	BLK3
Vmin_normal	875 mV	900 mV	925 mV	950 mV
Vmin_ENH	725 mV	725 mV	750 mV	750 mV
Op. mode	Normal	Normal	ENH	ENH

BLK #	BLK4	BLK5	BLK6	BLK7
Vmin_normal	925 mV	900 mV	925 mV	875 mV
Vmin_ENH	725 mV	700 mV	725 mV	700 mV
Op. mode	ENH	Normal	ENH	Normal

Fig. 10 (a) Block basis voltage droop control. (b) Cache configuration during voltage droop.

age is actual V_{min} of the memory array because the on-chip voltage monitor probes the local power rail of the memory blocks. The voltage monitor traces the bottom level of the testing voltage (V_{bottom}) during the testing time to record an actual V_{min}. The test result table is used as a reference for the voltage-temperature variation adaptive control described later.

2.4 Voltage and Temperature Variation Adaptive Control

Figures 9, 10, and 11 present a voltage-temperature variation adaptive control scheme. The autonomous controller detects degradation of the operating margin caused by the voltage and temperature fluctuation. If the margin is insufficient for stable operation, the controller changes the operation mode of 7T/14T bit-enhancing SRAM to the 14T enhancing mode. This adaptive control enables maintenance of the required voltage margin in the current operating condition.

To detect the voltage droop, reference voltages "high" (V_{ref_high}) and "low" (V_{ref_low}) are set to the proper level, as shown in Fig. 9. V_{dd} is monitored by the monitoring circuit

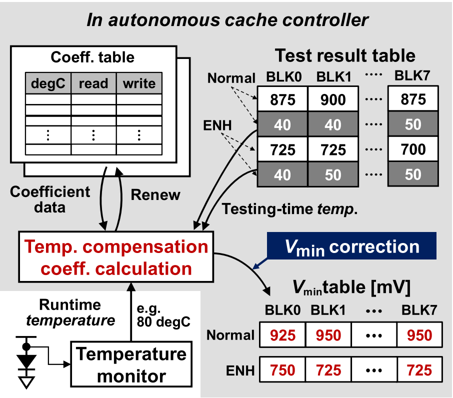


Fig. 11 V_{min} correction responding to temperature variation.

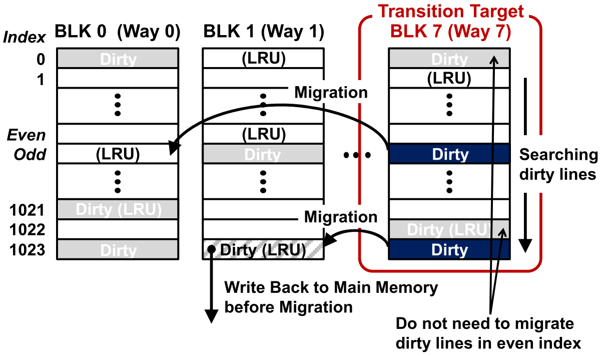


Fig. 12 Migration process for dirty cache lines in the mode transition target way.

using $V_{\mathrm{ref\_high}}$ and $V_{\mathrm{ref\_low}}$. When V_{dd} falls below $V_{\mathrm{ref\_high}}$, a timer starts to count. Then, as V_{dd} falls below $V_{\mathrm{ref\_low}}$, the timer stops to count and a gradient of the voltage droop is calculated. The autonomous controller estimates whether the V_{dd} drops below $V_{\mathrm{min\_normal}}$ or not using the gradient. If the gradient is greater than the threshold value, the controller estimates that the V_{dd} crosses $V_{\mathrm{min\_normal}}$. If not, the controller estimates that the V_{dd} does not cross $V_{\mathrm{min\_normal}}$ (shown in Fig. 9(b)). The resilient cache changes the operation mode to the 14T enhancing mode at the voltage below $V_{\mathrm{min\_normal}}$. The controller may miss detecting very steep droops and very slow droops. The very steep droops are caused by high frequency noises. SRAM cell is less susceptible for the high frequency noises [14]. The reconfiguration of the cache is accomplished even in case that the voltage droop is very slow because the autonomous controller changes operation mode to 14T enhancing mode when the supply voltage falls below specified level.

This voltage variation adaptive control scheme is performed in a block-basis manner. Only blocks for which the V_{dd} drops below its $V_{\mathrm{min\_normal}}$ change the operation mode to the 14T enhancing mode as presented in Fig. 10. The other blocks keep the operation mode as the 7T normal mode. Dirty lines in the proposed cache can be written back to main memory even if the V_{dd} drops by 35% in 100 μs.

To reconfigure the blocks, the tag array of the resilient cache must be modified. One bit is added to the tag bits in each cache line. The comparators for the tag comparison must be extended for the additional bit. The additional bit holds MSB of the index and is compared as the LSB of tag bits. Moreover, the decoder must be designed so as not to choose the half index. The LSB of the decoder input is fixed to “0” in the bit-enhancing mode.

The V_{min} at runtime is corrected in response to the runtime temperature to compensate the temperature fluctuation (shown in Fig. 11). The autonomous controller obtains the current temperature using the on-chip temperature monitor and looks up V_{min} in the test result table. The V_{min} corresponding to the current temperature is calculated using these data. The coefficient data to compensate temperature difference between the testing time and current time are recorded in coefficient tables. The calculated V_{min} are collected in V_{min} tables. The V_{min} tables are used to determine the threshold of the gradient in the droop detection.

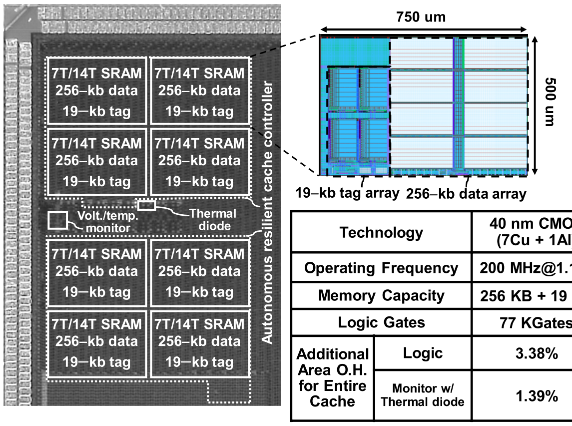
When the autonomous controller changes operation modes of the blocks into bit-enhancing mode, the dirty cache lines in the blocks must be migrated. The migration process is shown in Fig. 12. In this example, a target block of the mode transition is block 7. The controller searches dirty cache lines in the odd index of block 7. Dirty lines in the even index do not need to migrate because these lines are used after the mode transition. If the dirty cache line is detected, then the cache line migrates into the LRU cache line in the same set. If the LRU cache line is also dirty, then the LRU line is written back to main memory before the detected dirty line is migrated. If the detected dirty line is LRU line, then the line is written back to main memory.

If the V_{dd} is over $V_{\mathrm{ref\_high}}$ again, then the autonomous controller changes the operation mode of the blocks from bit-enhancing mode to normal mode. In such cases, it is unnecessary to migrate cache lines. The controller simply inactivates the control signal of the 7T/14T bit-enhancing SRAM (CL depicted in Fig. 2) and sets the cache state of the cache lines in the odd index to invalid.

3. Measurement Results

3.1 On-Chip Voltage Droop Waveform and V_{min} of Memory Blocks

Measurement results obtained using a test chip fabricated in 40-nm CMOS (Fig. 13) are presented in Figs. 14–16. The voltage monitoring circuit measures the on-chip voltage droop waveform (Fig. 14). An upper waveform in Fig. 14 is the injected waveform from outside the chip. This waveform is measured at off-chip probing point on the global power rail. A lower waveform is acquired by measurement with the on-chip monitoring circuit, which probes the local power rail of each memory block. The on-chip measurement waveform presents a different shape from that of the injected waveform because of parasitic elements of the chip. The result shows that the on-chip monitoring circuit is necessary to obtain a precise voltage level.



Technology		40 nm CMOS (7Cu + 1Al)
Operating Frequency		200 MHz@1.1 V
Memory Capacity		256 KB + 19 KB
Logic Gates		77 KGates
Additional Area O.H. for Entire Cache	Logic	3.38%
	Monitor w/ Thermal diode	1.39%

Fig. 13 Micrograph and features of test chips.

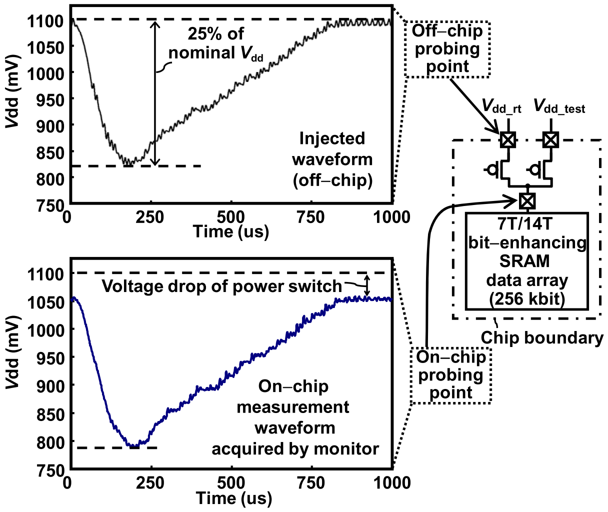


Fig. 14 Measured off-chip/on-chip voltage droop waveforms.

Measured V_{min} characteristics of the memory blocks are shown in Fig. 15. The V_{min}s are acquired for 8 blocks of 11 chips at each operation mode of BE SRAM. The temperature at the measurement is normal (25°C) and high (100°C). The averages of the V_{min} of the worst block (i.e. V_{min} of the entire cache) for 11 chips are 1015 mV in normal mode and 806 mV in bit-enhancing mode at 25°C. At 100°C, the average V_{min} in normal and bit-enhancing modes are 1050 mV and 827 mV respectively. Results show that changing the operation mode of BE SRAM to bit-enhancing mode improves the operating margin by 205 mV at 25°C and 223 mV at 100°C, on average.

3.2 Voltage Variation Tolerance

The voltage variation tolerance of the resilient cache is evaluated using a voltage droop injection to the external power supply rail. During voltage droop injection, the trace of cache access is input to the resilient cache. Then the accesses to fail bits are counted. Five cache traces were taken from SPEC2006 [12]. The evaluation shows that the resilient cache does not fail irrespective of the droop duration length when the voltage droop amplitude is 20%. Therefore, it is seen that the resilient cache can be applied to the ECUs in electronic vehicles.

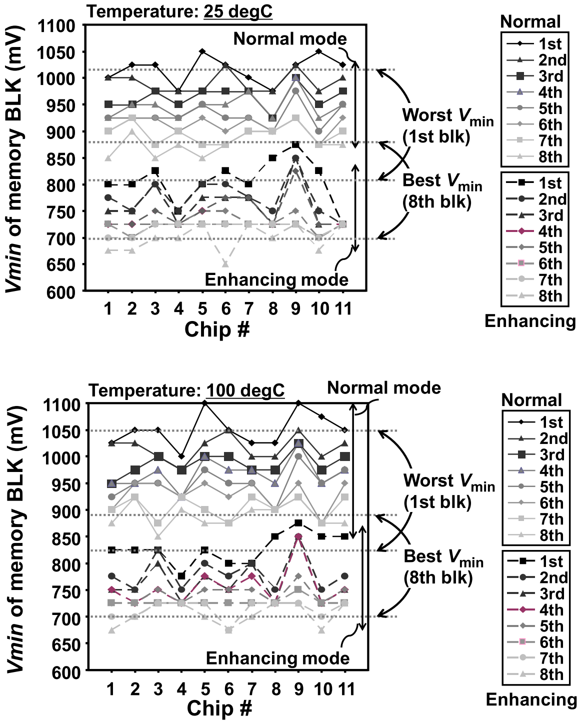


Fig. 15 V_{min}s of eight memory blocks of 11 chips (measured).

To investigate the voltage variation tolerance of the resilient cache, we conducted evaluations under voltage droop conditions with amplitude higher than 20%. The amplitudes are assumed to be 25%, 30%, and 35% of V_{dd} as shown in Fig. 16(a). The droop durations are 50 μs, 500 μs, 5 ms and 50 ms. Evaluation results under 25%, 30% and 35% droop condition are depicted respectively in Figs. 16(b)–16(d). Under 25% and 30% droop conditions, the failures increase linearly with droop duration length without the proposed scheme (no variation adaptive control and always normal mode). Using the proposed scheme (variation adaptive control and adopt switching to enhancing mode), the resilient cache does not fail irrespective of the droop duration length. Under a severe 35% droop condition, failures without the proposed scheme increased numerically to about ten times of those under a 25% droop condition. Using the proposed scheme, the failure rate improved by ×91 of that without the proposed scheme under 50 ms droop duration length.

3.3 Processor Performance

The cache reconfiguration affects processor performance. The cache capacity decreases by 16 KB when one block changes its operation mode into bit-enhancing mode. The capacity decrease degrades processor performance since cache misses occur more frequently. Figure 17 shows nor-

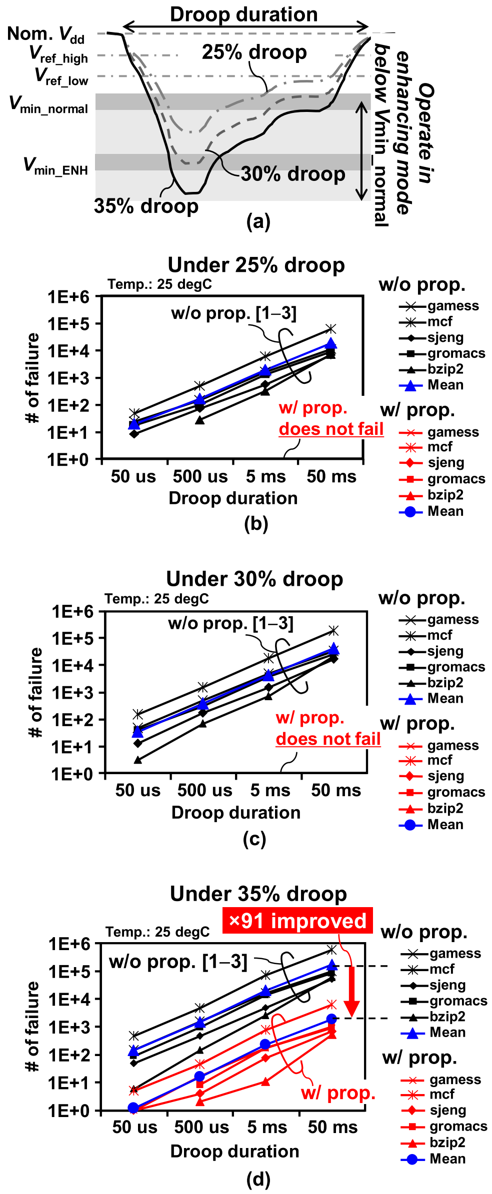


Fig. 16 Voltage droop tolerance and failure count evaluation: (a) droop waveform example, (b) 25% V_{dd} droop, (c) 30% V_{dd} droop, and (d) 35% V_{dd} droop.

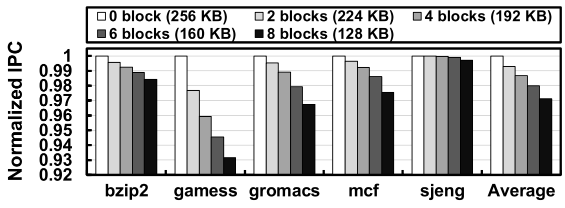


Fig. 17 Normalized IPCs with respect to the number of bit-enhancing mode blocks.

malized instruction per cycles (IPCs) with respect to the number of bit-enhancing mode blocks. The evaluation is conducted using gem5 simulator [13], with benchmarks selected from SPEC 2006 [12]. The average IPC loss is 2.88% when all blocks are bit-enhancing mode (128 KB cache capacity). The resilient cache operates in bit-enhancing mode only if the operating margin is insufficient, and continues stable operation though processor performance degrades.

4. Conclusion

As described in this report, we proposed a resilient cache with bit-enhancing memory and on-chip diagnosis structures in 40-nm CMOS. The resilient cache has a bit-enhancing memory that can dynamically change itself to enhancing mode and on-chip voltage/temperature monitoring circuit. It dynamically reconfigures its operation mode using the voltage/temperature monitoring result. It achieves a 91 times better failure rate under 35% droop of V_{dd} compared with that of the conventional design.

References

[1] K.A. Bowman, C. Tokunaga, J.W. Tschanz, A. Raychowdhury, M.M. Khellah, B.M. Geuskens, S.L. Lu, S. Member, P.A. Aseron, T. Karnik, and V. De, “All-digital circuit-level dynamic variation monitor for silicon debug and adaptive clock control,” IEEE Trans. Circuits Syst. I, vol.58, no.9, pp.2017–2025, Sept. 2011.

[2] K.A. Bowman, J.W. Tschanz, S.L. Lu, S. Member, P.A. Aseron, M.M. Khellah, A. Raychowdhury, B.M. Geuskens, C. Tokunaga, C.B. Wilkerson, T. Karnik, and V. De, “A 45 nm resilient microprocessor core for dynamic variation tolerance,” IEEE J. Solid-State Circuits, vol.46, no.1, pp.194–208, Jan. 2011.

[3] J. Tschanz, N.S. Kim, S. Dighe, J. Howard, G. Ruhl, S. Vangal, S. Narendra, Y. Hoskote, H. Wilson, C. Lam, M. Shuman, C. Tokunaga, D. Somasekhar, S. Tang, D. Finan, T. Karnik, N. Borkar, N. Kurd, and V. De, “Adaptive frequency and biasing techniques for tolerance to dynamic temperature-voltage variations and aging,” ISSCC Dig. of Tech. Papers, pp.292–293, Feb. 2007.

[4] A. Raychowdhury, B. Geuskens, K. Bowman, J. Tschanz, S.L. Lu, T. Karnik, M. Khellah, and V. De, “Tunable replica bits for dynamic variation tolerance in 8T SRAM arrays,” IEEE J. Solid-State Circuits, vol.46, no.4, pp.797–805, April 2011.

[5] J. Lee, Y.J. Lee, and Y.B. Kim, “SRAM Word-oriented redundancy methodology using built in self-repair,” Proc. IEEE Intl. System-on-Chip Conference (SOCC), pp.219–222, Sept. 2004.

[6] P.P. Shirvani and E.J. McCluskey, “PADed cache: A new fault-tolerance technique for cache memories,” Proc. VLSI Test Symp., pp.440–445, April 1999.

[7] J.L. Shin, B. Petrick, M. Singh, and A.S. Leon, “Design and implementation of an embedded 512-KB level-2 cache subsystem,” IEEE J. Solid-State Circuits, vol.40, no.9, pp.1815–1820, Sept. 2005.

[8] J. Kim, N. Hardavellas, K. Mai, B. Falsafi, and J. Hoe, “Multi-bit error tolerant caches using two-dimensional error coding,” Proc. IEEE/ACM Intl. Symp. on Microarchitecture (MICRO), pp.197–209, Dec. 2007.

[9] H. Sun, N. Zheng, and T. Zhang, “Leveraging access locality for the efficient use of multibit error-correcting codes in L2 cache,” IEEE Trans. Comput., vol.58, no.10, pp.1297–1306, Oct. 2009.

[10] H. Fujiwara, S. Okumura, Y. Iguchi, H. Noguchi, Y. Morita, H. Kawaguchi, and M. Yoshimoto, “Quality of a bit (QoB): A new concept in dependable SRAM,” Proc. IEEE Intl. Symp. on Quality Electronic Design (ISQED), pp.98–102, March 2008.

[11] K. Noguchi and M. Nagata, “An on-chip multichannel waveform monitor for diagnosis of systems-on-a-chip integration,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol.15, no.10, pp.1101–1110, Oct. 2007.

[12] Standard Performance Evaluation Corporation, “The SPEC CPU

2006 Benchmark Suite," http://www.specbench.org

[13] N. Binkert, S. Sardashti, R. Sen, K. Sewell, M. Shoaib, N. Vaish, M.D. Hill, D.A. Wood, B. Beckmann, G. Black, S.K. Reinhardt, A. Saidi, A. Basu, J. Hestness, D.R. Hower, and T. Krishna, "The gem5 simulator," ACM SIGARCH Computer Architecture News, vol.39, no.2, pp.1–7, Aug. 2011.

[14] T. Sawada, T. Toshikawa, K. Yoshikawa, H. Takaya, K. Nii, and M. Nagata, "Immunity evaluation of SRAM core using DPI with on-chip diagnosis structures," Proc. Workshop on Electromagnetic Compatibility of Integrated Circuits (EMC Compo), pp.65–70, Nov. 2011.

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