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A Practical ZCS-PWM Boost DC–DC Converter with Clamping Diode-assisted Active Edge-Resonant Cell and Its Extended Topologies

Tomokazu Mishima, *Member, IEEE,* and Mutsuo Nakaoka, *Member, IEEE*

***Abstract*— This paper presents the performance evaluations of a ZCS-PWM boost dc–dc converter with a practical active edge resonant cell. The active edge resonant cell (AERC) treated and discussed herein has auxiliary diodes for suppressing voltage surges and current ringings at the commutations of active switches in the dc–dc converters. The voltage surges together with the current ringings can be effectively eliminated in the AERC owing to the effect of the clamping diodes. Therefore, voltage ratings of the active switches can be considerably reduced as compared to the classical AERC without the clamping diodes, consequently the conversion efficiency can be improved in the ZCS-PWM boost dc–dc converter. The practical effectiveness of the clamping diode-assisted ZCS-PWM boost dc–dc converter is demonstrated in detail by means of experimental verifications based on a $1.6\,\mathrm{kW}$-$40\,\mathrm{kHz}$ laboratory prototype. In addition, an extended topological family of non-isolated ZCS-PWM dc–dc converters employing the practical AERC is originally described for demonstrating the high scalability of the AERC.**

Keywards– boost dc–dc converters, zero current soft-switching (ZCS), pulse width Modulation (PWM), edge resonance, active edge-resonant cell (AERC), clamping diode.

I. INTRODUCTION

A variety of soft switching PWM boost dc–dc converters have been considered to be effective for reduction of switching power losses, switching surges, EMI noises and high frequency leak currents, which is practically required for improving the performance quality and reliability of the applied power electronics circuits and systems such as Photovoltaic (PV) and Fuel Cell power conditioners [1]–[26].

ZCS techniques are generally recognized as more suitable soft switching schemes for the MOS-gate controlled bipolar power devices such as Insulated Gate Bipolar Transistors (IGBTs) and Emitter Switched Bipolar Transistors (ESBTs) than Zero Voltage Soft-switching (ZVS) ones [18]–[24]. Then, the higher efficiency can be attained in the soft switching boost dc–dc converter than the conventional hard-switched and even RCD snubber-assisted boost dc–dc converters.

Switching cells for the ZCS operations originate in the two or three-terminal Pulse Frequency Modulated (PFM) resonant cells [19],[20] as illustrated in Fig. 1. By employing an auxiliary active switch in series with the resonant capacitor C_r, the ZCS-PFM resonant cells can be modified into the two or three-terminal ZCS-PWM AERC operating under the constant switching frequency conditions as shown in Figs. 2 (a) and (b).

The ZCS-PWM AERCs have been investigated in [21]–[29] as classical but simple and practical soft switching circuit topologies for boost converters [21]–[24], buck converters [27], Power Factor Correction (PFC) converters [25],[26], and high frequency transformer-linked dc–dc converters [28],[29]. In the ZCS-PWM boost dc–dc converters, the soft commutating operations can be performed both in main and auxiliary switches under the wide range of load power variation[23]–[25] since the full-wave resonant currents that are required for ensuring the soft commutations are available for the full load-range. Although the resonant currents are relatively outstanding under the light load conditions, the ZCS-PWM AERCs with the clamping diodes are useful, attractive and still better candidates as soft switching cells which are suitable for the practical power converters from the view points of a wide range of soft-switching operation and a less number of the circuit components [1].

The technical issue of the ZCS-PWM AERCs is occurrences of voltage surges and current ringings at the turn-off transitions of the anti-parallel diodes that are necessary for attaining Zero Current and Zero Voltage Soft-switching (ZCZVS) of each active switch, as illustrated in Fig. 3 [10], [21]–[24]. The voltage surges and current ringings are caused by the oscillation due to the parasitic output capacitance of the active switch and the inductance including the resonant inductor in the AERC. Then, the voltage ringings lead to the increase of voltage stresses for the active switches, so that the performances and conversion efficiency of the ZCS-PWM boost dc–dc converters are degraded because of the relatively high saturation voltage of the power devices. It should be noted here that the occurrence of the surges and ringings mentioned above are not only limited to the AERCs illustrated in Figs. 2 (a) and (b), but also another types of the AERCs with the reduced peak-resonant currents [15], [25] as well as a ZVS-PWM cell [17].

In order to overcome the drawbacks of the ZCS-PWM AERCs, the introduction of clamping diodes into the AERC as introduced in Figs. 2 (c) and (d) is considered to be an

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[1]Comparisons between ZCS-PWM boost dc–dc converters are described in APPENDIX I.

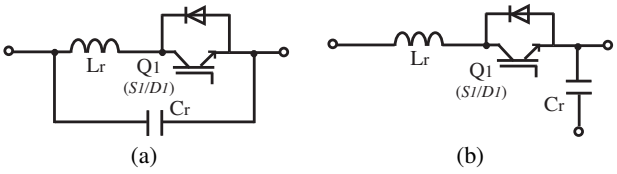


Fig. 1. ZCS-PFM resonant cells: (a) two-terminal, (b) three-terminal.

effective and practical solution. The implementation of the clamping diodes are quite effective for suppressing the voltage surge in each active switch without any lossy component. In addition to this, even a small amount of power inherent to the voltage and current ringings can be recycled to the input dc power source (regenerating) or to the load (redelivering). This contributes to improvement of the converter efficiency and enhancement of energy utilization from the dc–dc converter-interfaced power sources, which is especially useful for the renewable and sustainable energy-based power generation and conditioning systems. Moreover, the EMI noise level can be well reduced, which yields to improvement of the performance quality and reliability of the soft switching PWM dc–dc converters.

The similar approaches have been previously introduced in [21] and [22], but the detailed investigations on the actual switching performances and functionality are not presented and discussed enough to verify the effects of the clamping diodes.

In order to clarify the effect of the clamping diodes, the experimental evaluations were carried out and their results were reported by the authors in [24]. By adding the more detailed theoretical and experimental datum including a power loss analysis into the authors' previous work, this paper is dedicated for actually demonstrating the advantages of the practical ZCS-PWM boost dc–dc converter with the clamping diode-assisted AERC. Furthermore, its extended circuit topologies for other non-isolated PWM dc–dc converters are originally presented, then the high scalability of the ZCS-PWM AERC with the clamping diodes are schematically and theoretically demonstrated.

This paper is organized as follows: the factors of causing the voltage surges and current ringings are described in Section II. Then, the operating principle of the clamping diode-assisted ZCS-PWM boost dc–dc converter is explained. Moreover, its extended circuit arrangements for all types of the non-isolated ZCS-PWM dc–dc converters are originally introduced. In the following Section III, the soft switching range attained by the ZCS-PWM boost dc–dc converter with the clamping diode-assisted AERC is theoretically discussed and explained. Furthermore, the switching performance and static characteristics of the clamping diode-assisted AERC are demonstrated by experimental results based on its laboratory prototype of the ZCS-PWM boost dc–dc converter in Section IV. Finally, the practical effectiveness of the clamping-diode assisted AERC is evaluated from the view points of conversion efficiency and high frequency switching operations in Section V.

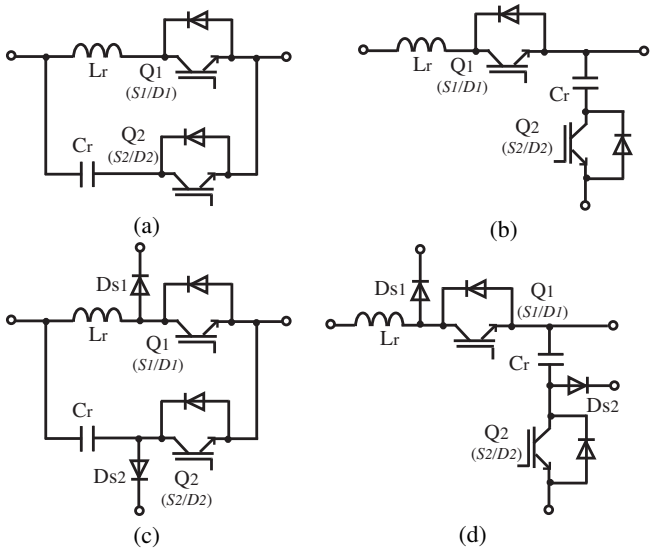
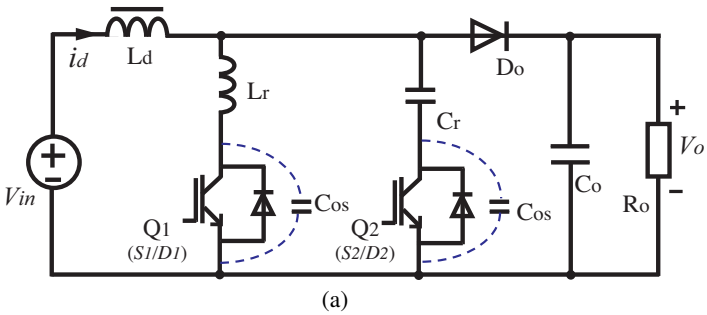


Fig. 2. ZCS-PWM AERC circuit topologies: (a) two-terminal, (b) three-terminal, (c) four-terminal, (d) five-terminal.



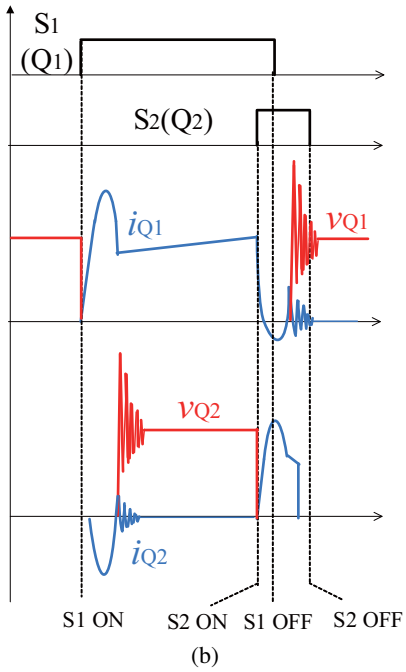


Fig. 3. Voltage surges and current ringings in ZCS-PWM boost dc–dc converter with two-terminal AERC: (a) circuit diagram with parasitic capacitances, (b) operating waveforms in active switches.

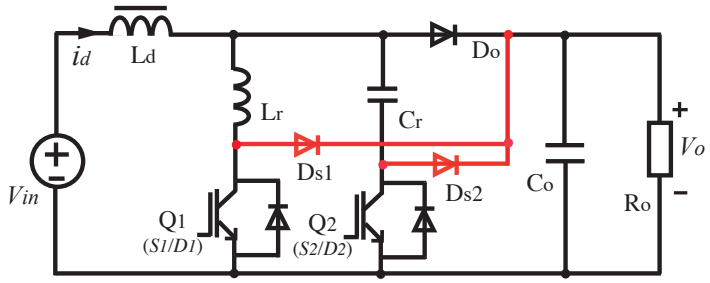


Fig. 4. Clamping diode-assisted ZCS-PWM boost dc–dc converter with four-terminal AERC.

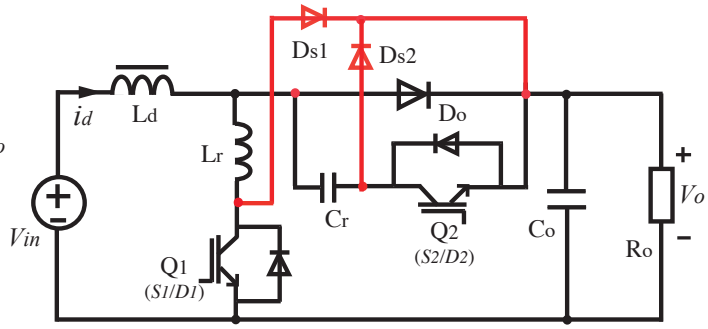


Fig. 5. Clamping diode-assisted ZCS-PWM boost dc–dc converter with five-terminal AERC.

II. Clamping Diode-Assisted ZCS-PWM Boost dc–dc Converters and Its Extended Circuits

A. Circuit Configuration

The circuit topology of the ZCS-PWM boost dc–dc converter with the two-terminal AERC is depicted in Fig. 3 (a), which consists of one main active switch Q_1 assisted with one auxiliary active switch Q_2, a resonant inductor L_r and a resonant capacitor C_r. In addition, the relevant operating waveforms of the AERC are shown in Fig. 3 (b). The parasitic output capacitance C_{os} exists in each active switch, and resonates with L_r at the turn-off transitions of D_1 and D_2 as depicted in Fig. 3 (b).

The theoretical one-cycle period of the ringing transition $t_p\,(=2\pi\,/\,\omega_p)$ in Q_1 and Q_2 due to the free oscillation in the AERC is defined by

$$t_p = \frac{2\pi}{\sqrt{\frac{1}{L_r C_{os}} - \left(\frac{r_l}{2L_r}\right)^2}}, \tag{1}$$

where r_l denotes the internal resistance in the AERC. Then, the voltage surge v_{sr} in Q_1 and Q_2 can be expressed by

$$\begin{aligned} v_{sr} &= V_o\left[1 - e^{-\alpha t}\frac{\sin(\omega_p+\beta)\,t}{\sqrt{1-\frac{C_{os}}{L_r}\left(\frac{r_l}{2}\right)^2}}\right], \\ \alpha &= \frac{r_l}{2L_r}, \quad \beta = \sqrt{\frac{1}{L_r C_{os}} - \left(\frac{r_l}{2L_r}\right)}. \end{aligned} \tag{2}$$

The circuit configurations of the ZCS-PWM boost dc–dc converter with the clamping diode-assisted AERCs of Figs. 2 (c) and (d) are shown in Figs. 4 and 5, respectively. The clamping diodes D_{s1} and D_{s2} are connected in the midpoints between L_r, C_r and the active switches Q_1, Q_2, respectively. The clamping diodes are forward-biased when the voltages v_{Q1} and v_{Q2} across Q_1 and Q_2 match with the output voltage V_o plus the forward-bias diode voltage V_F as given by

$$v_{Q1,Q2} = V_o + V_F \simeq V_o. \tag{3}$$

Thus, the voltages across the active switches can be naturally clamped to the output voltage, as a result the voltages and current ringings in Q_1 and Q_2 can be well reduced.

B. Operation Principle

The ideal operating waveforms and mode transitions with the equivalent circuits are illustrated in Fig. 6 and Fig. 7, respectively. One switching cycle operation of the ZCS-PWM boost dc–dc converter comprises the ten sub-modes including the commutation intervals of D_{s1} and D_{s2}. In order to simplify the explanation, it should be assumed herein that the input inductor L_d and the output capacitor C_o are large enough to establish the circuit conditions of the current source I_d in the input and voltage source V_o in the output, respectively.

- Mode 1 [t_0–t_1],<*main switch* Q_1 *ZCS turn-on mode*>: While the output D_o is now conducting, S_1 of Q_1 is turned on. Then, the switch current i_{Q_1} begins to increase softly with the aid of L_r, thereby the ZCS turn-on can be achieved in Q_1. During this mode, the clamping diode D_{s1} is conducting a small amount of current i_{Ds1}, which naturally decays at the end of this mode interval owing to the ZCS turn-on commutation of Q_1.
- Mode 2 [t_1–t_2], <L_r-C_r *resonant mode*>: Edge-resonance due to L_r and C_r begins after D_{s2} is turned off at the time t_1, and then D_2 of the auxiliary switch Q_2 delivers the resonant current circulating in the AERC. Consequently, the resonant capacitor C_r begins to be charged in the reverse polarity and its voltage v_{cr} gradually decreases.

The current i_{Q1} through the main switch during its turn-on transition interval ($t_{0-2} \simeq t_{1-2}$) is expressed by

$$\begin{aligned} i_{Q1}(t) &= \frac{v_{cr}(t_1)}{Z_q}\cdot\sin\omega_r(t-t_1) + I_d, \\ &= \frac{V_o}{Z_q}\cdot\sin\omega_r(t-t_1) + I_d, \end{aligned} \tag{4}$$

where $\omega_r = 1/\sqrt{L_r C_r}$, $Z_q = \sqrt{L_r/C_r}$. In addition, $v_{cr}(t_1)$ represents the capacitor voltage across C_r at t_1, which is ideally equal to V_o.

In the similar way, i_{Q2} through the auxiliary switch Q_2 is defined by

$$i_{Q2}(t) = -\frac{V_o}{Z_q}\cdot\sin\omega_r(t-t_1). \tag{5}$$

From the beginning of this mode to the end of the following mode (the time interval t_1–t_2), the capacitor voltage v_{cr} can be defined by

$$v_{cr}(t) = V_o\cdot\cos\omega_r(t-t_1). \tag{6}$$

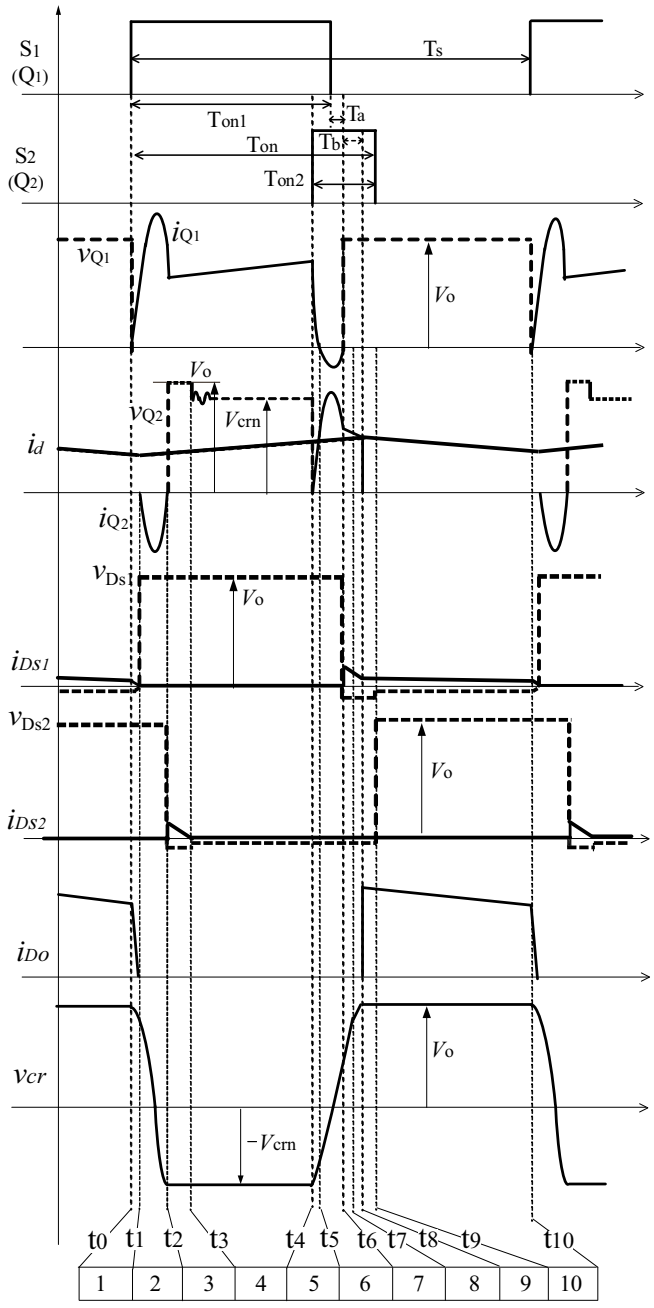


Fig. 6. Relevant operating waveforms for one switching cycle.

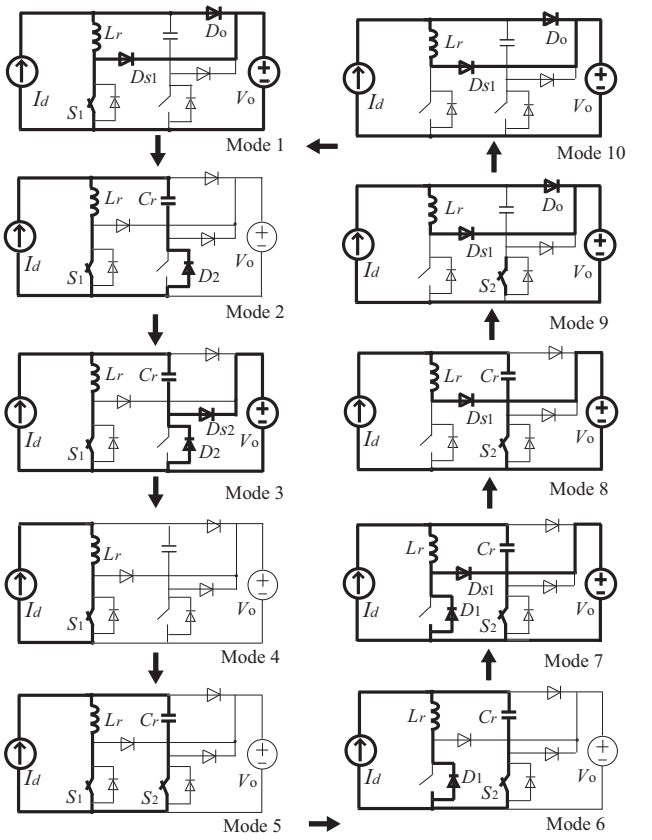


Fig. 7. Operating mode transitions and simplified equivalent circuits during one switching cycle.

- Mode 3 [t_2–t_3], <*clamping diode D_{s2} forward-bias mode*>: The resonant current i_{Q2} gets down to zero-level at $t = t_1$, and the clamping diode D_{s2} is forward-biased. Thereby, the voltage across Q_2 is clamped to V_o, and then the conduction of the anti-parallel diode D_{s2} is terminated without any occurrence of parasitic oscillation. The resonant capacitor C_r is reversely charged, and at the time point t_2 the capacitor voltage v_{cr} reaches into the negative peak values V_{crn} which is described by

$$V_{crn} = -V_o \cdot \cos \omega_r (t_2 - t_1). \quad (7)$$

It can be remarked herein that the time interval from t_1 to t_2 is shorter than half the resonant period of L_r and C_r as given by

$$t_2 - t_1 = \omega_r \cdot \cos^{-1}\left(-\frac{V_{crn}}{V_o}\right) < \pi\sqrt{L_r C_r}. \quad (8)$$

- Mode 4 [t_3–t_4], <*input inductor L_d energy storing mode*>: In this mode, the input DCL L_d is directly connected to V_{in} via L_r and Q_1, so that the input current increases in a linear manner. After the occurrence of small ringing period due to the parasitic inductance together with L_r and the parasitic capacitance in D_{s2}, the voltage v_{Q_2} across Q_2 is ideally fixed to V_{crn}. The cathode to anode voltage V_{KADs2} across D_{s2} corresponds to $V_o - V_{crn}$.
- Mode 5 [t_4–t_5], <*auxiliary switch Q_2 ZCS turn-on mode*>: Prior to the turn-off commutation of S_1 in the main switch Q_1, S_2 of the auxiliary switch Q_2 is turned on. Then, the current i_{Q_2} through Q_2 increases softly with the edge-resonance due to L_r and C_r, thereby the soft turn-on commutation of Q_3 can be performed under the ZCS condition. In this operating mode, the current through each active switch can be defined by

$$i_{Q1}(t) = I_d - \frac{V_{crn}}{Z_q} \cdot \sin \omega_r (t - t_4), \quad (9)$$

$$i_{Q2}(t) = \frac{V_{crn}}{Z_q} \cdot \sin \omega_r (t - t_4). \quad (10)$$

- Mode 6 [t_5–t_6], <*main switch Q_1 ZCZVS turn-off mode*>: Commutation of i_{Q_1} from S_1 to D_1 in the main

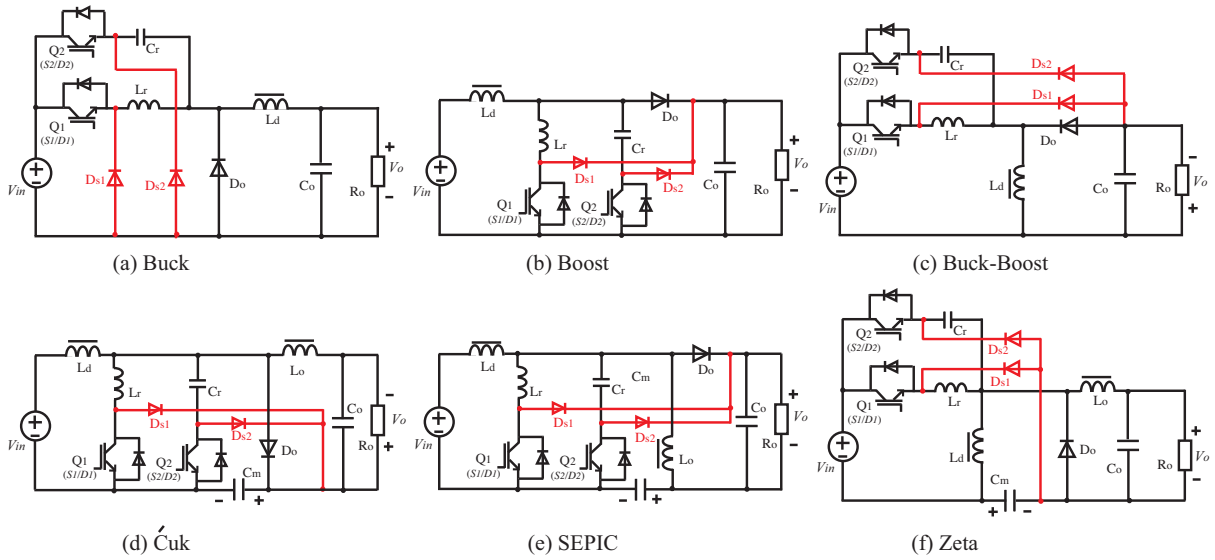


Fig. 8. Six non-isolated ZCS-PWM dc–dc converters with clamping diode-assisted AERC (four-terminal type): (a) Buck, (b) Boost, (c) Buck-Boost, (d) Ćuk, (e) SEPIC, (f) Zeta.

switch Q_1 completes naturally owing to the resonance continuing from the previous mode. During this interval, S_1 is turned off, thereby the ZCZVS mode turn-off operation can be completely achieved in Q_1.

- Mode 7 [t_6–t_7], <*clamping diode D_{s1} forward-bias mode*>: The resonant current i_{Q1} gets down to the zero-level, and the clamping diode D_{s1} is forward-biased at $t = t_5$. Thereby, the voltage across Q_1 is clamped to V_o, and the residual energy in L_r is continuously fed to the output load via D_{s1}. In the end of this interval, the conduction of the anti-parallel diode D_{s1} is terminated without any parasitic oscillation.
  From the beginning of Mode 5 to the end of Mode 7 (t_4–t_7), the resonant capacitor voltage v_{cr} can be expressed by

$$v_{cr}(t) = -V_{crn} \cdot \cos \omega_r (t - t_4). \tag{11}$$

- Mode 8 [t_7–t_8], <*resonant capacitor C_r charging mode*>: Following to the previous mode, a great part of input current I_d flows into C_r, then the voltage across C_r linearly increases as written by

$$v_{cr} = \frac{I_d}{C_r} \cdot (t - t_7). \tag{12}$$

  The capacitor voltage v_{cr} rises up to the same level as V_o at $t = t_8$, consequently the output diode D_o is naturally forward-biased.
- Mode 9 [t_8–t_9], <*auxiliary switch Q_2 ZCS turn-off mode*>: After $t = t_8$, no current is delivered into C_r and Q_2. During this interval, the gate signal for S_2 is removed, thereby the ZCS turn-off commutation can be attained in Q_2.
- Mode 10 [t_9–t_{10}], <*input inductor L_r energy releasing mode*>: The input current I_d is delivered to the output side mainly via D_o. During this interval, the energy in L_d is released and then the input voltage V_{in} is lifted to the output voltage V_o with the effect of the voltage across L_d.

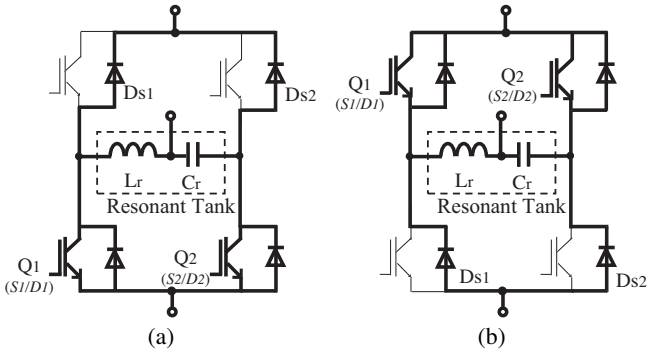


Fig. 9. Conceptual circuit arrangements of clamping diode-assisted AERCs based on H-bridge IGBT module: (a) for Boost, Ćuk and SEPIC, (b) for Buck, Buck-Boost, and Zeta.

Since the relatively small amounts of currents through D_{s1} and D_{s2} pass during the short durations as mentioned above, the conduction power losses of the clamping diodes D_{s1} and D_{s2} can be minimized.

C. Extended AERC Circuits for Non-Isolated ZCS-PWM DC–DC Converters

The clamping diode-assisted AERCs can be applied for all of the non-isolated PWM dc–dc converters (Buck, Boost, Buck-Boost, Ćuk, SEPIC and Zeta) as illustrated in Fig. 8.

The family of ZCS-PWM dc–dc converters with the clamping diode-assisted AERC is classified into two types: the current ringing regenerating and redelivering types. The current ringings in the AERCs are returned back to the input dc power source via D_{s1} and D_{s2} in the voltage source-type converters (Buck, Buck-Boost and Zeta). Therefore, the regenerating operation can be achieved. On the other hand, the ringing currents are forwarded into the load via D_{s1} and D_{s2} in the current source-type converters (Boost, Ćuk and

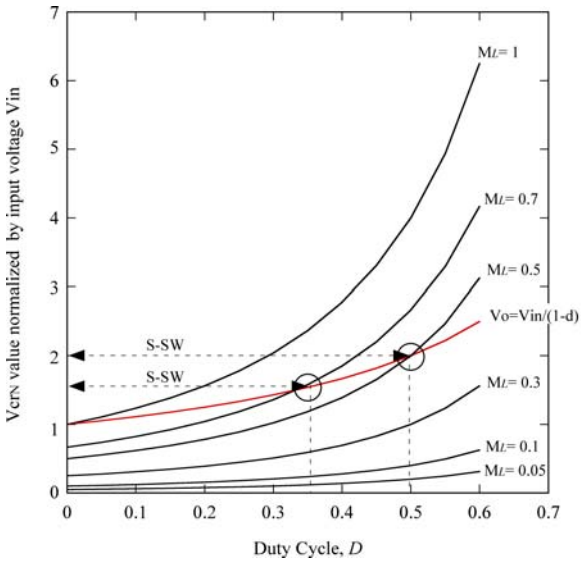


Fig. 10. Relationship between steady-state negative voltage V_{crn} across resonant capacitor C_r and duty cycle D with soft switching range.

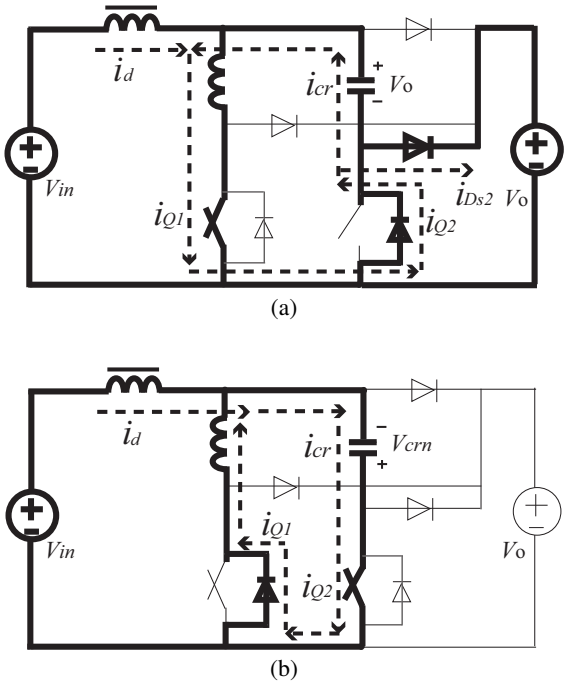


Fig. 11. Current flows for commutations in AERC: (a) Q_1 turn-on (initial value of V_{cr} is V_o), (b) Q_2 turn-on (initial value of V_{cr} is $-V_{crn}$).

SEPIC), which implies that the redelivering operation can be successfully performed.

According to the circuit topologies of the non-isolated PWM dc–dc converters mentioned above, the ZCS-PWM AERCs with the clamping diodes can be implemented by H-bridge IGBT modules as conceptually illustrated in Fig. 9.

The peak voltages and current stresses of the power devices and circuit components are summarized in TABLE I in accordance with the circuit topologies of the proposed ZCS-PWM dc–dc converter family. Note here that Z_p represents the resonant characteristic impedance due to L_r and C_{os} as defined by

$$Z_p = \sqrt{\frac{L_r}{C_{os}} - \left(\frac{r_l}{2}\right)^2}. \tag{13}$$

III. Consideration for Soft Switching Range

The ZCZVS turn-off operation in the main switch Q_1 depends on both the load resistance R_o and the resonant tank impedance Z_q of AERC.

The condition for achieving the ZCZVS turn-off commutation in Q_1 is simply given by

$$V_{crn} \geq M_L \cdot \frac{V_{in}}{(1-D)^2}, \tag{14}$$

$$M_L = \frac{Z_q}{R_o} = \frac{\sqrt{L_r/C_r}}{R_o}, \tag{15}$$

where M_L represents the ratio of the resonant tank impedance Z_q to the load resistance R_o. Furthermore, D denotes the on-duty cycle that can be defined with the switching period T_s by

$$D = \frac{T_{on}}{T_s} \simeq \frac{T_{on1} + T_a + T_b}{T_s}, \tag{16}$$

where T_a and T_b consist of the switch-on interval of the auxiliary switch Q_2 as indicated in Fig. 6, and they can be written by

$$T_a = \frac{\pi\sqrt{L_r C_r}}{2}, \tag{17}$$

$$T_b = C_r \cdot \frac{V_o - v_{cr}(t_6)}{I_d}. \tag{18}$$

Fig. 10 illustrates the characteristic curves of the steady-state negative voltage value V_{crn} in C_r with normalization by the input voltage V_{in}.

The resonant capacitor voltage v_{cr} has the two kinds of steady state-peak values V_o and V_{crn} for the positive and negative polarities as indicated in Fig. 6. The resonant currents circulating in the AERC are illustrated in Fig. 11. According to (6)–(8), the negative peak value V_{crn} of v_{cr} is less than the output voltage V_o as expressed by

$$\begin{aligned} V_{crn} &= -V_o \cdot \cos\omega_r(t_2 - t_1) \\ &< -V_o \cdot \cos\pi = V_o. \end{aligned} \tag{19}$$

From the view point of the complete soft switching operation in all the active switches, the maximum limit of the duty cycle variation can be decided by the cross points between the curves of V_o and V_{crn}. Therefore, it can be seen from Fig. 10 that the theoretical soft switching range, which is indicated by "S-SW", is $0 < D \leq 0.5$ for $M_L = 0.5$ while that is $0 < D \leq 0.35$ under the condition of $M_L = 0.7$. Thus, the soft switching range can be enlarged as the M_L value decreases.

IV. Experimental Results and Evaluations

A. Specification of Laboratory Prototype

The effectiveness of the four-terminal ZCS-PWM AERC with the clamping diodes in Fig. 2(c) is investigated in

TABLE I

VOLTAGE AND CURRENT STRESSES OF POWER DEVICES IN ZCS-PWM DC–DC CONVERTERS WITH CLAMPING DIODES.

Topologies \ switches		Q_1	Q_2	D_{s1}	D_{s2}	D_o	V_o/V_{in}
Buck	voltage	V_{in}	V_{in}	V_{in}	V_{in}	$2V_{in}$	D
	current	$\frac{V_{in}}{Z_q}$	$\frac{V_{in}}{Z_q}$	$\frac{Vin}{Z_p}$	$\frac{Vin}{Z_p}$	$I_d + \frac{(1-D)DT_s}{2L_d} \cdot V_{in}$	
Boost	voltage	V_o	V_o	V_o	V_o	$2V_o$	$\frac{1}{(1-D)}$
	current	$\frac{V_o}{Z_q}$	$\frac{V_o}{Z_q}$	$\frac{Vo}{Z_p}$	$\frac{Vo}{Z_p}$	$I_d + \frac{DT_s}{2L_d} \cdot V_{in}$	
Buck-Boost	voltage	$V_{in} + V_o$	$V_{in} + V_o$	$V_{in} + V_o$	$V_{in} + V_o$	$2V_{in} + V_o$	$\frac{D}{(1-D)}$
	current	$\frac{V_{in}+V_o}{Z_q}$	$\frac{V_{in}+V_o}{Z_q}$	$\frac{V_{in}+V_o}{Z_p}$	$\frac{V_{in}+V_o}{Z_p}$	$I_d + \frac{DT_s}{2L_d} \cdot V_{in}$	
Ćuk	voltage	$V_{in} + V_o$	$V_{in} + V_o$	$V_{in} + V_o$	$V_{in} + V_o$	$2(V_{in} + V_o)$	$\frac{D}{(1-D)}$
	current	$\frac{V_{in}+V_o}{Z_q}$	$\frac{V_{in}+V_o}{Z_q}$	$\frac{V_{in}+V_o}{Z_p}$	$\frac{Vin+V_o}{Z_p}$	$I_o + I_d + \frac{DT_s}{2} \cdot (\frac{1}{L_d} + \frac{1}{L_o})V_{in}$	
SEPIC	voltage	$V_{in} + V_o$	$V_{in} + V_o$	$V_{in} + V_o$	$V_{in} + V_o$	$2(V_{in} + V_o)$	$\frac{D}{(1-D)}$
	current	$\frac{V_{in}+V_o}{Z_q}$	$\frac{V_{in}+V_o}{Z_q}$	$\frac{V_{in}+V_o}{Z_p}$	$\frac{V_{in}+V_o}{Z_p}$	$I_o + I_d + \frac{DT_s}{2} \cdot (\frac{1}{L_d} + \frac{1}{L_o})V_{in}$	
Zeta	voltage	$V_{in} + V_o$	$V_{in} + V_o$	$V_{in} + V_o$	$V_{in} + V_o$	$2(V_{in} + V_o)$	$\frac{D}{(1-D)}$
	current	$\frac{V_{in}+V_o}{Z_q}$	$\frac{V_{in}+V_o}{Z_q}$	$\frac{V_{in}+V_o}{Z_p}$	$\frac{V_{in}+V_o}{Z_p}$	$I_o + I_d + \frac{DT_s}{2} \cdot (\frac{1}{L_d} + \frac{1}{L_o})V_{in}$	

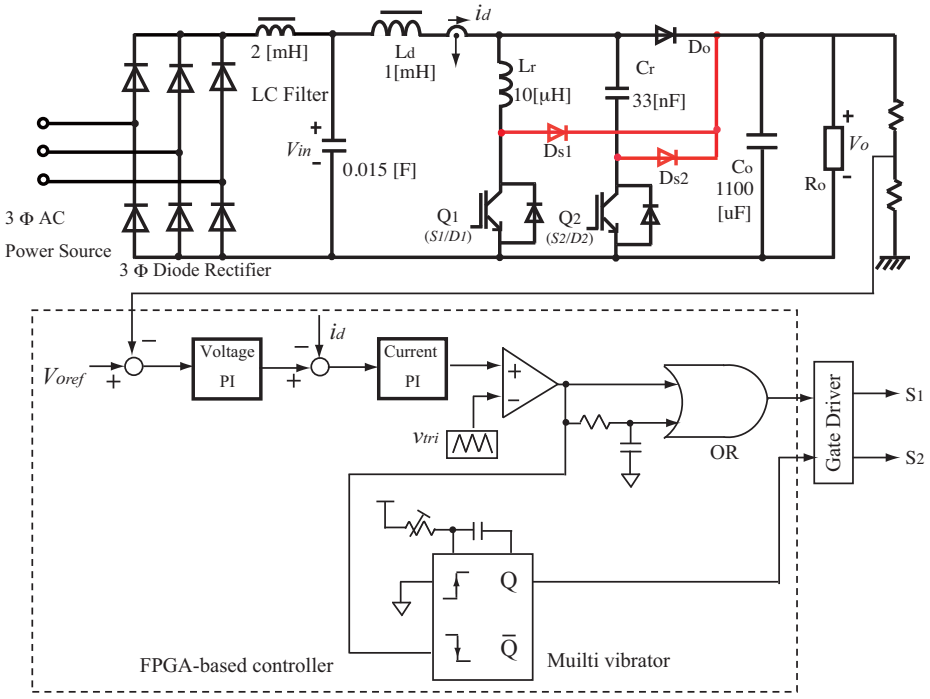


Fig. 12. Schematic diagram of experimental setup.

the 1.6 kW-40 kHz prototype of the ZCS-PWM boost dc–dc converter, as compared with the two-terminal ZCS-PWM AERC without the clamping diodes in Fig. 2 (a).

The schematic diagram of the experimental setup is illustrated in Fig. 12. In addition, the experimental conditions and circuit parameters are shown in TABLE II. The exterior appearances of the laboratory prototype and the experimental setup are provided in Fig. 13.

B. Switching Performances

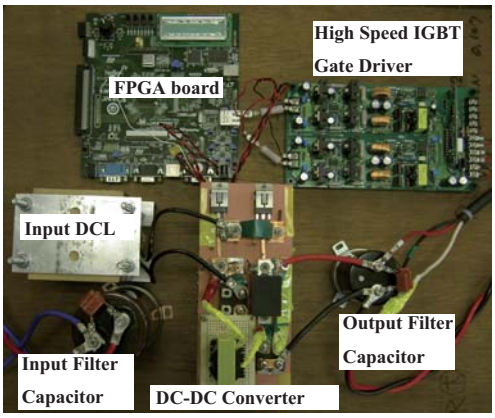
The voltage and current waveforms of Q_1 and Q_2 in the non-diode clamped two-terminal ZCS-PWM AERC are depicted in Fig. 14, where the voltage surges together with the current ringings are observed. Fig. 15 shows the enlarged waveforms of Q_1 and Q_2 during the turn-off transitions,

TABLE II

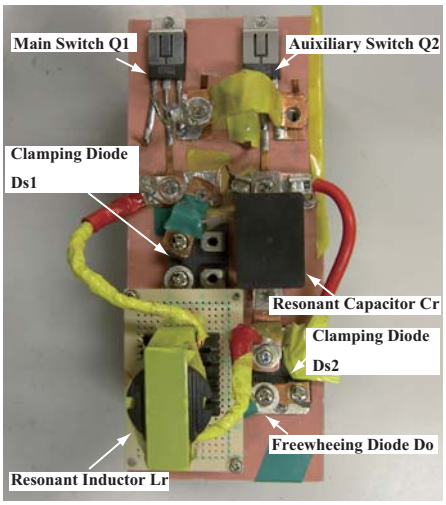
SPECIFICATIONS OF LABORATORY PROTOTYPE FOR ZCS-PWM BOOST DC–DC CONVERTER.

Parameter & symbol	value & unit
DC input voltage V_{in}	$160 - 170$ V
DC output voltage V_o	240 V
Output power (maximum)	1.6 kW
Switching frequency f_s	40 kHz
Resonant inductor L_r	10 μH
Resonant capacitor C_r	33 nF
Input DCL L_d	1 mH
Output smoothing capacitor C_o	1100 μF
Parasitic capacitance C_{os}	210 pF

·Q_1, Q_2 (IGBT): IXGR 40N60B2D1, 600 V, 75 A
·D_{s1}, D_{s2}, D_o (FRD): DSEI 2x 30, 600 V, 2 × 30 A



(a)



(b)

Fig. 13. Exterior appearance of laboratory prototype for diode-clamped ZCS-PWM boost dc–dc converter: (a) dc–dc converter setup, (b) AERC with clamping diodes.

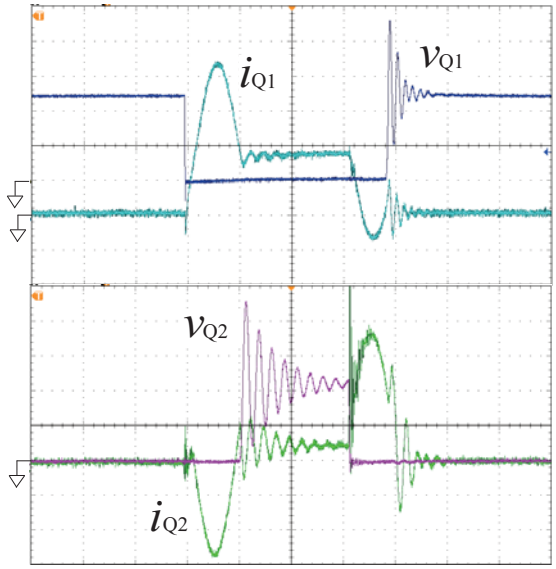
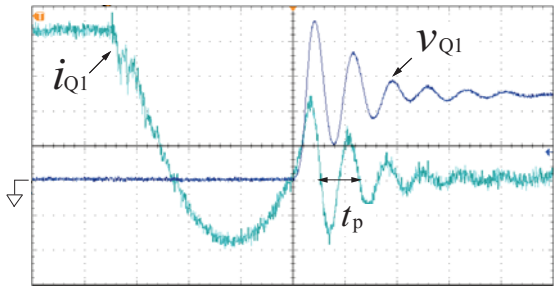
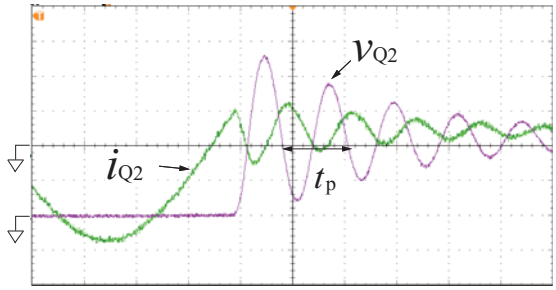


Fig. 14. Switching waveforms of Q_1, Q_2 without clamping diodes at $D = 0.3$ (v_{Q1}, v_{Q2}: 100V/div., i_{Q1}: 5A/div, i_{Q2}: 4A/div, time: 2μs/div).



(a)



(b)

Fig. 15. Parasitic voltage and current ringings in Q_1, Q_2: (a) main switch Q_1, (b) auxiliary switch Q_2 (v_{Q1}, v_{Q2}: 100 V/div, i_{Q1}: 2 A/div, i_{Q2}: 4 A/div, time: 400 ns/div).

respectively. The voltage surges in Q_1, Q_2 are 460 V, which is almost two times as high as the output voltage V_o (= 240 V). Those voltage surges and current ringings will also induce more conductive and radiative EMI noises in the power converter and the peripheral apparatuses as well as decreases the power conversion efficiency.

Assuming that the internal resistance r_l of the AERC is neglected, the calculated ringing period t_p is obtained from (1):

$$t_p \simeq 2\,\pi\sqrt{L_r C_{os}} = 290\,\text{ns}. \tag{20}$$

Based on the experimental results, the ringing period t_p of Q_1 is about 300 ns, which almost corresponds with the theoretical one in (20). On the other hand, the ringing period t_p of Q_2 is estimated about 480 ns. The discrepancy between the measured and the calculated values is due to the influence of the parasitic capacitance of the boost diode D_o in the prototype.

The measured switching voltage and current waveforms of Q_1 and Q_2 in the clamping diode-assisted ZCS-PWM AERC are shown in Fig. 16. In addition, the enlarged voltage and current waveforms for the turn-off transitions of Q_1 and Q_2 are shown in Fig. 17. The voltage surges mentioned above are well suppressed, and then the turn-off voltages of Q_1 and Q_2 are clamped to the output voltage V_o (= 240 V). As a result, the current ringings are effectively eliminated at the turn-off transitions of the anti-parallel diodes D_1 and D_2.

Fig. 18 indicates the operating waveforms of the clamping diodes D_{s1} and D_{s2}, where the small amounts of currents related to the parasitic ringings are transferred to the output load. Thus, the regenerating operations can be practically

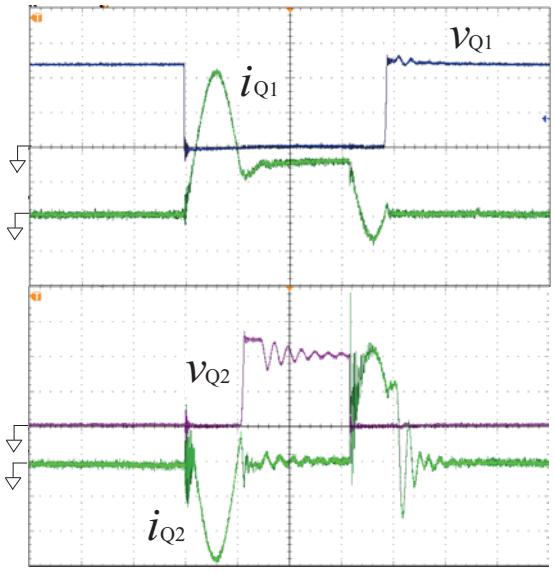


Fig. 16. Switching waveforms of Q_1, Q_2 with clamping diodes at $D = 0.3$ (v_{Q1}, v_{Q2}: 100 V/div., i_{Q1}: 5 A/div., i_{Q2}: 4 A/div., time: 2 μs/div).

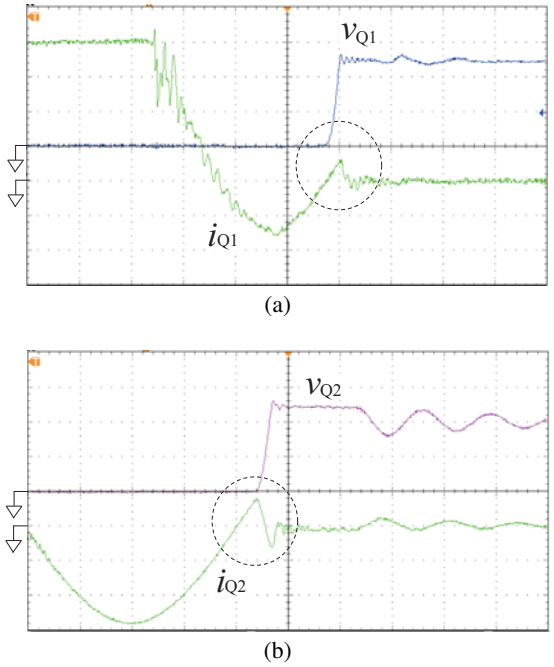


Fig. 17. Suppressed parasitic voltage and current ringings in Q_1, Q_2: (a) main switch Q_1, (b) auxiliary switch Q_2 (v_{Q1}, v_{Q2}: 100 V/div, i_{Q1}: 2 A/div, i_{Q2}: 4 A/div, time: 400 ns/div).

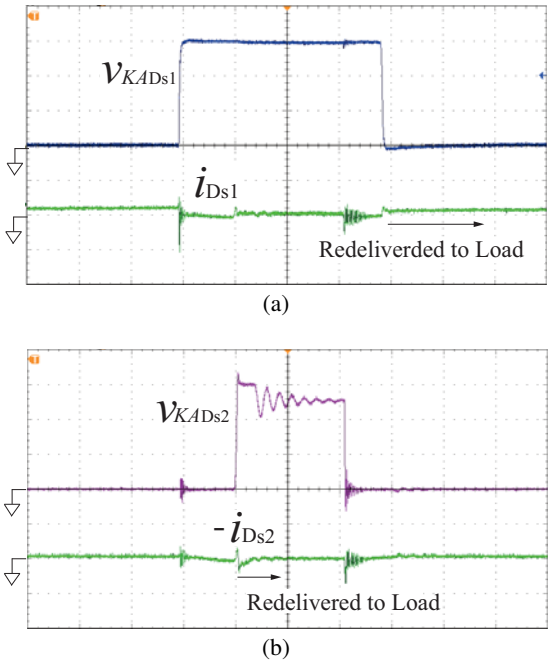


Fig. 18. Voltage and current waveforms of clamping diodes: (a) auxiliary diode D_{s1}, (b) auxiliary diode D_{s2} ($v_{KA(Ds1)}$, $v_{KA(Ds2)}$: 100 V/div, i_{Ds1}, i_{Ds2}, i_{Lr}: 10 A/div, time: 2 μs/div).

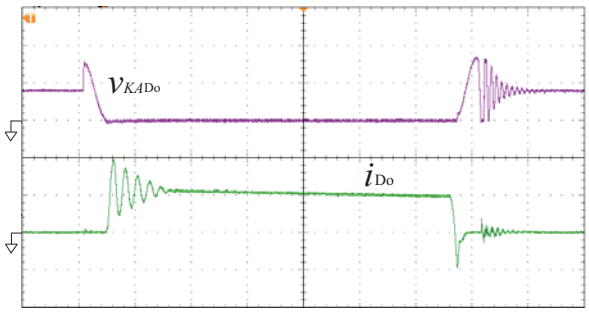


Fig. 19. Voltage and current waveforms of the output diode D_o ($v_{KA(Do)}$: 250 V/div, i_{Do}: 5 A/div, time: 2 μs/div)

TABLE III
COMPARISONS OF ENERGY LOSSES AT TURN-OFF TRANSITIONS IN D_1 AND D_2 (MEASURED AT OUTPUT POWER $P_o = 1$ kW AND SWITCHING FREQUENCY $f_s = 40$ kHz).

Item	Non-Clamped	Diode-Clamped
Turn-off energy loss E_{rr} in D_1	0.3 mJ	0.12 mJ
Turn-off energy loss E_{rr} in D_2	0.27 mJ	0.1 mJ

confirmed and verified in the clamping diode-assisted ZCS-PWM boost dc–dc converter. It can be observed in Fig. 18 that the small amount of current keeps passing through D_{s1} after the turn-off commutation of Q_1. This small current conduction can be eliminated by additionally employing a zener diode in series with D_{s1} [15],[21],[22].

The measured voltage and current waveforms in the output diode D_o are depicted in Fig. 19. The reverse recovery current of D_o can be alleviated by the effect of L_r in the AERC.

The energy losses at the turn-off transitions of the anti-parallel diodes D_1 in Q_1 and D_2 in Q_2 are compared between the non-clamped and the diode-clamped AERCs of the ZCS-PWM boost dc–dc converter in TABLE III. It can be clearly understood from the comparisons that the energy losses due to the voltage surges and current ringings can be effectively reduced in the AERC with the aid of the clamping diodes. It should be noted here that the effectiveness of the clamping diodes in the AERC will be more distinctive under the higher switching frequency operating condition.

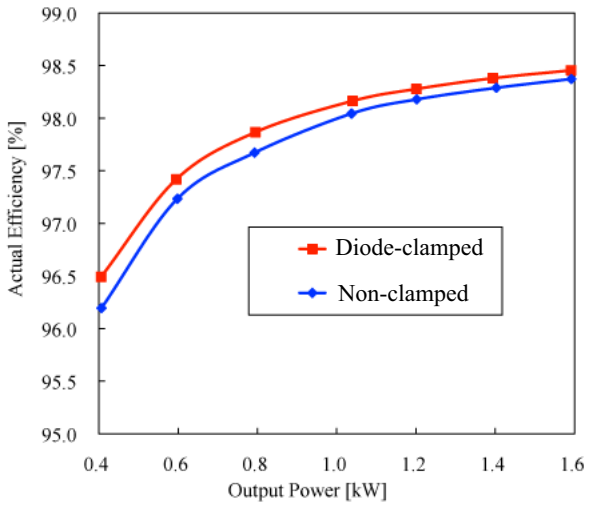


Fig. 20. Comparisons on actual efficiencies (measured by Digital Power Analyzer YOKOGAWA WT500).

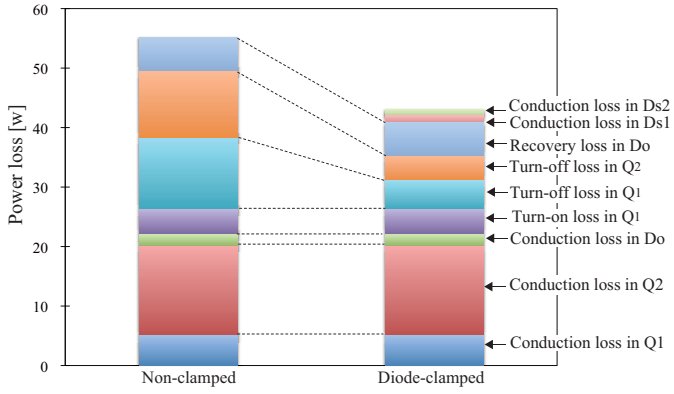


Fig. 21. Power loss analysis on diode-clamped and non-clamped AERCs: output power $P_o = 0.8\,\mathrm{kW}$.

C. Conversion Efficiencies

The actual conversion efficiencies are compared between the non-clamped and the diode-clamped ZCS-PWM boost dc–dc converters in Fig. 20, which are measured under the unified experimental condition. It can be confirmed from the result that the conversion efficiency can be improved in the whole power range by applying the clamping diodes into the AERC. This efficiency comparison indicates that no significant efficiency deterioration due to employing the additional clamping diodes emerges and affects the actual performances of the dc–dc converter.

The conversion efficiencies indicated in Fig. 20 are measured by using the same power devices for Q_1 and Q_2 in both the non-clamped and diode-clamped AERCs for evaluating the pure effects of the clamping diodes. Therefore, it should be remarked that the conversion efficiency can be improved more drastically by using lower voltage-rating power devices for the active switches Q_1 and Q_2 owing to the effect of the clamping diodes.

The power loss analysis on the non-clamped and diode-clamped AERCs are depicted in Fig. 21. The turn-off power losses of Q_1 and Q_2 are well reduced in the clamping diode-assisted AERC as compared with the non-clamped one, although the conduction power losses generate a little in the clamping diodes D_{s1} and D_{s2}, respectively. Thus, it can be known from the result that the clamping diodes D_{s1} and D_{s2} contribute effectively for reducing the turn-off power losses in Q_1 and Q_2, consequently the conversion efficiency of the ZCS-PWM boost dc–dc converter can be improved. Note in Fig. 21 that the turn-on power losses of the auxiliary switch Q_2 both in the diode-clamped and non-clamped ZCS-PWM AERCs are negligible due to the complete ZCZVS turn-on commutations.

V. Conclusions

The operating performances of the practical ZCS-PWM boost dc–dc converter topology with the clamping diode-assisted AERC (active edge-resonant cell) have been demonstrated and discussed in this paper. The $1.6\,\mathrm{kW}$-$40\,\mathrm{kHz}$ laboratory prototype of the clamping diode-assisted ZCS-PWM boost dc–dc converter with the high speed IGBTs has been built and tested for investigating the operations of the four-terminal AERC employing the clamping diodes. From the experimental results based on the prototype, the practical effectiveness of the clamping diode-assisted AERCs has been actually verified as summarized below:

- The clamping diodes work effectively for suppressing the voltage surges of the active switches and eliminating the current ringings in the AERCs.
- Lower voltage-rating power devices can be applied into the active switches in the ZCS-PWM AERCs, which is advantageous for producing the high power density, small size and low cost dc–dc converters.
- Improvement of the converter efficiency and reduction of the EMI noises can be effectively achieved.

Furthermore, the circuit topologies of the six non-isolated ZCS-PWM dc–dc converters using the AERCs with the clamping diodes have been originally presented in this paper. For power converters in renewable energy-based power generation systems, the redelivering-type AERCs are more suitable while the regenerating ones are quite effective for those of battery-source electric power systems.

The ZCS-PWM boost dc–dc converter treated in this paper is simple, practical and effective for using low voltage power devices and improving a conversion efficiency as well as reducing EMI noise emissions associated with the high frequency switching operations. Therefore, high power density due to a size and weight reduction attained by lifting the switching frequency, and high reliability owing to the low EMI noise level can be realized in the soft switching PWM dc–dc power converter that can be widely applied into the switching-mode power converters such as single phase / three-phase PFC converters.

APPENDIX I
TOPOLOGICAL COMPARISONS OF ZCS-PWM BOOST DC–DC CONVERTERS

Several types of ZCS-PWM AERCs with a reduced peak current have been proposed during the past decades, which are derived from the two-terminal ZCS-PWM AERC illustrated in Figs. 2 (a) and (b) by paying for increase of circuit components and limitation of a soft switching operation range[17]–[36]. Since the circuit configuration becomes complex and induces more transitional periods for the soft commutations, their applications seem to be rare in the industrial electric power converters.

The circuit topologies of ZCS-PWM boost dc–dc converters including the one in Fig. 4 are illustrated in Fig. 22. The comparison between the various circuit topologies are summarized in Tables IV and V in terms of the number of components, commutation and switching operations, although more detailed study should be carried out for the accurate comparisons in another opportunity.

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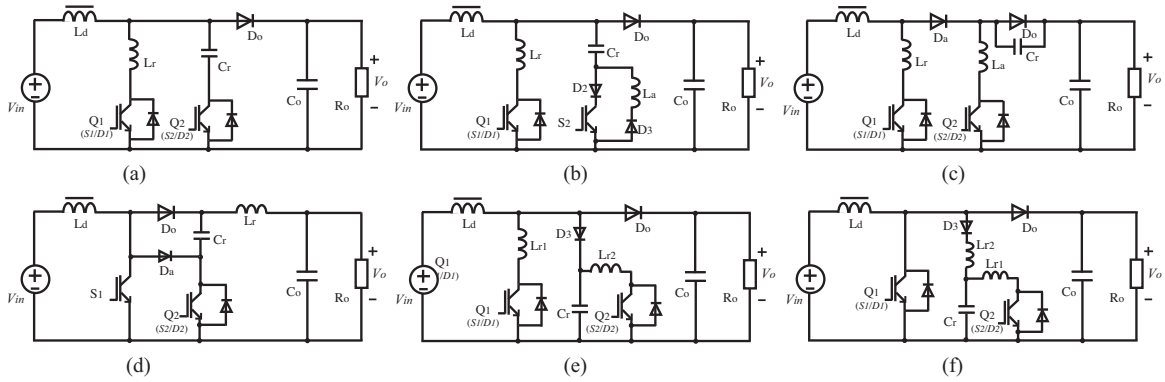

Fig. 22. ZCS-PWM boost dc–dc converters: (a) Type 1[21]–[26],[28], (b) Type 2[30], (c) Type 3[33], (d) Type 4[34], (e) Type 5[15], (f) Type 6[16].

TABLE IV

COMPARISONS OF SWITCHING CELLS FOR ZCS-PWM BOOST DC–DC CONVERTERS.

Topology	Number of Circuit Components excluding D_o		Commutations	
	power devices	passive components	main switch Q_1	auxiliary switch Q_2
Type 1	2 (2-switch)	2 (1-inductor, 1-capacitor)	ZCS turn-on / ZCZVS turn-off	ZCS turn-on / ZCS turn-off
Type 2	4 (2-switch, 2-diode)	3 (2-inductor, 1-capacitor)	ZCS turn-on / ZCZVS turn-off	ZCS turn-on / ZVS turn-off
Type 3	3 (2-switch, 1-diode)	3 (2-inductor, 1-capacitor)	ZCS turn-on / ZCZVS turn-off	ZCS turn-on / ZCS turn-off
Type 4	3 (2-switch, 1-diode)	2 (1-inductor, 1-capacitor)	ZCS turn-on / ZCS turn-off	ZCS turn-on / ZCS turn-off
Type 5	3 (2-switch, 1-diode)	3 (2-inductor, 1-capacitor)	ZCS turn-on / ZCZVS turn-off	ZCS turn-on / ZCZVS turn-off
Type 6	3 (2-switch, 1-diode)	3 (2-inductor, 1-capacitor)	ZCZVS turn-on / ZCZVS turn-off	ZCS turn-on / ZCZVS turn-off

TABLE V

COMPARISONS OF SWITCHING OPERATION.

Topology	Remarks
Type 1	The fully resonant currents generate in Q_1 and Q_2, so that a wide range of soft switching operations can be attained with less components. The condition losses in Q_1 and Q_2 are concerned under light load conditions.
Type 2	The fully resonant currents can be obtained as Type 1, but the number of the circuit components increases.
Type 3	The peak resonant current in Q_1 can be reduced with the assist of the additional resonant inductor L_a and the resonant capacitor C_r. Increase of the conduction losses in the two diodes D_a & D_o is concerned.
Type 4	The peak current is reduced in Q_1 with the assist of L_r. The drawback is the voltage stress in the boost diode D_o is twice as high as the one in a conventional hard-switched boost dc–dc converter. The ZCS turn-on condition in Q_1 is trade-off for reducing the circulating current in Q_2.
Type 5	No current stress appears in Q_1 by the effect of L_r and the parallel-connected auxiliary resonant tank. The conduction power loss in the auxiliary diode D_3 should be minimized. More capacitive energy in C_r is required as compared to Type 1 under the same condition of soft switching range.
Type 6	No current stress appears in Q_1 by the effect of the parallel-connected auxiliary resonant tank. A small amount of circulating current generates at the turn-on transition of Q_1. More capacitive energy in C_r is required as compared to Type 1 under the same condition of soft switching range. The inductive energy in L_{r1} can be regenerated to the load by employing an auxiliary circuit.

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