A Bridgeless BHB ZVS-PWM AC-AC Converter for High-Frequency Induction Heating Applications

Mishima, Tomokazu

Nakagawa, Yuki

Nakaoka, Mutsuo

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Tomokazu Mishima
Member, IEEE
Kobe University
5-1-1, Higashinada
Kobe, Hyogo 658-0022, Japan
mishima@maritime.kobe-u.ac.jp

Yuki Nakagawa
Non-member,
Kobe University
5-1-1, Higashinada
Kobe, Hyogo 658-0022, Japan
30w516w@stu.kobe-u.ac.jp

Mutsuo Nakaoka
Member, IEEE
Kyungnam University
Masan 630-701, Korea, and
University of Malaya
Kuala Lumpur, Malaysia

***Abstract*—A new prototype of a zero voltage soft-switching (ZVS) utility frequency ac (UFAC) to high-frequency ac (HFAC) resonant power converter for induction heating (IH) applications is presented in this paper. The series resonant ac-ac converter proposed herein can process the frequency conversion without any diode bridge rectifier (DBR), thereby reducing the relevant conduction power losses. In addition, power factor correction (PFC) can be naturally achieved by the inductor-based boost half-bridge (BHB) circuit with the non-smoothed dc (NSDC)-link. The operation principle together with a IH load power regulation scheme is described, and the converter performances including ZVS operations and PFC are demonstrated in an experiment with a 3.0 kW–30 kHz prototype by comparing with the previously-developed converter. Finally, the feasibility of the proposed ac-ac converter is evaluated from a practical point of view.**

Keywords*—Utility-frequency (UF)–high frequency (HF) ac-ac power converter, diode full-bridge rectifier-less (bridgeless), boost half-bridge (BHB), non-smoothed dc (NSDC)-link, power factor correction (PFC), zero voltage soft-switching (ZVS), pulse-width-modulation (PWM), induction heating (IH).

I. Introduction

IH power supplies for domestic and industry applications has been advanced with a wide variety of circuit topologies featuring soft switching technologies in the past decades, and now is getting into a new phase of research and development pursuing for high-efficiency and cost-effective electric power conversion and processing [1]– [9].

High-efficiency, low harmonics and high power factor are essentially demanded for the single-phase UFAC-HFAC power converter suitable for commercial power IH applications. The typical power conversion architecture for single-phase IH applications, as schematically drawn in Fig. 1, consist of three-stage power converters; UFAC–dc diode bridge rectifier (DBR), PFC converter (boost dc-dc converter), and dc–HF ac inverter. This circuit configuration is supported by the well-established power converter topologies, and has now been the basic power processing scheme in the domestic and consumer IH appliances. However, the multiple power conversion stages might lead to efficiency deterioration, consequently the further development of the ac-ac converter for attaining a higher power density could be obstructed.

In order to improve the efficiency with a cost-effective circuit configuration, the two-stage DBR-assisted BHB ZVS-PWM ac-ac converter as illustrated in Fig. 2 have been proposed and commercialized [10]. In this two-stage ac-ac converter, the NSDC–HFAC power processing can be performed simultaneously in the HF inverter stage, thereby the high efficiency and cost reduction can be attained. However, the DBR connecting the UFAC power source with the HF resonant inverter is still demanded, thus further improvement of the total efficiency can not be expected in the DBR-BHB ac-ac

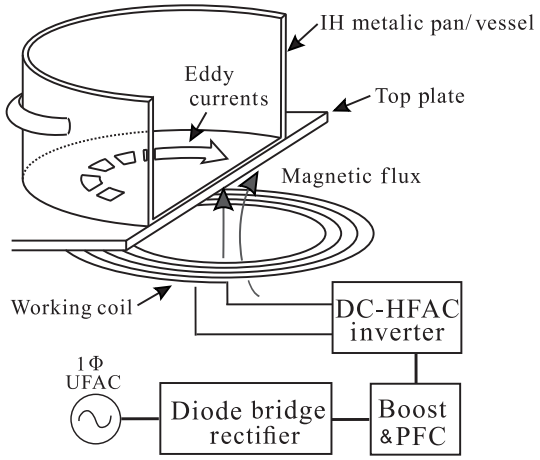


Fig. 1. Principle of induction heating with a typical three-stage power conversion.

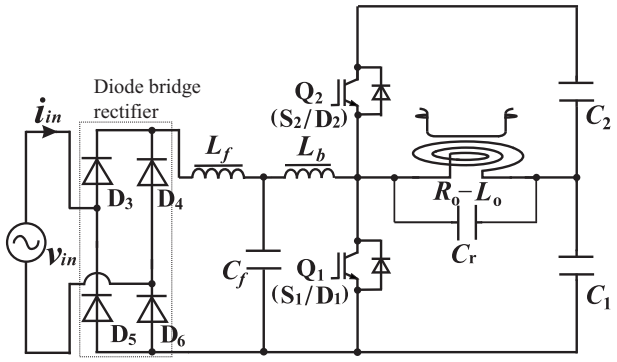


Fig. 2. A diode bridge rectifier (DBR)-assisted BHB ZVS-PWM ac-ac converter for IH applications [10].

converter.

A non-boost type single-stage ac-ac converter has been proposed [11], however the DBR is necessary and the cost-effectiveness is still in a challenge. Another types of single-stage ac-ac converter have been proposed by using bidirectional switches [12] [13], but the reliability of this new type of power device is not up to the practical level. The capacitor-boosted ac-ac converter that is free of the DBR, named as "bridgeless", has been proposed [14] [15], however no actively voltage regulation can be performed.

As a solution for the technical challenge of the DBR-assisted BHB topology as well as the other existing converters for the domestic and industrial IH applications, the innovative and cost-effective single-stage ZVS-PWM ac-ac converter with a series-resonant tank-applied IH load is proposed in this paper. The proposed ac-ac converter adopts the bridgeless BHB topology with the NSDC-link, whereby the UFAC-HFAC power conversion can be achieved with the passive PFC and the inductor-assisted voltage boost functions using insulated-gate-bipolar-transistors (IGBTs).

A ac-ac converter with similar functions to the circuit topology proposed herein has been presented in [16]. However, this ac-ac converter is based on the series resonant HF inverter by using the dc-link divided capacitors as resonant elements, thereby possibly inducing larger current ripples in the HF inverter stage and relevant power losses of capacitors. On top of that, there is no concept of the NSDC-link, and the essential performances such as an actual power conversion efficiency, PFC operation and ZVS range depending on the input-side source voltage level are not discussed in details in the literature.

The rest of this paper is organized as follows. The circuit configuration and operation principle with the commutating mode transitions of the proposed ac-ac converter are explained in Section II. The ZVS range of the ac-ac converter proposed herein is discussed with the aid of simulation analysis in Section III, thereby clarifying the ZVS behavior with consideration for the UFAC source voltage level and IH load power. Furthermore, the experimental results and practical evaluations of its laboratory prototype of 3.0 kW–30 kHz are demonstrated in Section V. Finally, the unique and advantageous properties of the proposed ac-ac converter are summarized in Section VI.

II. Proposed Bridgeless BHB AC-AC Converter

A. Circuit Configuration and Operation Principle

The main circuit diagram of the proposed ac-ac converter is depicted in Fig. 3 [17]. It should be noted here that the IH load and working coil are expressed by the series equivalent resistance and inductance R_o–L_o on the basis of HF transformer model. The utility-side L_f and C_f consist of the low-pass filter for eliminating the switching frequency component from the utility current i_{in}. The theoretical voltage and current waveforms for the UFAC cycle of the proposed ac-ac converter are displayed in Fig. 4.

The active switches Q_1, Q_2 comprise the BHB circuit that integrates the boost voltage regulator and the half-bridge HF load resonant inverter [18]. The source voltage v_{in} is lifted to the voltages v_{c1} and v_{c2} across the NSDC-link film capacitors

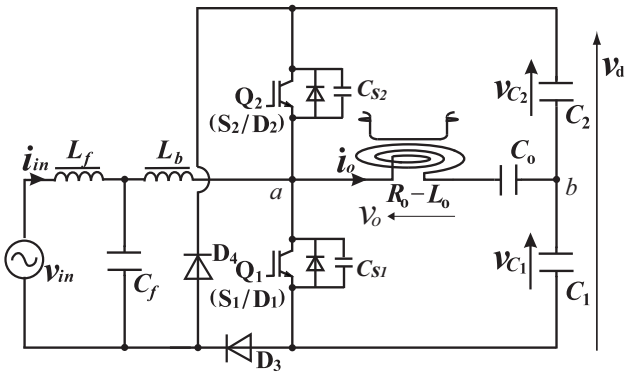


Fig. 3. A proposed bridgeless BHB ZVS-PWM ac-ac converter for IH applications.

C_1 and C_2 by the effect of the inductor L_b in the HFAC cycle. Besides that, PFC can be naturally achieved by the BHB circuit due to the NSDC-link voltage which is synchronous to the full-wave rectified waveform of v_{in} as depicted in Fig. 4.

The HF power is supplied into the IH load by the series-resonant tank comprised of C_o and the inductive load R_o-L_o. The capacitors C_{s1}, C_{s2} work as the lossless snubbing capacitors with L_o for ZVS commutations in Q_1 and Q_2. Therefore, the switching power losses can be effectively reduced as well as the switching noise in the proposed ac-ac converter.

The IH load power is controlled by asymmetrical pulse-width-modulation (A-PWM) with a dead time interval T_d for a switching cycle T_s as indicated in Fig. 5, where the duty cycle D is defined as

$$D = \frac{T_{on}}{T_s} < 0.5. \tag{1}$$

In order to make the symmetrical circuit operation for the positive and negative half-cycles of v_{in}, the gate signal pattern for adjusting D is exchanged in accordance with the polarity of v_{in} as illustrated in Fig. 6. The dc voltage and current components which are inherent to the A-PWM scheme controlled HF inverter can be eliminated from the IH load by the effect of C_o.

B. Operating Mode Transitions

The voltage and current waveforms of the proposed ac-ac converter for the HFAC cycle are shown in Fig. 7. In addition, the switch-mode transitions and simplified equivalent circuits during the positive and negative half-cycles of v_{in} are depicted in Figs. 8 and 9, respectively. For the sake of paper length restriction, only the positive half-cycle operation with neglecting the L_f-C_f filter is explained below.

[Mode 1: single-loop power supply mode] ($t_0 \le t < t_1$) The low-side switch Q_1 is on-state, and the line current i_{in} flows through the network of v_{in}–L_b–S_1–D_3. During this interval, the boost inductor L_b stores its magnetic energy. At the same time, the HF load resonant current i_o is fed from C_1 to the IH load R_o–L_o until S_1 is turned off at $t = t_1$.

The resonant frequency f_{r1} of the proposed ac-ac converter

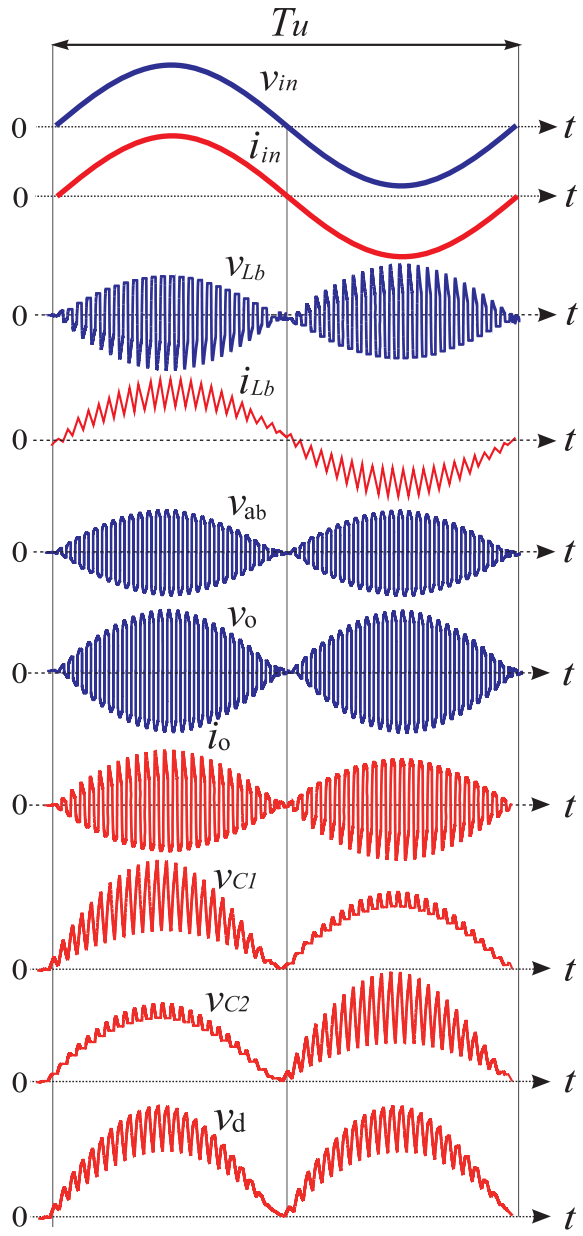


Fig. 4. Relevant voltage and current waveforms for an UFAC cycle.

for the duration of this mode can be defined as

$$f_{r1} = \frac{1}{2\pi\sqrt{L_o C_{r1}}} \tag{2}$$

$$C_{r1} = \frac{C_o C_1}{C_o + C_1} \tag{3}$$

[Mode 2: ZVS commutation mode] ($t_1 \le t < t_2$) The low-side active switch Q_1 is turned off at $t = t_1$, and the lossless snubbing capacitor C_{s1} and equivalent effective inductance L_o make the edge-resonance. Accordingly, C_{s1} is gradually charged and the voltage v_{Q1} across Q_1 rises with a certain slope, while C_{s2} is discharged and the voltage v_{Q2} across Q_2 gradually declines. Thus, ZVS turn-off transition starts in Q_1. It should be noted here that the input inductor current i_{Lb} through L_b also contributes for discharging C_{s1}. Accordingly, in order to successfully attain ZVS, any of the

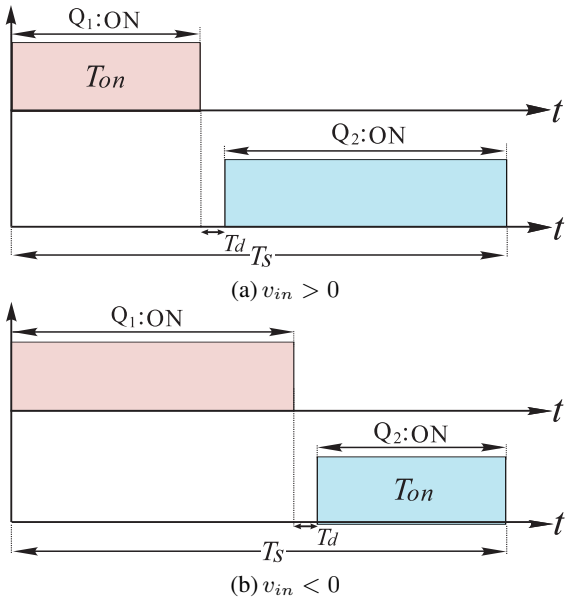


Fig. 5. Asymmetrical PWM gate signal patterns for low- and high-side active switches.

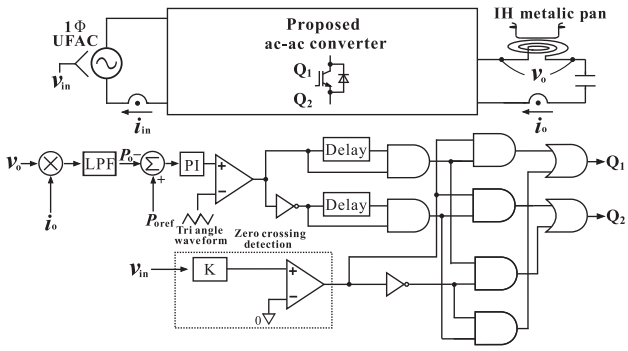


Fig. 6. Schematic controller diagram of logic circuit.

following conditions should be satisfied:

$$\frac{L_o i_o(t_1)^2}{2} > C_s v_d(t_1)^2 \tag{4}$$

$$\Delta t_{mode2} = t_2 - t_1 = C_s \frac{v_d(t_1)}{I_{Lb}} < T_d \tag{5}$$

where the two lossless snubbing capacitors have the same value as $C_s = C_{s1} = C_{s2}$, and I_{Lb} denotes the average value of i_{Lb} for a HFAC cycle.

[Mode 3: high-side free-wheeling mode] ($t_2 \le t < t_3$) The voltage v_{Q1} reaches the NSDC-link voltage v_d at $t = t_2$, then ZVS turn-off of Q_1 is completed. At the same time, the anti-parallel diode D_2 in Q_2 is naturally forward-biased. During this interval, the gate-signal is supplied for S_2 in Q_2, whereby zero voltage and zero current soft-switching (ZVZCS) turn-on can be performed in Q_2. The source current i_{in} is fed to C_1 and C_2 through L_b with releasing the magnetic energy into C_1 and C_2, thus the source voltage v_{in} is boosted in the HF switching cycle. The IH load current i_o gradually decreases due to the series resonance in this sub-mode interval, and reverses its polarity while D_2 keeps conducting. Thereby, a part of the line current i_{in} is supplied into the IH load while charging C_1

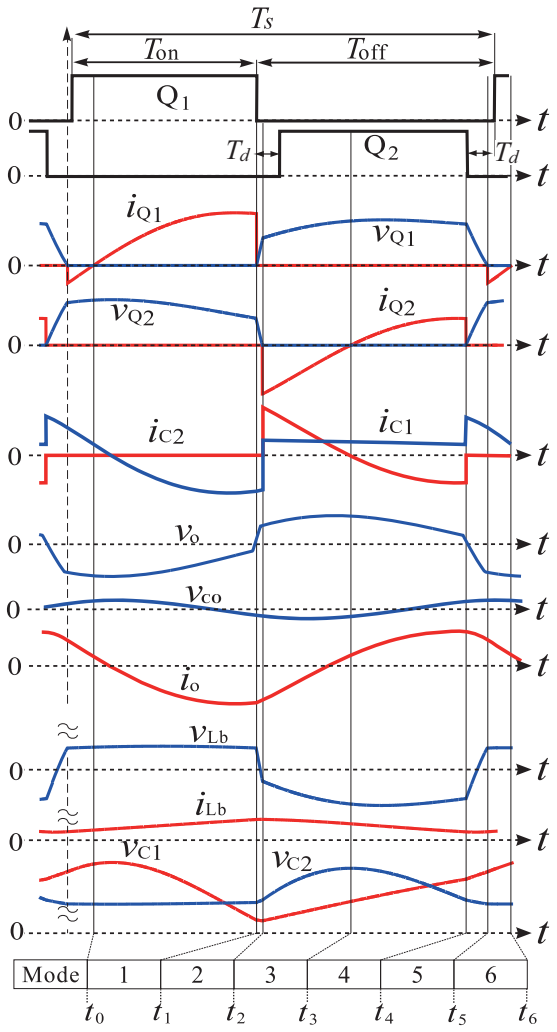


Fig. 7. Relevant voltage and current waveforms for a HFAC cycle ($v_{in} > 0$).

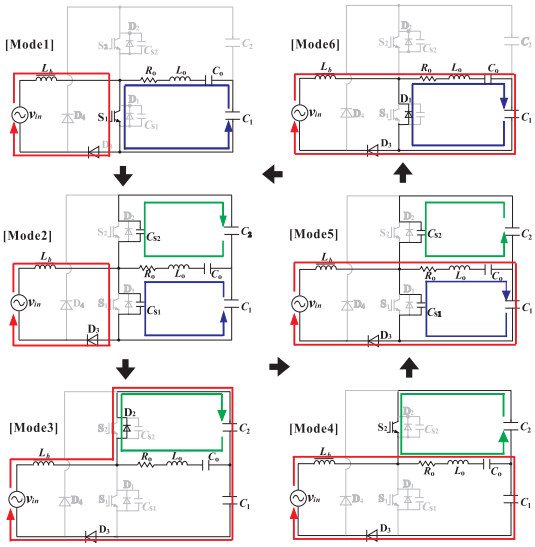


Fig. 8. Mode transitions and equivalent circuits during the positive polarity half-cycle of $v_{\rm in}$.

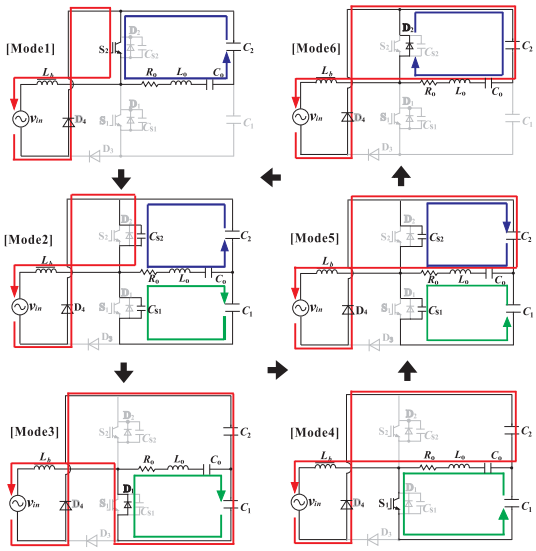


Fig. 9. Mode transitions and equivalent circuits during the negative polarity half-cycle of $v_{\rm in}$.

and C_2 via D_2.

[Mode 4: dual-loop power supply mode] ($t_3 \le t < t_4$) The IH load current i_o commutates naturally from D_2 to S_2 at $t = t_3$. Then, i_o and i_{Q2} rise gradually by the series resonance with L_o, C_o and C_2. During this sub-mode, the load power is supplied from both the UFAC source v_{in} and the high-side NSDC-link capacitor C_2.

The resonant frequency f_{r2} from Mode 3 to Mode 4 can be expressed by

$$f_{r2} = \frac{1}{2\pi\sqrt{L_o C_{r2}}} \tag{6}$$

$$C_{r2} = \frac{C_o C_1}{C_o + C_2} \tag{7}$$

[Mode 5: ZVS commutation mode] ($t_4 \le t < t_5$) The high-side active switch Q_2 is turned off at $t = t_4$, and C_{s1}, C_{s2} and equivalent effective inductor L_o produce the edge-resonance. Accordingly, C_{s2} is gradually discharged and v_{Q2} across Q_2 rises with a certain slope, while C_{s1} is discharged and the voltage v_{Q1} across Q_1 gradually declines. Thus, ZVS turn-off is started in Q_2. In order to attain ZVS successfully, the following condition should be satisfied:

$$\frac{L_o i_o(t_4)^2}{2} > C_s v_d(t_4)^2 \tag{8}$$

[Mode 6: low-side free-wheeling mode] ($t_5 \le t < t_6$) The voltage v_{Q2} reaches the NSDC-link voltage v_d at $t = t_5$, then ZVS turn-off operation of Q_2 is completed. At the same time, the anti-parallel diode D_1 in Q_1 is naturally forward-biased. During this interval, the gate-signal is provided for S_1 in Q_1, whereby ZVZCS turn-on is achieved in Q_1. The source current i_{in} is fed to the IH load through L_b with charging C_1. The current i_{Q1} through Q_1 commutates from D_1 to S_1 at $t = t_6$, then the circuit state is initiated into Mode 1 mentioned above.

The conduction power devices for the positive and negative half cycles of v_{in} are compared between the DBR-BHB and proposed bridgeless BHB ac-ac converters in TABLE I. The

TABLE I. COMPARISON OF CONDUCTING POWER DEVICES.

$v_{in} > 0$		
Duty cycle-controlled switch	DBR-BHB (Fig. 2)	Proposed bridgeless BHB (Fig. 3)
ON	Q_1, D_3, D_6	Q_1, D_3
OFF	Q_2, D_3, D_6	Q_2, D_3

$v_{in} < 0$		
Duty cycle-controlled switch*	DBR-BHB (Fig. 2)	Proposed bridgeless BHB (Fig. 3)
ON	Q_1*, D_4, D_5	Q_2, D_4
OFF	Q_2*, D_4, D_5	Q_1, D_4

*Duty cycle-controlled switch: Q_1 in DBR-BHB

TABLE II. COMPARISON OF VOLTAGE STRESSES OF POWER DEVICES.

Power devices	DBR-BHB (Fig. 2)	Proposed bridgeless BHB (Fig. 3)
Q_1, Q_2	$v_{d,peak}$	$v_{d,peak}$
D_3, D_4	$v_{in,peak}$	$v_{d,peak}$

number of conduction power devices of the bridgeless BHB circuit is reduced by one as compared to the DBR-BHB topology, which is advantageous for improving the power conversion efficiency.

The voltage stress across each power device is summarized in TABLE II. The bridgeless rectifying diodes require a higher voltage rating than the DBR. As measures to avoid increase of conduction power losses, a wide band gap power device such as Shottky barrier diode (SiC-SBD) can be effectively used for D_3 and D_4 in the proposed ac-ac converter.

III. ZVS PERFORMANCES WITH INSTANTANEOUS SOURCE VOLTAGE LEVEL

ZVS operations of the active switches Q_1 and Q_2 depend on the source voltage level v_{in} as well as the IH load current i_o in the proposed ac-ac converter. Since the NSDC-link voltage v_d fluctuates in twice the UFAC frequency, ZVS operations vary every moment during the UFAC cycle in the proposed ac-ac converter. Hence, there should be defined ZVS and non-complete (semi-ZVS) areas with respect to a HFAC cycle in the proposed ac-ac converter.

By assuming the source voltage as a constant value; $v_{in}(t) \simeq V_{in}$ for the HFAC cycle, the NSDC-link voltage v_d which is determined by the duty cycle D of active switches can be expressed for the HFAC cycle as

$$v_d = \frac{V_{in}}{1-D} + \frac{\Delta v_{d,HF}}{2} \tag{9}$$

where $\Delta v_{d,HF}$ denotes the ripple of the NSDC-link voltage v_d for the HFAC cycle due to the series resonance.

The non-complete ZVS operation named here as "semi-ZVS" causes the residual voltage that appears in the end of the commutation interval due to not fulfilling (4) and (8), as illustrated in Fig. 10. In particular, the turn-off of duty cycle-uncontrolled switch (Q_2 for $v_{in} > 0$, Q_1 for $v_{in} < 0$) is more susceptible for the semi-ZVS than that of the duty cycle-controlled switch (Q_1 for $v_{in} > 0$, Q_2 for $v_{in} < 0$) which is assisted with the input inductor current i_{Lb} as expressed by (5). Referring to Fig. 10, the residual voltage $v_{Cs,res}$ of

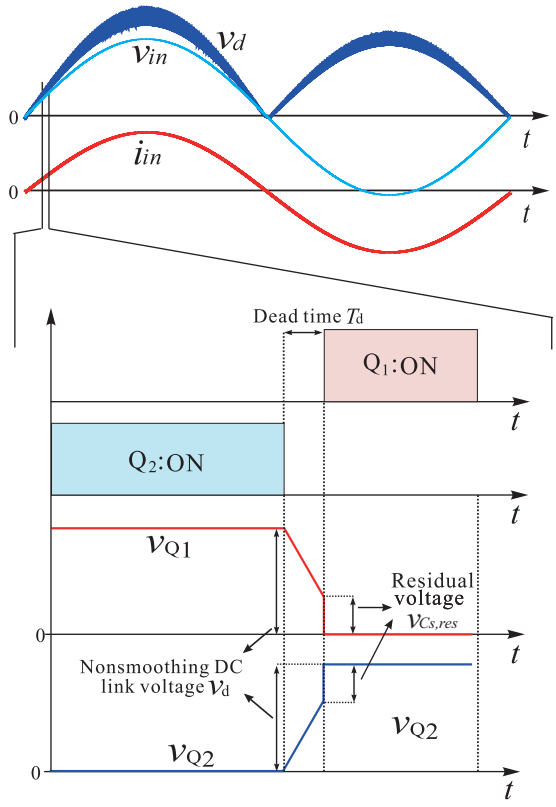


Fig. 10. Residual voltages of lossless snubbing capacitors for a HFAC cycle.

lossless snubbing capacitor in the the duty cycle-uncontrolled switch can be expressed from the energy balance between the IH load equivalent inductance and lossless snubbing capacitor capacitors as

$$v_{Cs,res} = v_d - \frac{I_{L_o,off}}{C_s} \cdot T_d > 0 \tag{10}$$

where $I_{L_o,off}$ is identical with $i_o(t_4)$ in (8). In contrast to the semi-ZVS, the "complete ZVS" behavior can be defined as $v_{Cs,res} = 0$. Fig.11 exhibits the characteristics of $v_{Cs,res}$ which is calculated by simulation based on the relevant conditional equations (4), (8) and (9) in $v_{in} > 0$. It can be understood from the characteristics that the switching transition is partly out of the complete ZVS in accordance with the source voltage level as well as the load power setting, i.e. duty cycle.

Small amounts of capacitive energies stored in C_{s1} and C_{s2} are forced to discharge in the semi-ZVS conditions. However, the power loss due to the discharging of stored capacitive energy is not outstanding since the lossless capacitors C_{s1} and C_{s2} are small so as to produce the edge resonance during the dead time interval, and the switching frequency f_s is limited in the range of several tens of kHz with IGBTs. Moreover, the residual voltage varies in accordance with the level of v_{in}, consequently the power loss is relatively a low profile in the UFAC cycle.

In contrast to a hard-switching operation, no significant voltage occurs at the turn-off transitions of the active switches by the effect of C_{s1}, C_{s2} even for the semi-ZVS behavior.

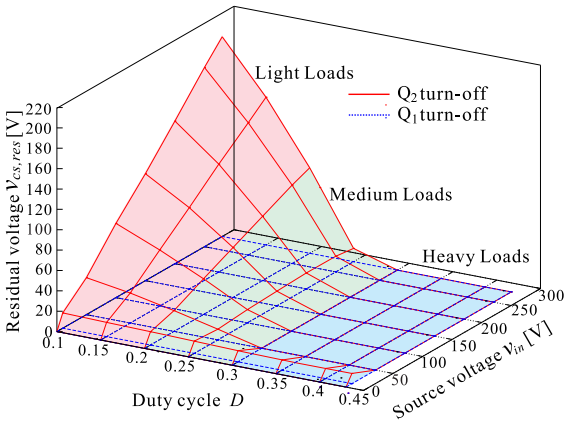


Fig. 11. Residual voltage characteristics with the instantaneous source voltage and duty cycle for a HFAC cycle in $v_{in} > 0$.

Accordingly, conducted emission which has more relevance with a dv/dt rate of switch can be kept at a low level in the whole power range of the proposed ac-ac converter. The radiated emission that is concerned with a di/dt rate could be influenced slightly by the turn-on transition in the zemi-ZVS, but limited for the operating condition around the peak level of v_{in}.

IV. Design Guideline of Circuit Parameters

A. Lossless Snubbing Capacitors

The lossless snubbing capacitors C_{s1} and C_{s2} should be designed by taking the ZVS range into account as discussed in Section III. The residual voltage $v_{Cs,res}$ varies in accordance with the source voltage level as well as the duty cycle, i.e. output power as indicated by Fig. 11. The maximum turn-off switching current $I^*_{L_o,off}$ with D_{max} can be determined with the peak value $v_{d,peak}$ of the NSDC-link voltage in accordance with (10) as

$$I^*_{L_o,off} \simeq \frac{2v_{d,peak}}{\pi Z_o} \tag{11}$$

$$Z_o = \sqrt{{R_o}^2 + \left(\omega_h L_o - \frac{1}{\omega_h C_o}\right)^2} \tag{12}$$

where $\omega_h\,(=\ 2\pi f_s)$ represents the angular frequency of HFAC (switching frequency). By assuming the load factor k where the complete ZVS operation can maintain, the capacitance $C_s\,(= C_{s1} = C_{s2})$ can be determined by

$$C_s = \frac{kI^*_{L_o,off}}{v_{d,peak}} \cdot T_d. \tag{13}$$

B. NSDC-Link and Load Series-Resonant Capacitors

The two resonant frequencies f_{r1} in (2) and f_{r2} in (6) should be identical with the load series-resonant frequency f_r for obtaining a low-distorted IH load current in the proposed ac-ac converter. Accordingly, the two NSDC-link capacitors C_1, C_2 are designed to the same value, thereby f_r is expressed as

$$f_r = f_{r1} = f_{r2} = \frac{1}{2\pi\sqrt{L_o C_r}} \tag{14}$$

$$C_r = C_{r1} = C_{r2}. \tag{15}$$

The load series-resonant capacitor C_o is tuned so that the switching frequency f_s is greater than f_r in order to guarantee the ZVS operations in Q_1 and Q_2. In addition, C_o is relevant with the quality factor Q of the load series-resonant tank which is expressed as

$$Q = \frac{\omega_r L_o}{R_o} = \frac{R_o}{\omega_r C_r} \tag{16}$$

where $\omega_r\,(=\ 2\pi f_r)$ represents the angular frequency of the series resonance. It should be considered that the voltage stresses across the IH working coil and C_o rise in proportion to Q due to the series resonant principle, which might lead to increase of voltage stress in Q_1 and Q_2. Therefore, setting the value of Q in accordance with the IH load parameters and Q can yield the effective parameter of C_o under the condition of $f_s > f_r$.

Selection of the NSDC-link capacitors C_1, C_2 has great relevance with the PFC operation as well as the load series-resonant frequency f_r defined in (14). In order to achieve the PFC operation based on A-PWM scheme, C_1, C_2 should be small enough to include the frequency component of two times as high as the utility frequency in v_d with low distortion of the line current i_{in}.

C. Boost Inductor

The boost inductor current i_{Lb} is regulated by A-PWM under the condition of continuous conduction mode (CCM). Given $i_{Lb} = I_{Lb,peak}$ at $t = t_1$ with the time origin $t_0 = 0$ in Fig. 7, the boost inductor current can be defined under the ideal condition for the HFAC cycle as

$$i_{Lb}(t) = -\frac{\overline{v_d} - V_{in}}{L_b}(t - DT_s) + I_{Lb,peak}. \tag{17}$$

The CCM constraint in i_{Lb} for a wide-range operating conditions leads to the condition as $i_{Lb}(T_s) > 0$. Accordingly, the boost inductor L_b is expressed from (17) as

$$L_b > \frac{\overline{v_d} - V_{in}}{I_{Lb,peak}}(1 - D)T_s \tag{18}$$

where $\overline{v_d}$ represents the average value of the NSDC-link voltage for a HFAC cycle and is expressed from (9) as

$$\overline{v_d} = \frac{V_{in}}{1 - D}. \tag{19}$$

Considering the current ripple ΔI_{Lb}, the peak value $I_{Lb,peak}$ is defined by

$$I_{Lb,peak} = I_{Lb} + \frac{\Delta I_{Lb}}{2}. \tag{20}$$

By using the ripple factor $\gamma = \Delta I_{Lb}/I_{Lb}$, L_b in (18) can be described by (19) and (20) by

$$L_b > \frac{DT_s\left(V_{in}/I_{Lb}\right)}{1 + \left(\gamma/2\right)} = \frac{DT_s Z_{in}}{1 + \left(\gamma/2\right)} \tag{21}$$

where Z_{in} represents the input impedance under the condition of unity power factor. By setting the maximum duty cycle D_{max} and minimum ripple factor γ_{min} in conjunction with the maximum (rated) IH load power, i.e. minimum input

impedance $Z_{in,min}$, the maximum inductance $L_{b,max}$ can be specified from (21) as

$$L_{b,max} = \frac{D_{max} T_s Z_{in,min}}{1 + (\gamma_{max}/2)}. \tag{22}$$

In contrast to that, by setting the minimum duty cycle D_{min} and maximum ripple factor γ_{max} in conjunction with the minimum IH load power, i.e. maximum input impedance $Z_{in,max}$, the minimum inductance $L_{b,max}$ can also be obtained from (21) as

$$L_{b,min} = \frac{D_{min} T_s Z_{in,max}}{1 + (\gamma_{max}/2)}. \tag{23}$$

Thus, the input inductor L_b can be determined in the range from $L_{b,min}$ to $L_{b,max}$ together with consideration for size and volume as well as the implementation cost.

V. Experimental Results and Evaluations

A. Experimental Set-Up and Specification

The practical feasibility of the proposed ac-ac converter is investigated in an experiment using a 3.0 kW-30 kHz laboratory prototype.

The exterior appearance of the prototype assembly is indicated in Fig. 12. The specification of the laboratory prototype and the experimental conditions are indicated in TABLE III. The circuit parameters are designed in accordance with the procedure described in Section IV by setting the variable ranges of key parameters: duty cycle $0.1 \le D \le 0.45$, complete ZVS achievable load factor $0.5 \le k \le 1$, ripple factor of input inductor current $0.5 \le \gamma < 2$, input impedance $13 \le Z_{in} \le 133$, and quality factor of load resonant tank $Q = 20$ at the rated output power, respectively. In this experiment, a stainless utensil (SUS 430) is used for the IH load, and the high frequency resonant current is supplied with LITZ wires through an insulator of acrylic plate.

The theoretical voltage stresses across the two active switches Q_1 and Q_2 are equal to $v_{d,peak}$ as displayed in TABLE II. Given the amplitude of the source voltage 282 V, the maximum duty cycle (D_{max}) 0.45 and the HF voltage ripple ($\Delta v_{d,HF}$) 200 V, the NSDC-link peak voltage $v_{d,peak}$ is estimated over 600 V. Accordingly, the power devices of 800 V and more voltage rating are should be selected for the active switches and diodes. As an example for assembling the prototype, a high-speed IGBT two-in-one module CM100DU-24NFH (1200 V, 100 A) suitable for IH applications is selected for the active switches Q_1, Q_2 while the bridgeless rectifying diodes D_1 and D_2 are configured by Si-fast recovery diodes (FRDs) STTH6012 (1200 V, 60 A) .

The actual power conversion efficiency η of the prototype circuit is obtained by measuring the average input and load powers P_{in}, P_o with a precision power analyzer (WT1800). It can be described under the condition of PFC as

$$\eta = \frac{P_o}{P_{in}} = \frac{\overline{v_o i_o}}{\overline{v_{in} i_{in}}} \tag{24}$$

$$P_{in} = V_{in,rms} I_{in,rms} \cos\phi_{in} \simeq V_{in,rms} I_{in,rms} \tag{25}$$

$$P_o = V_{o,rms} I_{o,rms} \cos\phi_o \tag{26}$$

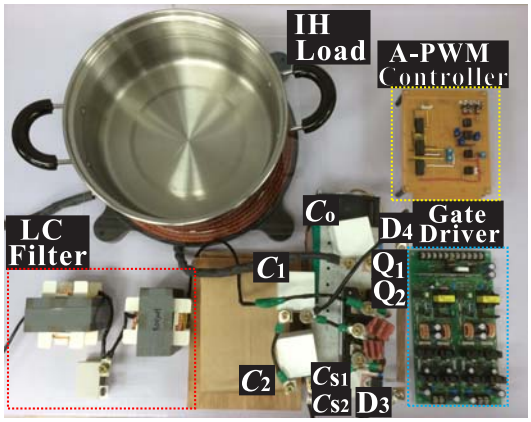


Fig. 12. Experimental setup of the proposed ac-ac converter prototype.

TABLE III. Circuit Parameters and Specifications of Prototype.

Item	Symbol	Value [unit]
Input source voltage(rms)	$v_{\rm in}$	200 [V]
Low-pass filter inductor	L_f	200 [μH]
Low-pass filter capacitor	C_f	750 [nF]
Cut-off frequency of low-pass filter	f_c	51 [kHz]
Input boost inductor	L_b	500 [μH]
Utility frequency	f_u	60 [Hz]
Switching frequency	f_s	30 [kHz]
Series resonant frequency	f_r	19 [kHz]
Dead time interval	T_d	2 [μs]
Lossless snubbing capacitors	C_{s1},C_{s2}	80 [nF]
Non-smoothed dc-link film capacitors	C_1,C_2	2 [μF]
Series resonant capacitor	C_o	2 [μF]
IH load equivalent resistance	R_o	4.7 [Ω]
IH load equivalent inductance	L_o	35 [μH]
IGBTs Q_1,Q_2 : CM100DU-24NFH (1200V,100A)		
Bridgeless diode rectifier D_1,D_2: STTH6012 (1200 V, 60 A)		

where

$$v_o(t) = v_o(2\omega_u t) + \sum_{n=1,3,5,\ldots}^{\infty} v_o(n\omega_h t)$$
$$= \sqrt{2}\Big\{ V_{ou} \sin 2\omega_u t + \sum_{n=1,3,5,\ldots}^{\infty} V_{noh} \sin(n\omega_h t) \Big\} \tag{27}$$

$$V_{o,rms} = \sqrt{{V_{ou}}^2 + \sum_{n=1,3,5,\ldots}^{\infty} {V_{noh}}^2} \tag{28}$$

$$i_o(t) = i_o(2\omega_u t) + \sum_{n=1,3,5,\ldots}^{\infty} i_o(n\omega_h t)$$
$$= \sqrt{2}\Big\{ I_{ou} \sin(2\omega_u t - \phi_{ou}) + \sum_{n=1,3,5,\ldots}^{\infty} I_{noh} \sin(n\omega_h t - \phi_{noh}) \Big\} \tag{29}$$

$$I_{o,rms} = \sqrt{{I_{ou}}^2 + \sum_{n=1,3,5,\ldots}^{\infty} {I_{noh}}^2} \tag{30}$$

$$\cos\phi_o = \frac{\overline{v_o i_o}}{V_{o,rms} I_{o,rms}} = \frac{V_{ou} I_{ou} \cos\phi_{ou} + \sum_{n=1,3,5,\ldots}^{\infty} V_{noh} I_{noh} \cos\phi_{noh}}{V_{o,rms} I_{o,rms}}, \quad (31)$$

where ϕ_{ou} and ϕ_{noh} denote the phase angles between output voltage and current of the UFAC and HFAC components, respectively. It should also be noted here that $\omega_u\,(=2\pi f_u)$ represents the angular frequency of UFAC, and n denotes the harmonics order relevant to HFAC. Power losses of the input low-pass filter L_f-C_f are also took into account for the efficiency evaluation.

B. Switching Performances

The voltage and current waveforms of active switches for a HFAC cycle under the rated and light load settings are depicted in Fig. 13. In addition, the corresponding voltage-current trajectories are displayed in Fig. 14. ZVZCS turn-on and ZVS turn-off operations can be actually confirmed in those measured results.

ZVS operations, especially for the duty cycle-controlled switch (Q_1 for $v_{in} > 0$, and Q_2 for $v_{in} < 0$) significantly depend on the source voltage v_{in} as well as the load power P_o as discussed in Section III. The enlarged waveforms of the turn-on and turn-off transitions of Q_1 and Q_2 are depicted in Fig. 15 for $P_o = 3.0\,\text{kW}$ and Fig. 16 for $P_o = 1.0\,\text{kW}$, respectively. The semi-ZVS operation is portrayed in Fig. 16 (a), however no surge current generates and the switching power loss is considered to be far less than that of a typical hard switching circuit.

C. Steady-State Characteristics

The observed UFAC-cycle converter waveforms including the NSDC-link and its capacitors voltages are demonstrated in Fig. 17. The UFAC-HFAC power conversion, HF load power regulation, and boost operation in the NSDC-link voltage are actually verified.

The measured characteristics of the NSDC-link voltage v_d versus the duty cycle D are shown in Fig. 18 in terms of its peak value. It can be confirmed from those results that the inductor-assisted boost operation can be attained for the HFAC cycle according to D in the proposed ac-ac converter. Thus, the effectiveness of the BHB circuit in the bridgeless topology is verified herein.

The output power versus duty cycle characteristics are presented in Fig. 19. It can be verified from the measured curve that the A-PWM scheme is effective for the HF output power regulation in the proposed ac-ac converter. The complete ZVS operation can be accomplished in the duty cycle-controlled switch (Q_1 for $v_{in} > 0$, and Q_2 for $v_{in} < 0$) in the whole output power range. For the duty cycle-uncontrolled switch (Q_2 for $v_{in} > 0$, and Q_1 for $v_{in} < 0$), the complete ZVS can be achieved in the output power range from $3.0\,\text{kW}$ ($100\,\%$ load setting) to $1.4\,\text{kW}$ ($47\,\%$ load setting), while the semi-ZVS emerges in accordance with the source voltage level v_{in} in the output power range from $1.4\,\text{kW}$ to $0.1\,\text{kW}$ ($3\,\%$ load setting).

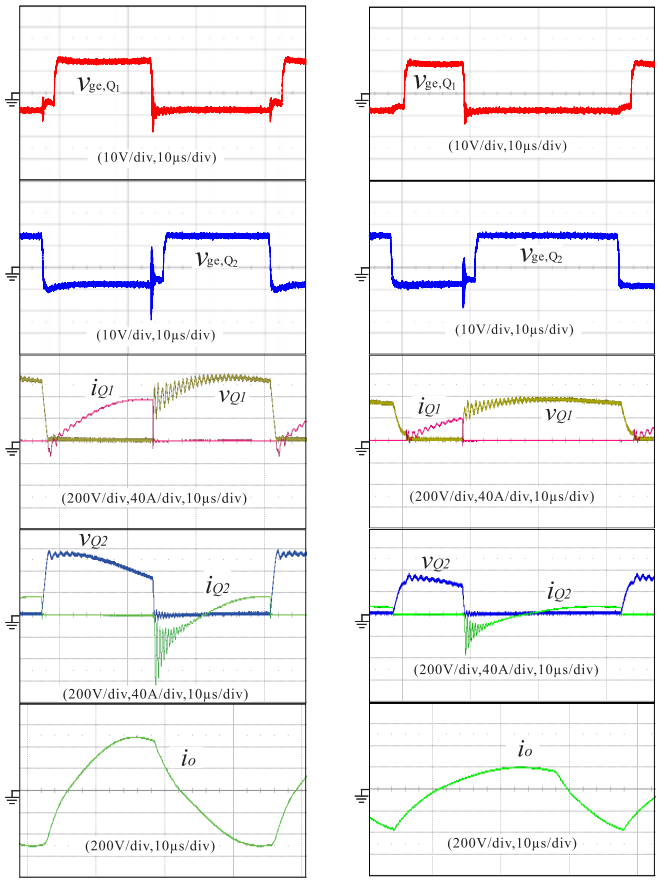


Fig. 13. Observed voltage and current waveforms of active switches Q_1, Q_2 with gate-emitter signals, and IH load for a switching cycle ($v_{in} = 282\,\text{V}$): (a) $P_o = 3.0\,\text{kW}$, $D = 0.43$, and (b) $P_o = 1.0\,\text{kW}$, $D = 0.25$.

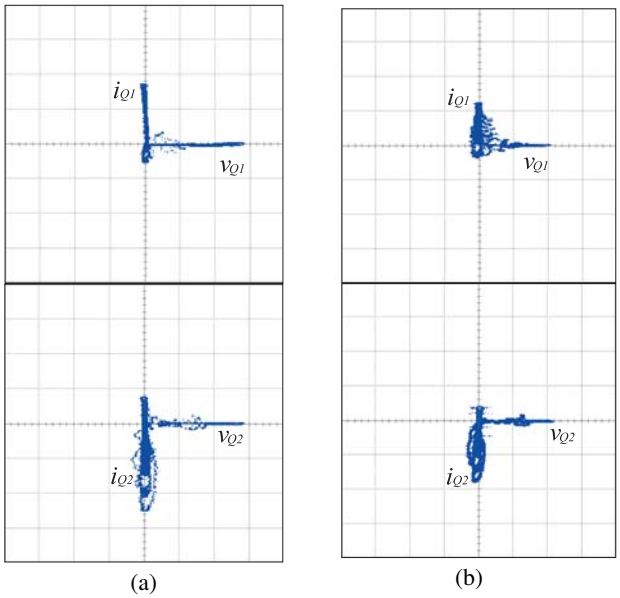


Fig. 14. Voltage and current trajectories of Q_1 and Q_2 for a HFAC cycle ($v_{in} = 282\,\text{V}$): (a) $P_o = 3.0\,\text{kW}$ (v_{Q1}, v_{Q2}: $200\,\text{V/div}$, i_{Q1}, i_{Q2}: $40\,\text{A/div}$), (b) $P_o = 1.0\,\text{kW}$ (v_{Q1}, v_{Q2}: $200\,\text{V/div}$, i_{Q1}, i_{Q2}: $20\,\text{A/div}$).

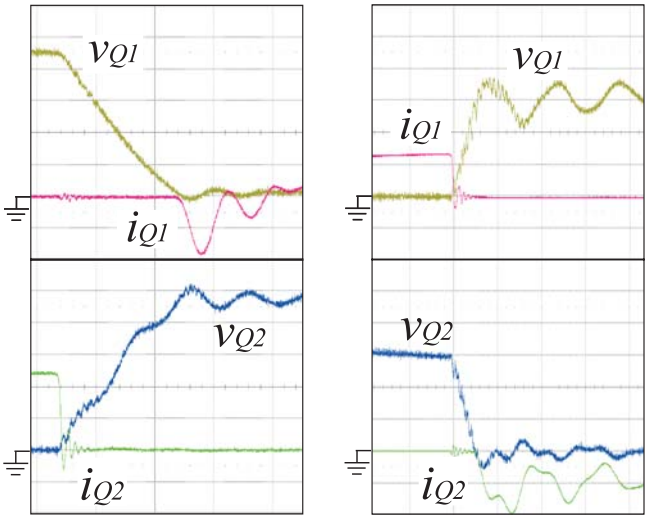


Fig. 15. Enlarged switching waveforms at $P_o = 3.0\,\mathrm{kW}$ ($v_{in} = 282\,\mathrm{V}$): (a) Q_1 turn-on with Q_2 turn-off (v_{Q1}, v_{Q2}: $100\,\mathrm{V/div}$, i_{Q1},i_{Q2}: $10\,\mathrm{A/div}$, $500\,\mathrm{ns/div}$), and (b) Q_1 turn-off and Q_2 turn-on (v_{Q1}, v_{Q2}: $100\,\mathrm{V/div}$, i_{Q1}, i_{Q2}: $50\,\mathrm{A/div}$, $500\,\mathrm{ns/div}$).

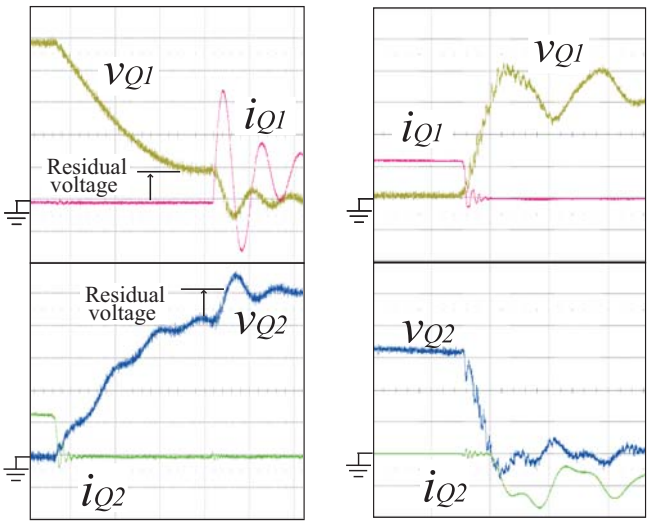


Fig. 16. Enlarged switching waveforms at $P_o = 1.0\,\mathrm{kW}$ ($v_{in} = 282\,\mathrm{V}$): (a) Q_1 turn-on with Q_2 turn-off (v_{Q1}, v_{Q2}: $100\,\mathrm{V/div}$, i_{Q1}, i_{Q2}: $10\,\mathrm{A/div}$, $500\,\mathrm{ns/div}$), and (b) Q_1 turn-off and Q_2 turn-on (v_{Q1}, v_{Q2}: $100\,\mathrm{V/div}$, i_{Q1}, i_{Q2}: $35\,\mathrm{A/div}$, $500\,\mathrm{ns/div}$).

The actual power conversion efficiency characteristics of the proposed ac-ac converter are depicted in Fig. 20 in comparison with the DBR-BHB prototype using 600 V Si-FRDs (DSE 2x 31-06C) for D_5–D_6 in Fig. 2. The high efficiency can be attained in the proposed ac-ac converter over the wide power range owing to keeping the wide-range ZVS commutation. The maximum efficiency $95.2\,\%$ attains at $P_o = 2.0\,\mathrm{kW}$ in the proposed prototype. Furthermore, the efficiency of the proposed ac-ac converter exceeds even with the 1200 V Si-FRDs for the bridgeless diode rectifiers that of DBR-BHB type with the 600 V Si-FRDs for the full-bridge rectifier in the whole output power range. Thus, the advantageous property of the proposed ac-ac converter featuring the bridgeless BHB

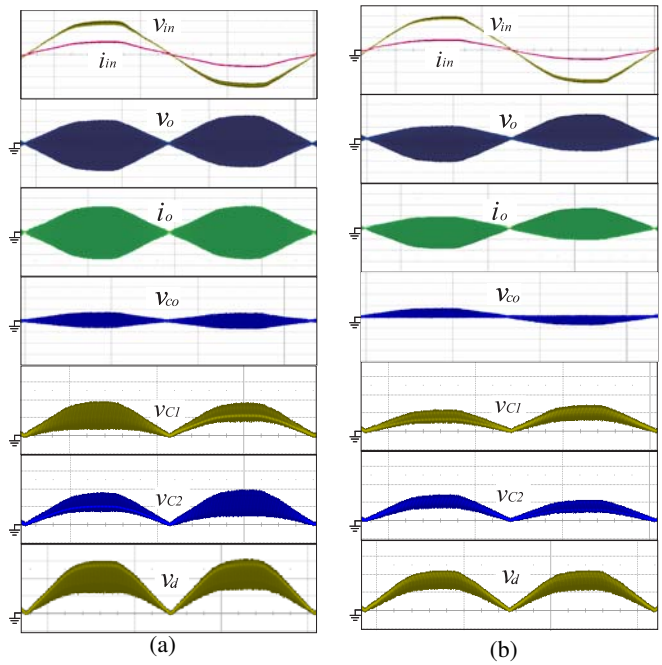


Fig. 17. Observed steady-state waveforms in an UFAC cycle ($200\,\mathrm{V/div}$, $20\,\mathrm{A/div}$, and $5.0\mathrm{ms/div}$): (a) $P_o = 3.0\,\mathrm{kW}$, and (b) $P_o = 1.0\,\mathrm{kW}$.

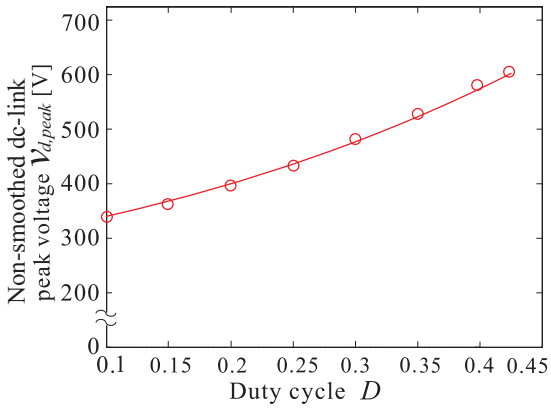


Fig. 18. Measured characteristics of the NSDC-link peak voltage $v_{d,peak}$ versus duty cycle.

topology is actually demonstrated.

The power losses of the power devices and passive components are measured for the HFAC cycle in accordance with the output powers and input voltage levels. The power loss breakdowns are presented in Fig. 21 under the condition of $v_{in} > 0$. It can be understood from the experimental result that the conduction power loss in the duty cycle-controlled switch (Q_1) constitutes a large part of the total value especially for the rated output power ($3.0\,\mathrm{kW}$). This is due to the sub-mode interval where the conduction current of Q_1 is a sum of the boost inductor current i_{Lb} and IH load current i_o with a relatively large duty cycle. On the other hand, the conduction power loss in the duty cycle-uncontrolled switch (Q_2) exhibits high profile for the low output power settings ($1.0\,\mathrm{kW}$ and $0.3\,\mathrm{kW}$) with the smaller duty cycle in Q_1.

The switching power losses of all the power devices

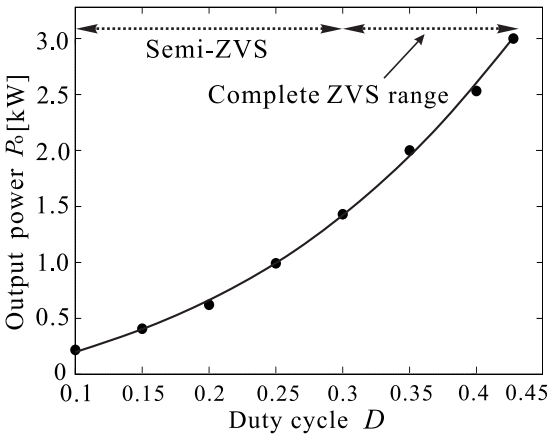


Fig. 19. Experimental characteristics of output power versus duty cycle.

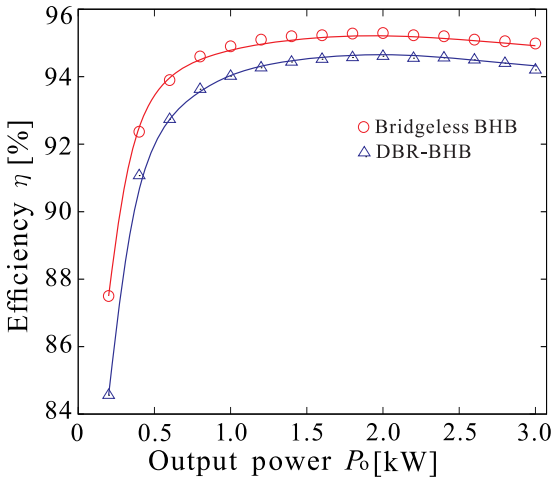


Fig. 20. Actual efficiency versus output power curves.

are well mitigated as compared to conduction power losses by the effect of ZVS. The turn-on power loss of the duty cycle-controlled switch Q_1 which is caused by the semi-ZVS operation appears for the condition of $P_o = 0.3\,\mathrm{kW}$ as well as $P_o = 1.0\,\mathrm{kW}$, however it shares the smaller part of the breakdowns as compared to the other conduction power losses in the prototype.

D. Harmonics Analysis of UFAC Line Current

The observed UFAC source voltage and current waveforms are provided in Fig. 22, where high power factor 0.98–0.99 can be confirmed by Fourier transformation with the power analyzer.

The UFAC line current harmonics analysis corresponding to Fig. 22 is depicted in Fig. 23, where the measured values are compared with the standards of IEC61000-3-2-Class A. It can be confirmed from the results that the measured harmonics are well lower than the regulation values at all the orders regardless of the output power conditions. Thus, effectiveness of the bridgeless BHB topology on the PFC and low distortion utility current is actually proven in the experiment.

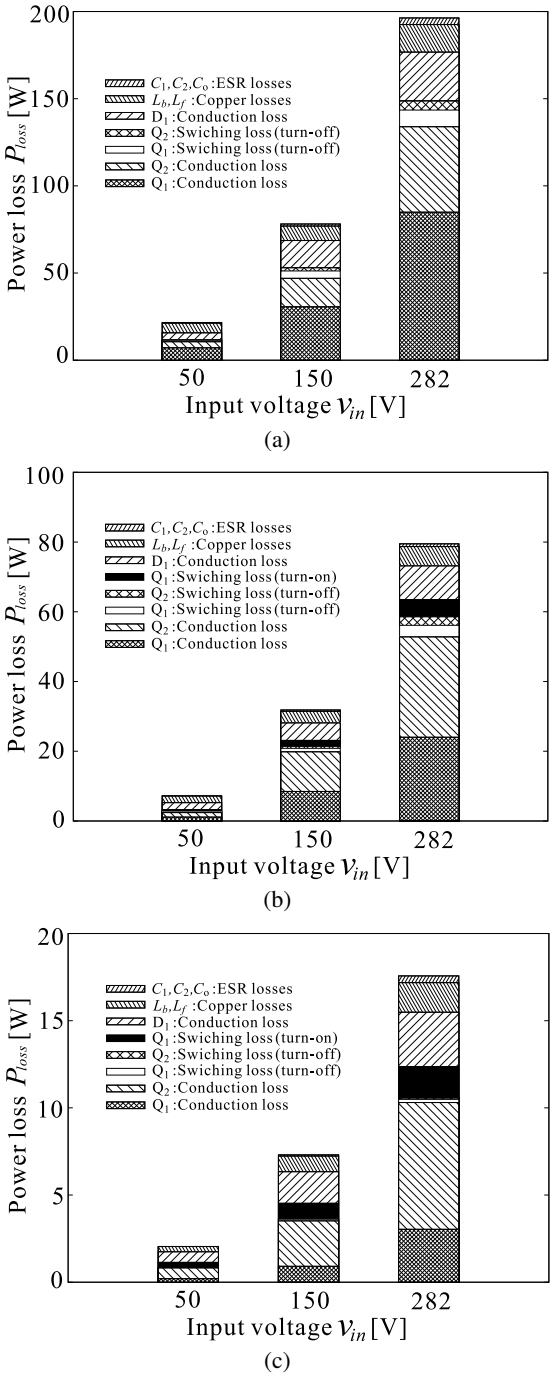
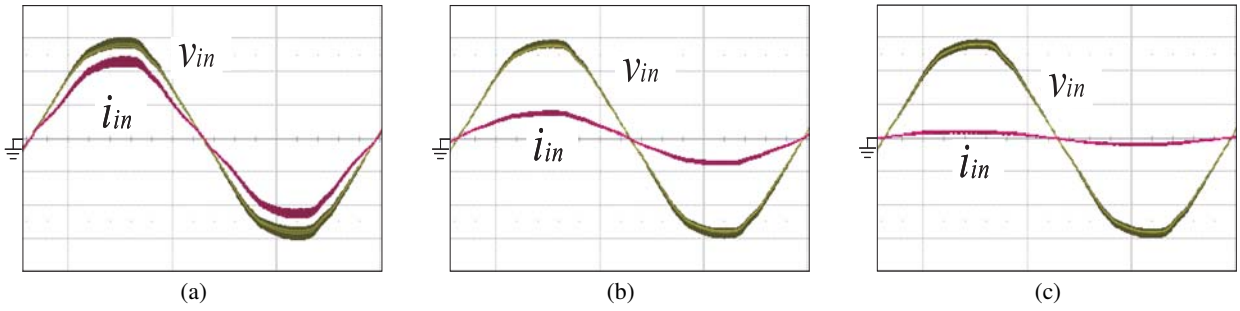


Fig. 21. Power loss analysis of the proposed ac-ac converter prototype: (a) $P_o = 3.0\,\mathrm{kW}$, (b) $P_o = 1.0\,\mathrm{kW}$, and (c) $P_o = 0.3\,\mathrm{kW}$.

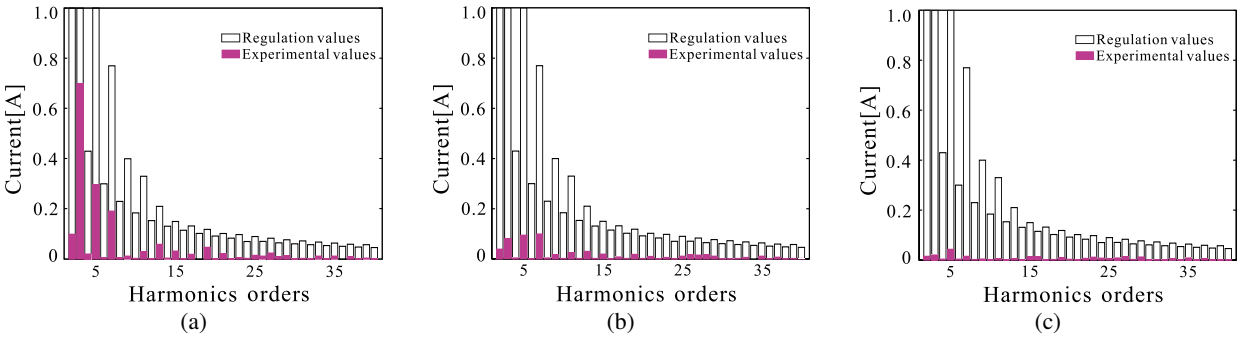
VI. Conclusion

The practical effectiveness of the newly proposed ZVS-PWM UFAC–HFAC converter has been demonstrated in this paper. The operation principle of single-stage ac-ac conversion with voltage boost and PFC operations by BHB has been explained in details, and ZVS characteristics have been described. The design methodology of circuit parameters has been presented by taking the wide-range of ZVS and NSDC-link assisted PFC operations into account. The BHB-based



(a) (b) (c)

Fig. 22. Voltage and current waveforms of the utility power source: (a) $P_o = 3.0\,\mathrm{kW}$, (b) $P_o = 1.0\,\mathrm{kW}$, and (c) $P_o = 0.2\,\mathrm{kW}$ ($100\,\mathrm{V/div}$, $10\,\mathrm{A/div}$, $5.0\,\mathrm{ms/div}$).



(a) (b) (c)

Fig. 23. Harmonics analysis of UFAC line current i_{in}: (a) $P_o = 3.0\,\mathrm{kW}$, (b) $P_o = 1.0\,\mathrm{kW}$, and (c) $P_o = 0.2\,\mathrm{kW}$.

PFC and the NSDC–HFAC resonant inverter operations with ZVS have been verified as summarized below:

- A wide range of output power regulation ($0.1\,\mathrm{kW}$–$3.0\,\mathrm{kW}$) can be achieved by the asymmetrical PWM scheme.
- PFC and low harmonics in the UFAC line current can be attained, which clears the relevant industrial standard.
- The UFAC source voltage is effectively lifted in the NSDC-link voltage with the aid of the inductor-type BHB circuit.
- The high-efficiency power over $94\,\%$ conversion with the complete and semi-ZVS operations can be realized over the wide-rage output power setting of $0.6\,\mathrm{kW}$–$3.0\,\mathrm{kW}$ ($20\,\%$–$100\,\%$ load settings).

The advantageous properties of the proposed ac-ac converter over the diode bridge rectifier-based BHB UFAC-HFAC converter have also been clarified by comparison of the actual power conversion efficiency. The efficiency improvement due to the bridgeless BHB circuit topology with the NSDC-link has been confirmed in the experiment, then the validity of the proposed ac-ac converter for IH applications has been proven in this paper.

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