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***Abstract*—An LLC resonant circuit-based full-bridge dc-dc converter with an LC anti-resonant tank for improving the performance of pulse-frequency-modulation (PFM) is proposed in this paper. The proposed resonant dc-dc converter, named as LLC-LC converter can extend a voltage regulation area below the unity gain with a smaller frequency variation of PFM by the effect of the anti-resonant tank. This advantageous property contributes for protecting over-current in the case of the short-circuit load condition as well as the start-up interval in the designed band of switching frequency. The circuit topology and operating principle of the proposed converter is described, after which the design procedure of the operating frequency and circuit parameters is presented. The performances on the soft switching and the steady-state PFM characteristics of the LLC-LC converter are evaluated under the open-loop control in experiment of a $2.5\,\mathrm{kW}$ prototype, and its actual efficiency is compared with a LLC converter prototype. For revealing the effectiveness of the LLC-LC resonant circuitry, voltages and currents of the series and anti-resonant tanks are analyzed respectively with state-plane trajectories based on calculation and experiment, whereby the power and energy of each resonant tank are demonstrated. Finally, the feasibility of the proposed converter is evaluated from the practical point of view.**

Keywords– LLC resonant converter, anti-resonant tank, LLC-LC resonant converter, pulse frequency modulation (PFM), over-current protection (OCP), buck and boost voltage regulations, zero voltage soft-switching (ZVS), zero current soft-switching (ZCS).

Nomenclature

f_s : Switching frequency
ω_s : Angular switching frequency ($\omega_s = 2\pi f_s$)
M : Input / output voltage conversion ratio ($M = V_o/V_{in}$)
a : High-frequency transformer windings turns ratio ($a = N_1/N_2$)
f_{rs} : Series resonant frequency ($f_{rs} = 1/(2\pi\sqrt{L_sC_s})$)
f_{rm}: LLC resonant frequency ($f_{rm} = 1/(2\pi\sqrt{(L_s+L_m)C_s})$)
F_{rs}: Switching frequency normalized to series resonant frequency ($F_{rs} = f_s/f_{rs}$)
F_{rm}: Switching frequency normalized to LLC resonant frequency ($F_{rm} = f_s/f_{rm}$)
f_{r1} : First resonant frequency of LLC-LC resonant converter (referred to (4))
f_{r2} : Second resonant frequency of LLC-LC resonant converter (referred to (5))
f_{rp} : Anti-resonant frequency ($f_{rp} = 1/(2\pi\sqrt{L_pC_p})$)
F_{rp}: Switching frequency normalized to anti-resonant frequency ($F_{rp} = f_s/f_{rp}$)
S : LLC resonant-tank inductors ratio ($S = L_m/L_s$)
γ_L : Series / anti-resonant inductors ratio ($\gamma_L = L_s/L_p$)
γ_C : Series / anti- resonant capacitors ratio ($\gamma_C = C_s/C_p$)
R_{ac}: AC equivalent load resistance ($R_{ac} = 8a^2R_o/\pi^2$)
Z_{rs}: Series resonant characteristics impedance ($Z_{rs} = \sqrt{L_s/C_s}$)
Z_{rm}: LLC resonant characteristics impedance ($Z_{rm} = \sqrt{(L_s+L_m)/C_s}$)
Z_{rp}: Anti-resonant characteristics impedance ($Z_{rp} = \sqrt{L_p/C_p}$)
Q_{rs}: Series resonant loaded quality factor ($Q_{rs} = Z_{rs}/R_{ac}$)
λ_{rs} : Series / ant-resonant characteristics impedances ratio ($\lambda_{rs} = Z_{rs}/Z_{rp}$)
λ_{rm}: LLC / anti-resonant characteristics impedances ratio ($\lambda_{rm} = Z_{rm}/Z_{rp}$)

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I. Introduction

An asymmetrical half-bridge LLC resonant dc-dc converter has been gaining the popularity in a variety of switching power supplies encompassing from a small power ICT equipment, LED lighting, battery chargers for electric vehicles, to a dc micro-grid power distribution system due to a soft-switching operation over the wide range of load power; zero voltage soft-switching (ZVS) of active switches and zero current soft-switching (ZCS) of rectifier diodes[1]–[11]. The wide range of soft switching operation in the LLC converter is attractive for a full-bridge dc-dc converter topology as well, while a typical phase-shift pulse-width-modulation (PS-PWM) full-bridge circuit topology suffers from a severely-limited range of soft switching for load power variations.

The primary modulation scheme of the LLC converter is PFM since the magnetizing current of the high-frequency (HF) transformer can be utilized for ZVS under the wide load conditions, as treated in the majority of the reference papers[1]-[15]. In contrast to the advantageous characteristics mentioned above, the operation of LLC converter is

inherently allocated over the unity gain of the input-output voltage ratio, which is named herein as "boost area", for ensuring the excellent soft switching performance and lower switching noise emission. This constraint of voltage regulation poses another performance limitation on the LLC converter especially under the short-circuit and overload conditions due to a moderate sensitivity in the PFM-controlled voltage ratio characteristics[16][17]. Therefore, over-current might occur in building up the output voltage quickly at the start-up process of the LLC converter, where the dc power is fed from the dc-bus that is tightly controlled to 380 V into the low-voltage dc load as appears in a dc microgrid system[18].

As a solution for this technical problem, a pulse modulation strategy that incorporates an asymmetrical pulse-width-modulation (PWM) into PFM has been proposed in [16]. Although it can be effective for the start-up process, no over-current protection is guaranteed for the short-circuit load condition by the hybrid pulse modulation scheme. This technical problem will affect on feasibility and reliability of power converters in the dc-source power supplies such as microgrid and transportation applications.

A circuitry-oriented method for the OCP has been proposed in [19]. This converter features an auxiliary circuit for clamping the resonant capacitor voltage in case of the short-circuit load, thereby limits the over-current in the primary-side inverter. This technique is, however, effective only for a low output voltage application since the clamping voltage depends on the output voltage, accordingly not suitable for the full-bridge topology. In addition, the auxiliary transformer and rectifier diodes will lead to increase of power losses and deteriorate the efficiency under light load conditions.

As a more advantageous solution for the OCP, the anti-resonant circuitry-applied dc-dc converter has been proposed in [20]-[25]. Among those literatures, an LLC asymmetrical half-bridge dc-dc converter with a notch filter has been reported in [20]. However, the main idea of the converter is to actively inject the third-harmonics current by the effect of the anti-resonance due to the notch filter, and utilize the harmonics component as the active power. Another literature [21] also deals with the anti-resonant tank-based LLC converter has been presented for protecting it from the over-current under the short-circuit and overload conditions as well as the start-up process. However, the main argument of the literature is focused on exploring a method of magnetic integration of resonant inductors and utilizing the third harmonics components as well as the discussion in [20]. Injection of the harmonics components will lead to decrease of the most useful component; fundamental frequency (switching frequency) active power, consequently the converter efficiency might deteriorate especially for the full-bridge LLC converter applications. Both of the two reference papers include no evaluation on the actual performances of the multi-resonant dc-dc converter nor circuit parameter design guideline is deeply discussed with experimental verifications.

The LLC resonant full-bridge dc-dc converter with an LC anti-resonant tank, named as "LLC-LC resonant converter" has been proposed by the authors of this paper in [22]–[25]. The original idea of the proposed resonant converter is to achieve OCP with a designed anti-resonant frequency and characteristics impedance while the operating principle of the LLC converter is retained under the normal load condition between two series resonant frequencies. Accordingly, it can be ensured to supply the fundamental frequency components of HF resonant current and active power to the load while precluding the harmonics components. The circuit topology and PFM scheme contribute for a wider range of buck voltage regulation with a smaller band of switching frequency variations besides the inherent boost operation. Thus, the buck and boost voltage regulations that are tantamount to a pulse-amplitude-modulation (PAM)-based input dc voltage control can attain in the LLC-LC converter.

The relevant papers [22]–[24] have verified the buck and boost voltage regulations of the proposed converter. In addition, the dual pulse modulation scheme suitable for the LLC-LC dc-dc converter has been investigated in [25], whereby it has been verified that power conversion efficiency can improve by adopting pulse-density-modulation (PDM) for the light load conditions.

This paper presents the performance of the LLC-LC resonant converter with the complete experimental results on soft-switching performance, output voltage and power regulations, power conversion efficiency and loss analysis, including the design consideration of resonant tank parameters, all of which are not mentioned or evaluated in any past reference papers. Performance comparison between the LLC and proposed converters are presented in experiment, then the feasibility of the LLC-LC resonant topology are proven. Furthermore, the steady-state characteristics of the series and anti-resonant tanks are originally analyzed by the state-plane trajectory, which is truly effective for demonstrating the power and energy within the resonant tanks[26].

The rest of this paper is organized as follows. The steady-state performances on the voltage and power regulations of the LLC converter are theoretically described in Section II, whereby the low sensitivity of PFM for the buck voltage regulation is pointed out by the relevant characteristics curves. The circuit configuration and operation principle of the proposed LLC-LC converter are explained in Section III, after which the series-/anti-resonant frequencies are explained in conjunction with the resonant tank impedances as well as the input impedance of the proposed converter. The design procedure of the circuit parameters and resonant frequencies are described in Section IV. The essential performances on the wide range of output voltage and power regulations with soft-switching are demonstrated by the time-domain analysis with both the calculation and measured state plane trajectories under the various load conditions including the short-load in Section V, and compared with the LLC converter. Finally, the experimental verifications ate summarized, then effectiveness of the multi-element resonant dc-dc converter topology is originally revealed from a practical point of view in Section VI.

II. PFM Characteristics of LLC Resonant DC–DC Converter

The circuit diagram of LLC resonant full-bridge dc-dc converter is depicted in Fig. 1. The series inductor L_s includes

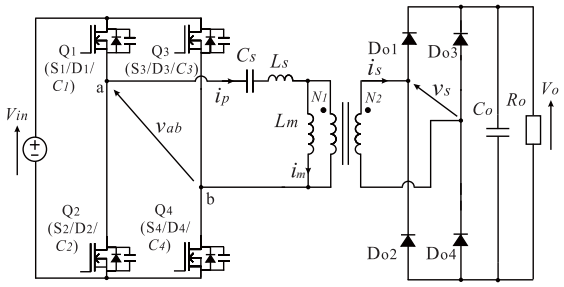


Fig. 1. Circuit diagram of the conventional LLC resonant full-bridge dc-dc converter.

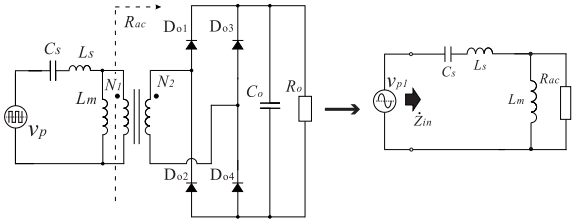


Fig. 2. Simplified equivalent circuits of LLC converter based on FHA method.

the leakage inductance of the HF transformer, while the resonant capacitor C_s is additionally inserted in the primary-side HF inverter.

The steady-state characteristics of the LLC converter can be derived from the Fundamental Harmonics Approximation (FHA)[27]. This analysis method is based on the simplified equivalent circuit of the LLC converter as shown in Fig. 2, where the fundamental component v_{p1} of the rectangular voltage v_p in the HF inverter is defined by

$$v_{p1}(t) = \frac{4}{\pi} V_{in} \sin \omega_s t. \tag{1}$$

The input impedances Z_{in} of the LLC converter are defined from Fig. 2 as

$$Z_{in} = \left|\dot{Z}_{in}\right| = \left| \frac{\omega_s L_m \left(1 - {F_{rs}}^2\right) - j R_{ac} \left(1 - {F_m}^2\right)}{\omega_s C_s \left(R_{ac} + j \omega_s L_m\right)} \right|. \tag{2}$$

The input impedance versus switching frequency curves are drawn in Fig 3 by referring to (2). The voltage conversion ratio $M = V_o/V_{in}$ of the LLC converter can be derived from Fig. 2 as

$$M = \frac{1}{a\sqrt{\left(1 + \frac{1}{S} - \frac{1}{S{F_{rs}}^2}\right)^2 + {Q_{rs}}^2 \left(F_{rs} - \frac{1}{F_{rs}}\right)^2}} \tag{3}$$

Based on (3), the theoretical characteristics of the voltage conversion ratio and output power versus normalized switching frequency for the LLC converter are depicted in Fig. 4 (a) and (b), respectively. The frequency area between f_{rm} and f_{rs} is defined as "ZVS area 1", and dedicates for the boost operation. The frequency area over f_{rs} is defined as "ZVS area 2" and performs the buck operation. The voltage conversion ratio M in the frequency area $f_s > f_{rs}$ exhibits the flat curve due

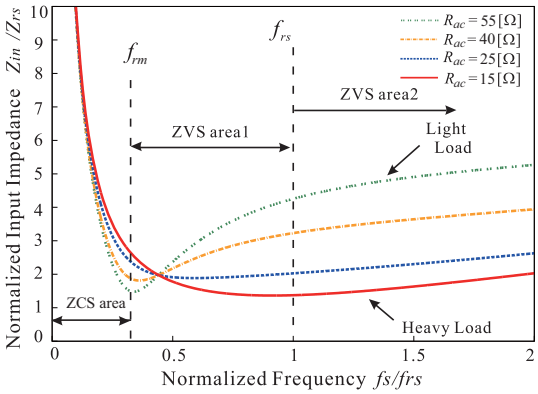


Fig. 3. Theoretical input impedance characteristics of LLC converter.

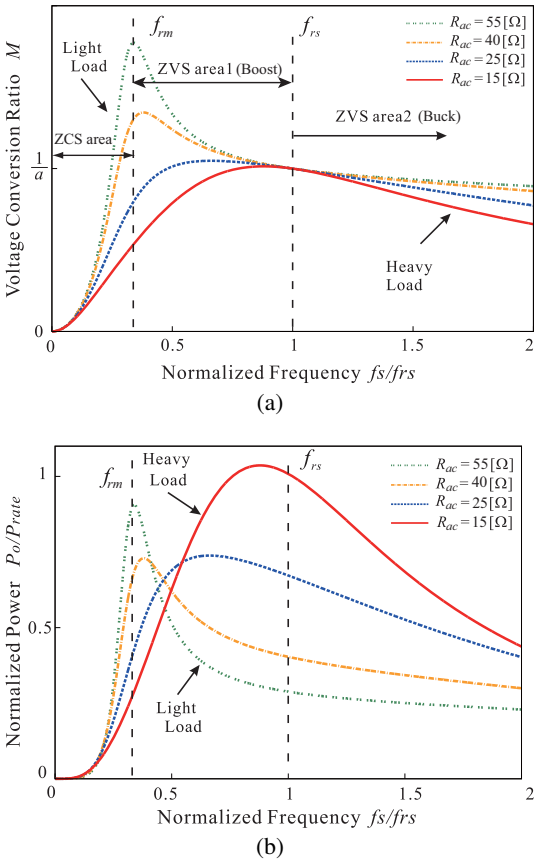


Fig. 4. Theoretical characteristics of the LLC converter:(a) M–normalized f_s, and (b) normalized P_o–normalized f_s.

to the low-sensitivity impedance of the series resonant tank, consequently the output power cannot also be regulated widely for the load power variations. It should be noted here the frequency area below f_{rm} represents the ZCS area, which is not suitable for the LLC converter because the soft switching is lost at the turn-on transitions of Q_1–Q_4.

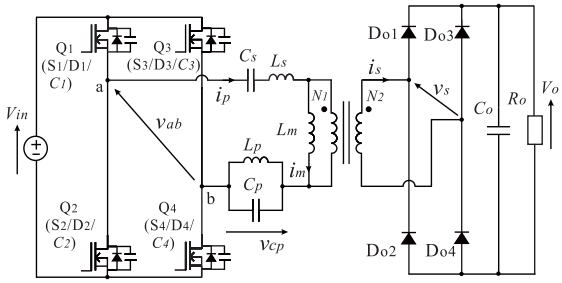


Fig. 5. Proposed LLC-LC resonant full-bridge dc-dc converter.

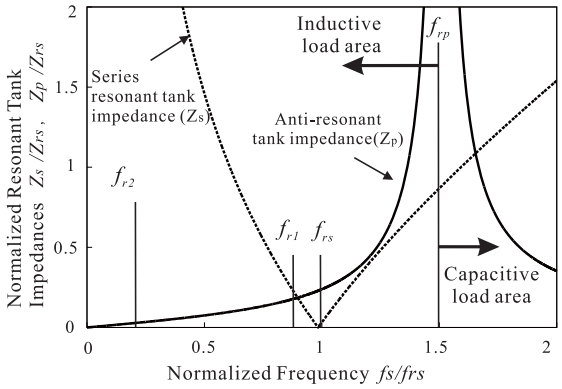


Fig. 6. Theoretical characteristics of the series and anti-resonant impedances versus switching frequency in the proposed LLC-LC converter.

III. Proposed LLC-LC Resonant DC–DC Converter

A. Circuit Topology and Operating Principle

The proposed LLC-LC resonant full-bridge dc-dc converter is schematically depicted in Fig. 5[22]-[24]. The anti-resonant tank (L_p-C_p) is employed in series with the series resonant network (L_s-C_s) in the primary-side HF inverter.

The proposed converter has two series resonant frequencies; the first resonant frequency f_{r1} and the second resonant frequency f_{r2} are defined respectively as (4) and (5), where $Q_{rp}\,(=Z_{rp}/R_{ac})$ denotes the impedances ratio with respect to the anti-resonant tank. The series and anti-resonant tank impedances Z_s, Z_p are defined respectively as

$$Z_s = \left|\dot{Z}_s\right| = \left|j\left(\omega_s L_s - \frac{1}{\omega_s C_s}\right)\right| \tag{6}$$

$$Z_p = \left|\dot{Z}_p\right| = \left|\frac{j\omega_s L_p}{1-{\omega_s}^2 L_p C_p}\right|. \tag{7}$$

Based on (6) and (7), the typical characteristics of series and anti-resonant tank impedances versus switching frequency are illustrated in Fig. 6. According to the PFM scheme, Z_s and Z_p are correlatively expressed as

$$f_{r2} \le f_s < f_{r1} \Rightarrow Z_s \gg Z_p \tag{8}$$

$$f_s = f_{r1} \Rightarrow Z_s = Z_p \tag{9}$$

$$f_{r1} < f_s < f_{rp} \Rightarrow Z_s < Z_p \tag{10}$$

$$f_s = f_{rp} \Rightarrow Z_p \to \infty. \tag{11}$$

The HF transformer primary-side current I_p^* under the short-circuit and overload conditions can be theoretically expressed at $f_s = f_{rp}$ as

$$I_p^* = \frac{V_{rp,max}}{Z_p} = \frac{4V_{in}(1-{\omega_s}^2 L_p C_p)}{\pi\omega_s L_p} \to 0 \tag{12}$$

where Z_p is defined by (11).

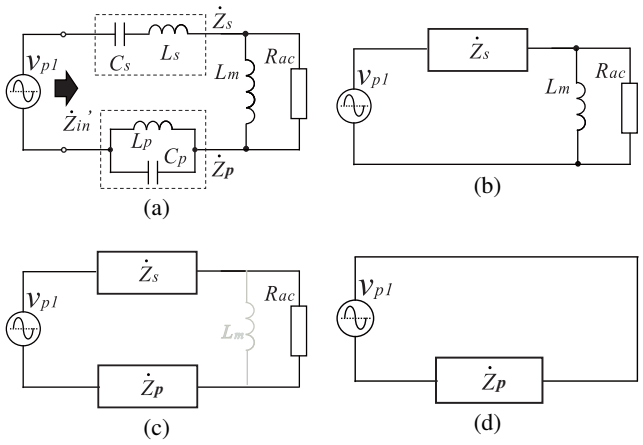


Fig. 7. Simplified equivalent circuits of LLC-LC converter: (a) common topology, and modified for (b) $f_{r2} \le f_s < f_{r1}$, (c) $f_{r1} \le f_s < f_{rp}$, (d) $f_s = f_{rp}$.

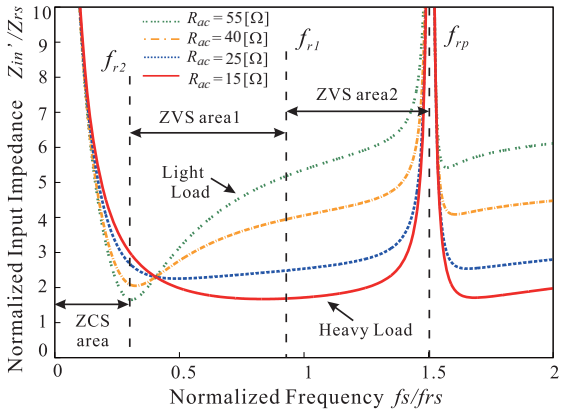


Fig. 8. Theoretical input impedance characteristics of LLC-LC converter.

The frequency-domain equivalent circuits of the proposed LLC-LC converter are illustrated in Fig. 7, where the frequency-dependent modifications are included in accordance with (8)-(11). The input impedance $Z_{in}{}'$ can be defined on the basis of Fig. 7 as (13).

Based on (13), the input impedance versus switching frequency curves are depicted in Fig. 8. In $f_{r2} \le f_s \le f_{r1}$; ZVS area 1, $Z_{in}{}'$ exhibits the property similar to Z_{in} of Fig. 3, thus no significant difference on the operating characteristics appears between the LLC and LLC-LC converters. On the other hand, $Z_{in}{}'$ escalates with a high sensitivity in $f_{r1} < f_s \le f_{rp}$; ZVS area 2. In order to mitigate the influence of anti-resonant tank in the ZVS area 1, the input impedance of the LLC-LC converter should be designed as compatible with the LLC converter.

The theoretical voltage conversion ratio M of the proposed converter can be derived similarly from FHA as (14) and

$$f_{r1} = \sqrt{\frac{{f_{rs}}^2 + {\lambda_{rs}}^{-1} f_{rs} f_{rp} + {f_{rp}}^2 - \sqrt{\left({f_{rs}}^2 + {\lambda_{rs}}^{-1} f_{rs} f_{rp} + {f_{rp}}^2\right)^2 - 4{f_{rs}}^2 {f_{rp}}^2}}{2}} \tag{4}$$

$$f_{r2} = \sqrt{\frac{{f_{rm}}^2 + {\lambda_{rm}}^{-1} f_{rm} f_{rp} + {f_{rp}}^2 - \sqrt{\left({f_{rm}}^2 + {\lambda_{rm}}^{-1} f_{rm} f_{rp} + {f_{rp}}^2\right)^2 - 4{f_{rm}}^2 {f_{rp}}^2}}{2}} \tag{5}$$

$$Z_{in}{}' = \left|\dot{Z}_{in}{}'\right| = \left| \frac{\omega_s L_m \left[1 - \left(1 - {F_{rs}}^2\right) {F_{rp}}^2 - \left(1 + 1/\gamma_L\right) {F_{rs}}^2\right]}{\omega_s C_s \left(1 - {F_{rp}}^2\right) \left[R_{ac} + j\omega_s L_m\right]} - j \frac{R_{ac} \left[1 - \left(1 - {F_{rp}}^2\right) {F_m}^2 - \left(1 + \gamma_c\right) {F_{rp}}^2\right]}{\omega_s C_s \left(1 - {F_{rp}}^2\right) \left[R_{ac} + j\omega_s L_m\right]} \right| \tag{13}$$

$$M = \frac{1}{a\sqrt{\left(1 + \frac{\xi}{\omega L_m}\right)^2 + \left[Q_{rs}\left(F_{rs} - \frac{1}{F_{rs}}\right) - Q_{rp}\left(F_{rp} - \frac{1}{F_{rp}}\right)^{-1}\right]^2}} \tag{14}$$

$$\xi = Z_{rs}\left(F_{rs} - \frac{1}{F_{rs}}\right) - Z_{rp}\left(F_{rp} - \frac{1}{F_{rp}}\right)^{-1}. \tag{15}$$

(15). Based on (14), the theoretical curves of the voltage conversion ratio and output power versus the normalized switching frequency are shown in Fig. 9. Those curves indicate the dc voltage conversion ratio decreases due to the high-sensitivity of PFM in the ZVS area 2, consequently the output voltage can be regulated over the wide range of load power variations by the effect of the anti-resonant tank. It should be remarked the FHA-based analysis is effective for the proposed converter since the harmonics in the resonant currents of the primary- and secondary-side circuits can be suppressed by designing f_{rp} and Z_{rp}.

B. Switching Mode Transitions

The key operating waveforms and mode-transition equivalent circuits of the proposed converter for the ZVS area 1 (boost voltage regulation) are shown in Figs.10 (a) and (b), respectively. The circuit operation during one switching cycle can be divided into ten modes as follows:

- Mode 1 [power transfer mode (i_m reverses its polarity and linearly increases): $t_0 \le t < t_1$] The polarity of the magnetizing current i_m reverses from negative to positive at $t = t_0$. During this interval, the active switches Q_1 and Q_4 are on-state, then the power starts to be fed from the input voltage source V_{in} to the load R_o. The primary-side HF inverter current i_p gradually decays toward zero by the effect of series resonance.
- Mode 2 [$\mathrm{D}_{o1}, \mathrm{D}_{o4}$ ZCS turn-off mode: $t_1 \le t < t_2$] The primary-side current i_p decreases gradually due to the series resonance by L_s and C_s, then it corresponds to i_m at $t = t_1$. The secondary-side current i_s naturally becomes zero, as a result D_{o1} and D_{o4} can be turned-off by ZCS with a minimized reverse recovery current. During this interval, i_m appears only in the primary-side HF inverter, while the secondary-side rectifier gets into the discontinuous conduction current mode (DCM).
- Mode 3 [$\mathrm{Q}_1, \mathrm{Q}_4$ ZVS turn-off mode: $t_2 \le t < t_3$] The gate signals for Q_1 and Q_4 are removed at $t = t_2$. Then, their voltages v_{Q1} and v_{Q4} rise gradually from zero with the effects of parasitic, or the lossless snubber capacitors C_1–C_4, while the voltages v_{Q2} and v_{Q3} across Q_2 and Q_3 decrease gradually from V_{in} to zero. ZVS turn-off herein can be attained by i_m in Q_1 and Q_4. During this interval, ZVS condition is defined by

$$\frac{1}{2} L_m i_m(t_2)^2 > 2 C_r V_{in}^2, \tag{14}$$

  where C_r represents the lossless snubber capacitor $C_1 = C_2 = C_3 = C_4$.
- Mode 4 [$\mathrm{Q}_2, \mathrm{Q}_3$ ZVS & ZCS turn-on / $\mathrm{D}_{o2}, \mathrm{D}_{o3}$ ZCS turn-on mode: $t_3 \le t < t_4$] The voltages v_{Q2} and v_{Q3} across Q_2 and Q_3 reach to zero at $t = t_3$ due to the edge-resonance sustaining from Mode 3, thereby D_2 and D_3 are forward-biased. During this interval, the gate terminals of Q_2 and Q_3 are triggered, thereby ZVS & ZCS turn-on commutation can be achieved in the two switches. At the same time, i_p reverses its polarity, then i_s begins to rise gradually from zero. Thus, ZCS turn-on can be obtained in D_{o2} and D_{o3}.
- Mode 5 [power transfer mode (i_m linearly decreases): $t_4 \le t < t_5$] At $t = t_4$, the current through Q_2 and Q_3 commutate from D_2 and D_3 to S_2 and S_3. Accordingly, power transfers from V_{in} to R_o in the resonant behavior.
- Mode 6 [power transfer mode (i_m reverses its polarity and linearly decreases): $t_5 \le t < t_6$] The polarity of i_m reverses from positive to negative at $t = t_5$. During this interval, Q_2 and Q_3 are on-state, then power starts to be fed from V_{in} to R_o. Accordingly, i_p gradually decays toward zero by the effect of series resonance.

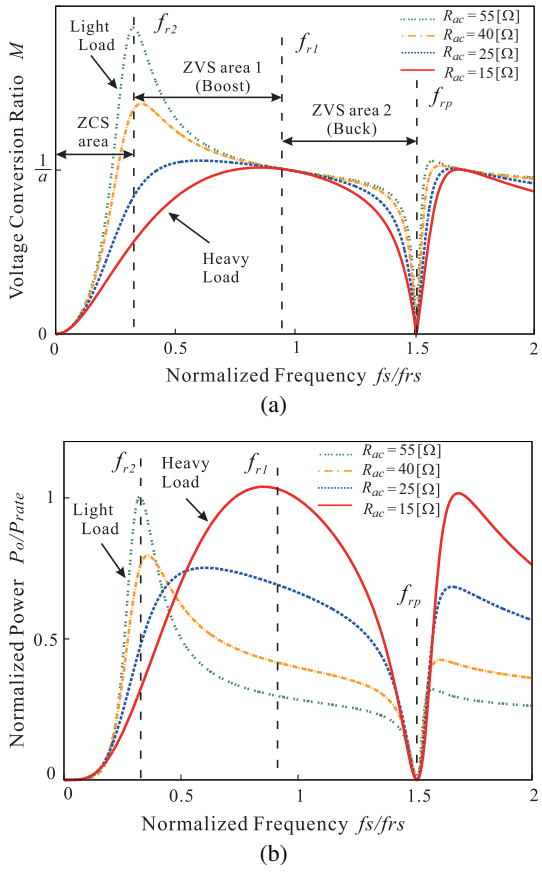


Fig. 9. Theoretical characteristics of the LLC-LC converter : (a) M–normalized f_s, and (b) normalized P_o–normalized f_s.

- Mode 7 [D_{o2}, D_{o3} ZCS turn-off mode: $t_6 \le t < t_7$] The primary-side i_p decreases gradually due to the series resonance by L_s and C_s, and it corresponds with i_m at $t = t_6$. Then, the secondary-side i_s naturally becomes zero, as a result D_{o2} and D_{o3} can be turned-off by ZCS with a minimized reverse recovery current. During this interval, i_m appears only in the primary-side circuit, while the secondary-side power stage gets into DCM.
- Mode 8 [Q_2, Q_3 ZVS turn-off mode: $t_7 \le t < t_8$] The gate signals for Q_2 and Q_3 are removed at $t = t_7$. Then, their voltages v_{Q2} and v_{Q3} rise gradually from zero with the effects of parasitic, or the lossless snubber capacitors $C_1 - C_4$, while the voltages across Q_1 and Q_4 decrease gradually from V_{in} to zero. ZVS turn-off herein can be attained by i_m in Q_2 and Q_3. During this interval, ZVS condition is expressed by

$$\frac{1}{2} L_m i_m(t_7)^2 > 2 C_r V_{in}^2. \quad (15)$$

- Mode 9 [Q_1, Q_4 ZVS &ZCS turn-on / D_{o1}, D_{o4} ZCS turn-on mode: $t_8 \le t < t_9$] The terminal voltages v_{Q1} and v_{Q4} reach to zero at $t = t_8$ due to the edge-resonance sustaining from Mode 8, then D_1 and D_4 are forward-biased. During this interval, the gate terminals of Q_1 and Q_4 are triggered, thereby ZVS & ZCS turn-on commutation can be achieved in those switches. At the same time, i_p reverses its polarity, then i_s begins to rise gradually from zero. Thus, ZCS turn-on can be obtained in D_{o1} and D_{o4}.
- Mode 10 [power transfer mode (i_m linearly increases): $t_9 \le t < t_{10}$] At $t = t_9$, the current through Q_1 and Q_4 commutate from D_1 and D_4 to S_1 and S_4. Accordingly, the power transfer stars from V_{in} to R_o in the resonant behavior.

The voltage and current waveforms for the ZVS area 2 (buck voltage regulation) are depicted in Fig. 11 (a), and the corresponding circuit transitions are illustrated in Fig. 11 (b), respectively. The secondary-side current i_s is naturally continuous in the ZVS area 2, so the operating and commutation process is similar to ZVS area 1 with the exception of Mode 2 and Mode 7 mentioned above.

The time-domain formulas with high-order differential equations are summarized in TABLE I for the ZVS area 1 and the ZVS area 2, respectively. The resonant capacitor voltage v_{cs} of the series resonant tank is selected as the state valuable to express the steady-state operations of the proposed coverer. Accordingly, the current i_{Ls} through L_s, current i_{Lp} through L_p and voltage v_{cp} across C_p can be expressed on the basis of v_{cs} as

$$i_{Ls} = C_s \frac{dv_{cs}}{dt}, \; i_{Lp} = \frac{-{\omega_s}^2 L_p C_p i_{Ls}}{1 - {\omega_s}^2 L_p C_p}, \; v_{cp} = L_p \frac{di_{Lp}}{dt}. \quad (16)$$

IV. Design Procedure of Circuit Parameters

A. Resonant Frequencies

The first resonant frequency f_{r1} and the second resonant frequency f_{r2} of the proposed LLC-LC converter are designed as close to f_{rs} and f_{rm} of the LLC converter, respectively. The anti-resonant frequency f_{rp} should be set well less than three times f_{r1} for precluding the harmonics from i_p while the switching frequency variation from f_{r1} should be small as much as possible for a better response of the OCP. This idea on setting the resonant frequencies leads to a design guideline of $f_{rp} = 1.5 f_{r_1}$.

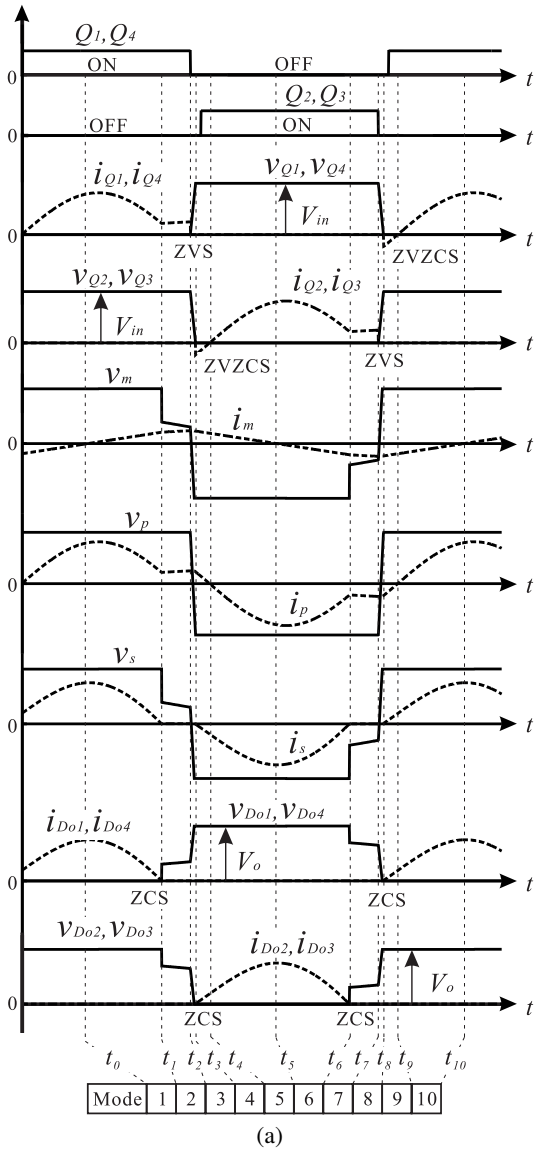
Once f_{rs} and f_{rm} are set as 90 kHz and 30 kHz in consideration of the wide-range ZVS operation in the LLC converter, the anti-resonant frequency f_{rp} can be designed as

$$f_{rp} = 1.5 f_{r1} = 135\,\text{kHz}. \quad (17)$$

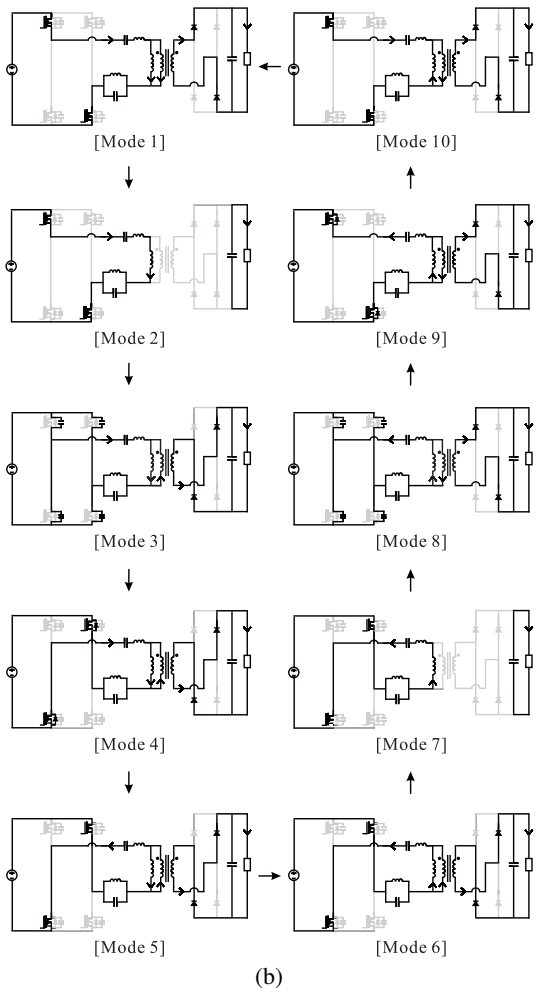
The resonant tank characteristics impedances ratios of the proposed converter are given by considering F_{rp} for ${Z_{in}}'$ as $\lambda_{rs} = 5$ and $\lambda_{rm} = 15$. As a result, the first and second resonant frequencies are designed from (4) and (5) as $f_{r1} = 86\,\text{kHz}$ and $f_{r2} = 27\,\text{kHz}$, respectively. Thus, the switching frequency band of PFM for the proposed converter can be determined as

$$f_{r2} = 27\,\text{kHz} \le f_s \le f_{r1} = 86\,\text{kHz} \text{ (for ZVS area 1)} \quad (18)$$
$$f_{r1} = 27\,\text{kHz} < f_s \le f_{rp} = 135\,\text{kHz} \text{ (for ZVS area 2)} \quad (19)$$

where the minimum and maximum switching frequencies can also be expressed as 27 kHz and 135 kHz.



(a)



(b)

Fig. 10. Key voltage and current waveforms, and switch-mode transitions operating in $f_{r2} \leq f_s \leq f_{r1}$ (ZVS area 1): (a) voltage and current waveforms during one switching-cycle, and (b) equivalent circuits.

TABLE I
STEADY-STATE TIME-DOMAIN FORMULAS OF THE SERIES RESONANT CAPACITOR VOLTAGE

Intervals	ZVS area 1 (secondary-side DCM)
$*t_0 \leq t < t_1$	$\frac{d^4 v_{cs}(t)}{dt^4} + \left(\omega_{rs}^2 + \omega_{sp1}^2 + \omega_{rp}^2\right) \frac{d^2 v_{cs}(t)}{dt^2} + \omega_{rs}^2 \omega_{rp}^2 v_{cs}(t) = \omega_{rs}^2 \omega_{rp}^2 (V_{in} - aV_o)$
$t_1 \leq t < t_2$	$\frac{d^4 v_{cs}(t)}{dt^4} + \left(\omega_m^2 + \omega_{sp2}^2 + \omega_{rp}^2\right) \frac{d^2 v_{cs}(t)}{dt^2} + \omega_m^2 \omega_{rp}^2 v_{cs}(t) = \omega_m^2 \omega_{rp}^2 V_{in}$
$t_2 \leq t < t_3$	$\frac{d^4 v_{cs}(t)}{dt^4} + \left[\left(1 + \frac{C_s}{C_{sp}}\right) \omega_m^2 + \omega_{sp2}^2 + \omega_{rp}^2\right] \frac{d^2 v_{cs}(t)}{dt^2} + \left(1 + \frac{C_s}{C_{sp}}\right) \omega_m^2 \omega_{rp}^2 v_{cs}(t) = 0$
Intervals	ZVS area 2 (secondary-side CCM)
$**t_0 \leq t < t_1$	$\frac{d^4 v_{cs}(t)}{dt^4} + \left(\omega_{rs}^2 + \omega_{sp1}^2 + \omega_{rp}^2\right) \frac{d^2 v_{cs}(t)}{dt^2} + \omega_{rs}^2 \omega_{rp}^2 v_{cs}(t) = \omega_{rs}^2 \omega_{rp}^2 (V_{in} - aV_o)$
$t_1 \leq t < t_2$	$\frac{d^4 v_{cs}(t)}{dt^4} + \left[\left(1 + \frac{C_s}{C_{sp}}\right) \omega_{rs}^2 + \omega_{sp1}^2 + \omega_{rp}^2\right] \frac{d^2 v_{cs}(t)}{dt^2} + \left(1 + \frac{C_s}{C_{sp}}\right) \omega_{rs}^2 \omega_{rp}^2 v_{cs}(t) = -\omega_{rs}^2 \omega_{rp}^2 aV_o$
$t_1 \leq t < t_2$	$\frac{d^4 v_{cs}(t)}{dt^4} + \left(\omega_{rs}^2 + \omega_{sp1}^2 + \omega_{rp}^2\right) \frac{d^2 v_{cs}(t)}{dt^2} + \omega_{rs}^2 \omega_p^2 v_{cs}(t) = \omega_{rs}^2 \omega_{rp}^2 (V_{in} + aV_o)$
$C_{sp} = \frac{C_s + C_p}{C_s C_p}$, $\omega_{rs} = \frac{1}{\sqrt{L_s C_s}}$, $\omega_{sp1} = \frac{1}{\sqrt{L_s C_p}}$, $\omega_{rp} = \frac{1}{\sqrt{L_p C_p}}$, $\omega_m = \frac{1}{\sqrt{(L_s + L_m) C_s}}$, $\omega_{sp2} = \frac{1}{\sqrt{(L_s + L_m) C_p}}$, $a = \frac{N_1}{N_2}$	

*Following to previous Mode 8 in Fig.10, **Following to previous Mode 8 in Fig.11

B. Resonant Inductors and Capacitors

By setting the lossless snubber capacitor C_r ($= C_1 = \cdots = C_4$) as 1 nF to attain a low dv/dt rate sufficient for the ZVS turn-off transitions of Q_1–Q_4 with the constant dc input voltage V_{in} ($= 220$ V), the magnetizing inductance L_m of the

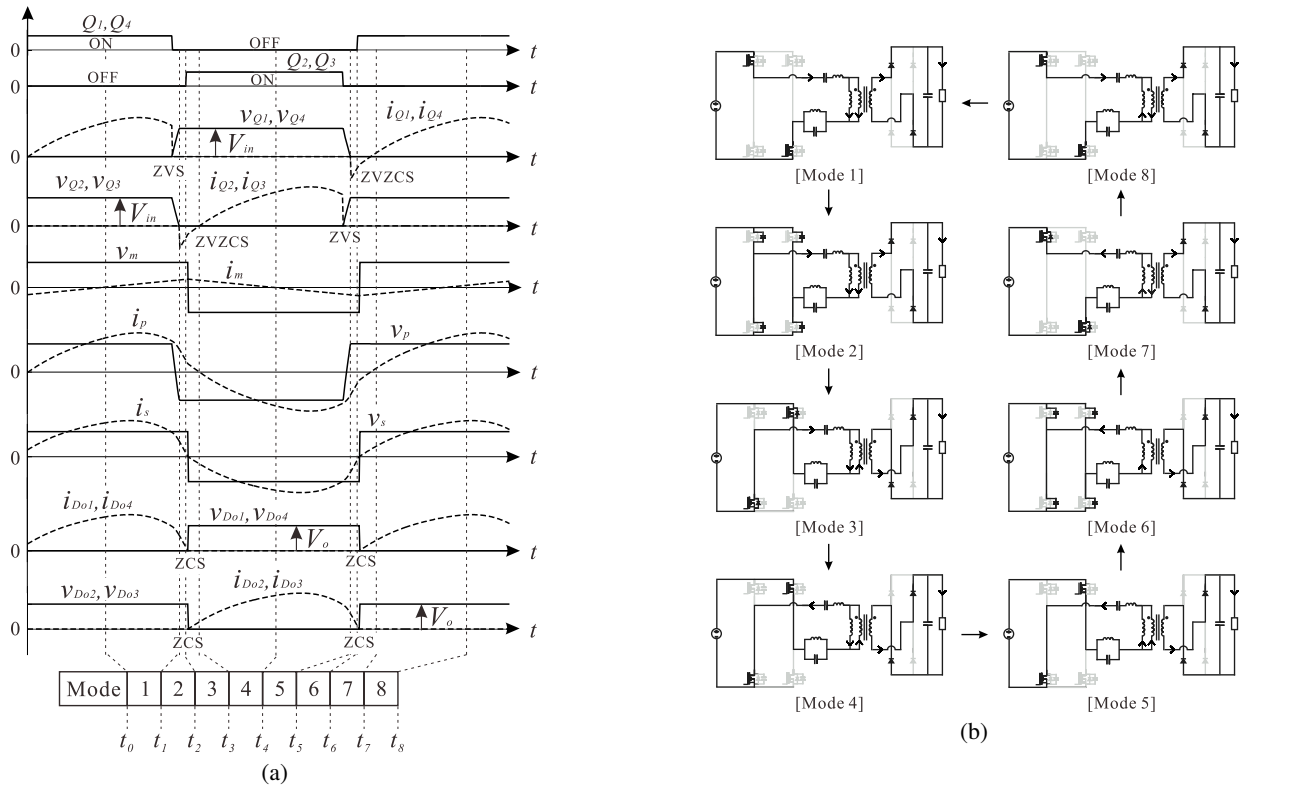


Fig. 11. Key voltage and current waveforms, and switch-mode transitions operating in $f_{r1} < f_s \leq f_{rp}$ (ZVS area 2): (a) voltage and current waveforms during one switching-cycle, and (b) equivalent circuits.

HF transformer can be determined from (14) and (15) as

$$L_m = \frac{4C_r {V_{in}}^2}{{i_{m,min}}^2} = 190\,\mu\text{H} \tag{20}$$

where $i_{m,min}$ represents the magnetizing current of the HF transformer at the turn-off transitions of Q_1–Q_4 under the minimum load condition, and assumed $= 1$ A herein. The series resonant-tank inductor L_s is designed as

$$L_s = \frac{L_m}{S} \simeq 16\,\mu\text{H} \tag{21}$$

where S is selected more than 10 in order to suppress the circulating current in the primary-side HF inverter.

The series and anti-resonant inductors ratio γ_L should be given by considering $Z_{in}{}'$ characteristics in the ZVS area 1 of Fig. 8. When γ_L is selected as greater than 5, the anti-resonant inductor L_p can be determined as

$$L_p = \frac{L_s}{\gamma_L} \simeq 2.5\,\mu\text{H}. \tag{22}$$

The series-resonant capacitor C_s and the anti-series resonant capacitor C_p can be determined from (4) and (5) with (21) and (22), respectively as

$$\begin{aligned} C_s &= \frac{{f_{rs}}^2 - {f_{rp}}^2}{(2\pi f_{rs})^2\left[\left({f_{rs}}^2 - {f_{rp}}^2\right)L_s - {f_{rp}}^2 L_p\right]} \\ &= \frac{1}{(2\pi f_{rs})^2 L_s\left[1 + \frac{1}{\gamma_L\{1-\left(\frac{f_{rs}}{f_{rp}}\right)^2\}}\right]} \simeq 170\,\text{nF} \end{aligned} \tag{23}$$

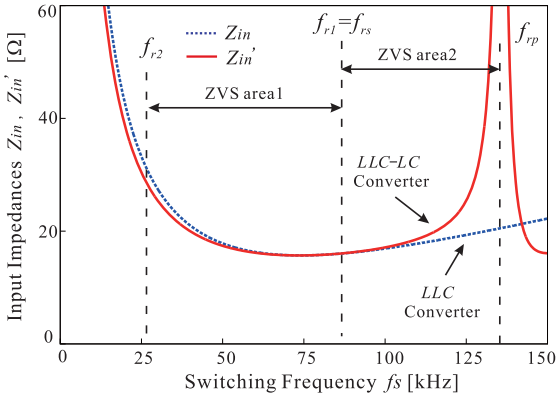


Fig. 12. Input impedance characteristics of the LLC and LLC-LC converters with the circuit parameters based on the design procedure.

$$C_p = \frac{1}{{\omega_{rp}}^2 L_p} = \frac{1}{(2\pi f_{rp})^2 L_p} = \frac{\gamma_L}{(2\pi f_{rp})^2 L_s} \simeq 550\,\text{nF}. \tag{24}$$

Based on those circuit parameters of the series and anti-resonant tanks, the input impedance characteristics of the LLC and LLC-LC converters are depicted in Fig.12 for the rated output power and voltage condition. Due to the circuit parameters designed above, the LLC-LC converter exhibits the comparable characteristics to those of the LLC converter in the ZVS area 1.

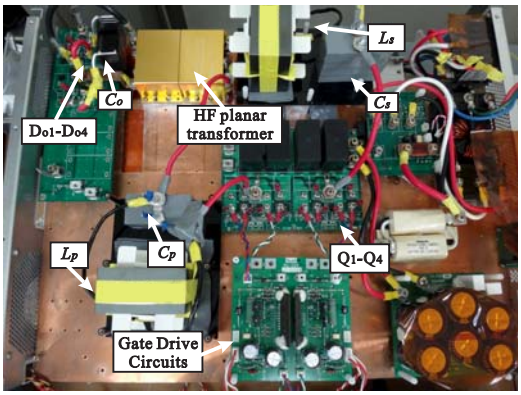


Fig. 13. Exterior appearance of the LLC-LC converter prototype.

TABLE II
CIRCUIT PARAMETERS AND SPECIFICATION OF PROTOTYPES

Item,Symbol	Value
Input dc voltage V_{in}	220 V
Rated output voltage V_o	240 V
Rated output power P_o	2.5 kW
HF transformer windings turns ratio $a(=N_1/N_2)$	$1(=6/6)$
HF transformer magnetizing inductance L_m	190 μH
Series resonant-tank inductor L_s	16 μH
Series resonant capacitor C_s	170 nF
Anti-resonant inductor L_p	2.5 μH
Anti-resonant capacitor C_p	550 nF
Lossless snubber capacitors $C_r = C_{1-4}$	1 nF
Output smoothing capacitor C_o	20 μF
First series-resonant frequency (LLC) f_{rs}	90 kHz
Second series-resonant frequency(LLC) f_{rm}	30 kHz
First series-resonant frequency (LLC-LC) f_{r1}	86 kHz
Second series-resonant frequency(LLC-LC) f_{r2}	27 kHz
Anti-resonant frequency f_{rp}	135 kHz

V. EXPERIMENTAL RESULTS AND EVALUATIONS

A. Specification of Prototype

The performances of the proposed LLC-LC converter are evaluated in experiment using a 2.5 kW laboratory prototype by comparison with a LLC converter prototype. The exterior appearance of the proposed converter prototype with a HF planer transformer is depicted in Fig. 13, and the circuit parameters and specifications which are introduced in Section IV are listed in TABLE II, respectively. The super junction-power MOSFETs (IXYS IXKN 40N 60C: 600 V-40 A) are applied for Q_1–Q_4 while the fast recover diodes (IXYS DSEI 2x31-06C: 600 V-60 A) are implemented for D_{o1}–D_{o4}.

B. Soft-Switching Performance

The switching waveforms of the LLC-LC converter prototype under a heavy load condition (80 % output power) are shown in Fig. 14. ZVS and ZCS commutations can be actually confirmed from those results. Fig. 15 shows the switching waveforms under a light load condition (20 % output power), which proves ZVS and ZCS commutations can achieve for the light load area as well.

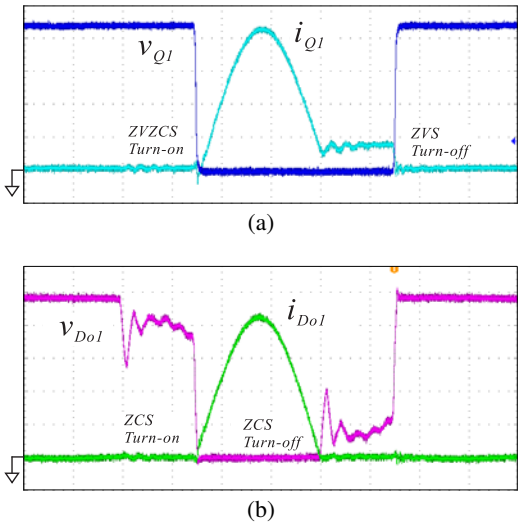


Fig. 14. Observed waveforms of the LLC-LC converter prototype at $f_s = 61$ kHz and $P_o = 2$ kW: (a) active switch Q_1, and (b) rectifying diode D_{o1} (100 V/div, 5 A/div, 2 μs/div).

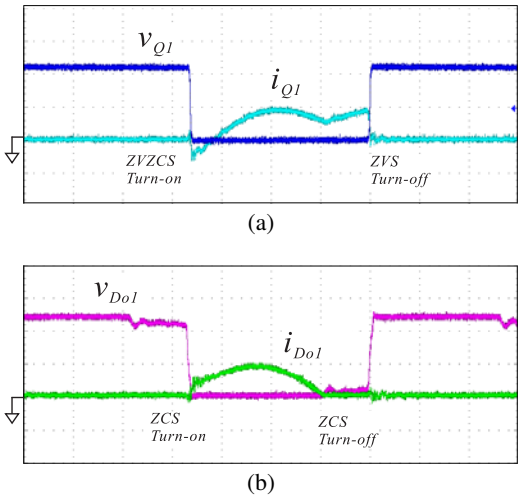


Fig. 15. Observed waveforms of the LLC-LC converter prototype at $f_s = 67$ kHz and $P_o = 0.5$ kW: (a) active switch Q_1, and (b) rectifying diode D_{o1} (100 V/div, 5 A/div, 2 μs/div).

The switching voltage and current waveforms for the open-circuit load condition are depicted in Fig. 16. ZVS commutations of the active switches due to i_m can be confirmed from those waveforms. Thus, it is verified the advantageous characteristics of the LLC converter can maintain in the LLC-LC converter.

The switching voltage and current waveforms for the short-circuit load condition are demonstrated in Fig. 17. The peak currents through the active switches and diodes are suppressed as less than the peak value of 20 A for the heavy load condition of Fig. 14 by setting f_s to f_{rp} while ZVS and ZCS operations still maintain. Furthermore, the switching currents, which are identical with the primary-side i_p, exhibit the 90 deg lagging-phase behavior, thereby the inductive impedance characteristics of the anti-resonant tank is actually confirmed.

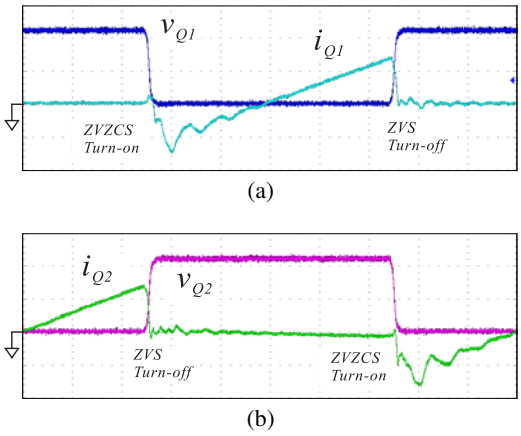


Fig. 16. Observed waveforms of the LLC-LC converter under the open-circuit load condition at $f_s = 100\,\mathrm{kHz}$: (a) active switch Q_1, and (b) active switch Q_2 ($100\,\mathrm{V/div}, 2\,\mathrm{A/div}, 1\,\mu\mathrm{s/div}$).

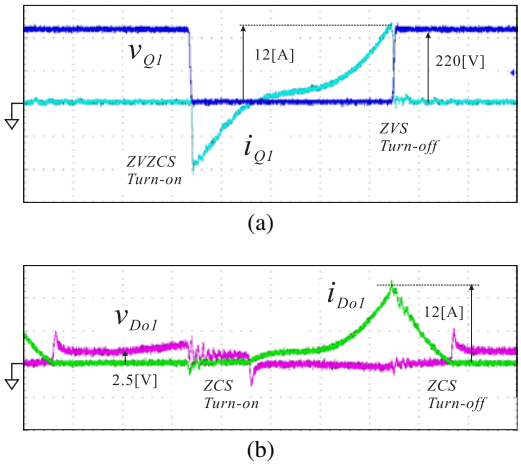


Fig. 17. Observed voltage and current waveforms of the LLC-LC converter under the short-circuit load condition at $f_s = 131\,\mathrm{kHz}$: (a) active switch Q_1 ($50\,\mathrm{V/div}, 5\,\mathrm{A/div}$, $1\,\mu\mathrm{s/div}$), and (b) rectifying diode D_{o1} ($5\,\mathrm{V/div}, 5\,\mathrm{A/div}$, $1\,\mu\mathrm{s/div}$).

The enlarged waveforms and voltage-current trajectory are revealed in Fig. 18 under the condition of full load (100 % output power). The ZVS & ZCS turn-on of the active switch is toward the critical condition around the full load because the switching frequency approaches gradually the second resonant frequency f_{rm}; the boundary point of inductive and capacitive load areas of the LLC-LC converter. However, the ZVS transitions can still maintain by adjusting the dead time interval, thereby no significant current surge appears at the turn-off transitions. Thus, the switching power losses are well reduced as compared to the hard switching behavior. The margin of inductive load area for the load power variations exhibits the trade-off relation between the ZVS performance and circulating current in the primary-side power stage. It should be noted here the small part of voltage and current overlapping in the first-quadrant of Fig. 18 (b) is due to charging of the parasitic output capacitance at the turn-off transition of power MOSFET.

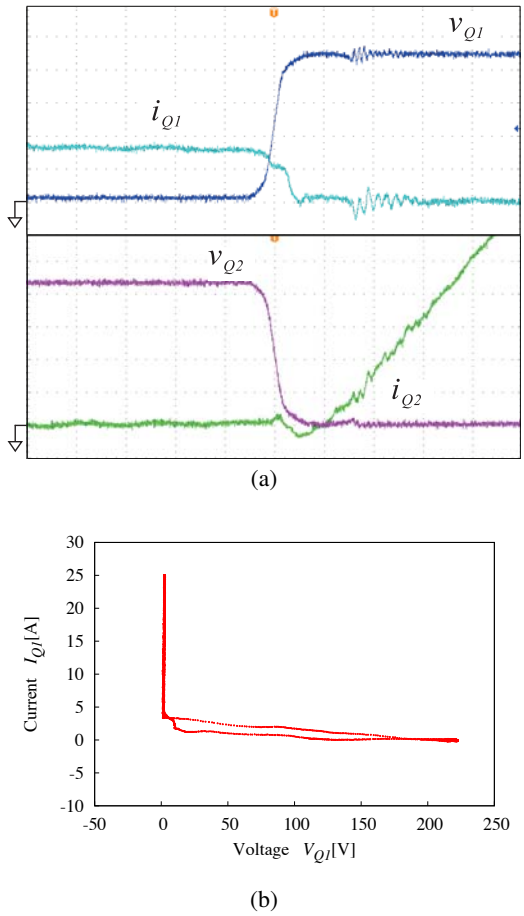


Fig. 18. Commutation of the active switch at the boundary of inductive and captive load areas at $f_s = 60\,\mathrm{kHz}$ and $P_o = 2.5\,\mathrm{kW}$: (a) switching waveforms ($50\,\mathrm{V/div}, 2\,\mathrm{A/div}, 200\,\mathrm{ns/div}$) and (b) voltage and current trajectory.

C. Steady-State Characteristics

The steady-state characteristics of the proposed converter are compared with the LLC converter under the open-loop control in experiment.

The measured steady-state characteristics of the LLC converter prototype are demonstrated in Fig. 19 for variations of R_o in compared with the simulation values. In the ZVS area 1 ($30\,\mathrm{kHz} \leq f_s \leq 90\,\mathrm{kHz}$), the voltage conversion ratio varies from 1.0 to 1.2 by changing f_s between 44 kHz to 86 kHz. Consequently the output power is regulated in the range of 1.0 kW–2.5 kW. In contrast to that, the voltage conversion ratio changes from 1.0 to 0.6 even by extending f_s from 86 kHz to 200 kHz in the ZVS area 2. Thus, the minimum output power is 0.65 kW (26 % output power) at $f_s = 200\,\mathrm{kHz}$ ($F_{rs} = 2.3$).

The measured steady-state characteristics of the LLC-LC converter are presented in Fig. 20 with the same parameters of R_o for the LLC converter. Compared to the results in Fig. 19, it can be understood that the wider range of output voltage and power as well as current can be controlled in the LLC-LC converter; $0.2 \leq M \leq 1.2$ and $0.1\,\mathrm{kW} \leq P_o \leq 2.5\,\mathrm{kW}$. In particular, the PFM adaptable range is successfully extended to

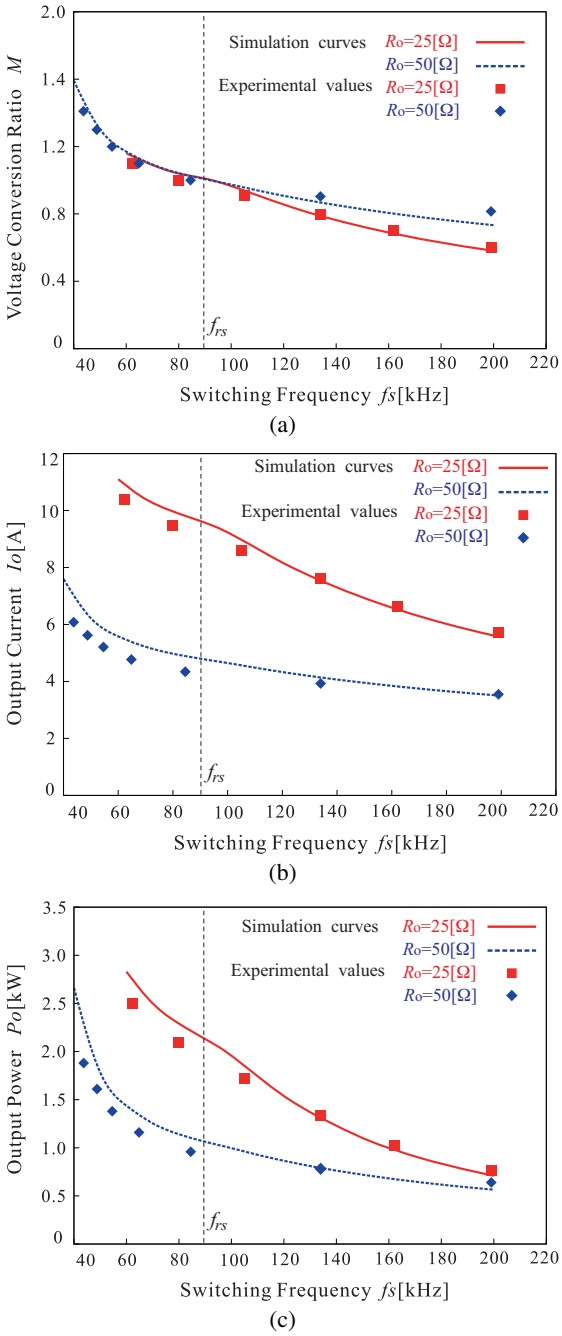


Fig. 19. Measured steady-state characteristics of the LLC converter under the open-loop control: (a) M–f_s, (b) I_o–f_s, and (c) P_o–f_s ($f_{rs} = 90\,\mathrm{kHz}$ and $f_{rm} = 30\,\mathrm{kHz}$).

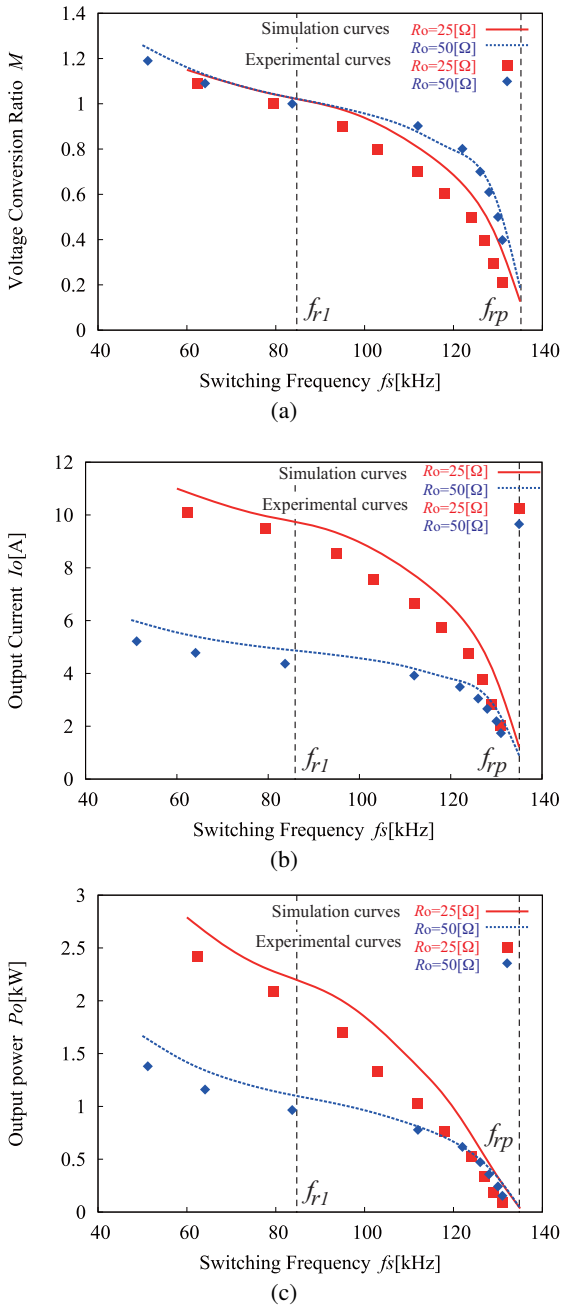


Fig. 20. Measured steady-state characteristics of the LLC-LC converter under the open-loop control: (a) M–f_s, (b) I_o–f_s, and (c) P_o–f_s ($f_{r1} = 86\,\mathrm{kHz}$, $f_{r2} = 27\,\mathrm{kHz}$, and $f_{rp} = 135$).

the ZVS area 2 with the smaller frequency variation 86 kHz–131 kHz, consequently the minimum output power is obtained as 0.1 kW (less than 10 % output power) at $f_s = 131\,\mathrm{kHz}$ ($F_{rs} = 1.5$). It might be hard to perform the voltage regulation practically around f_{rp} in the ZVS area 2 under the light load condition.

D. Actual Efficiency and Power Loss Analysis

The actual power conversion efficiencies of the LLC and LLC-LC converters are compared under the rated output voltage condition of $V_o = 240\,\mathrm{V}$ in Fig. 21. It should be remarked herein the soft switching operations (ZVS in Q_1-Q_4, and ZCS in D_{o1}-D_{o4}) can achieve through the whole output power in both the resonant converters. The maximum efficiency of the LLC-LC converter is measured at $P_o = 1.5\,\mathrm{kW}$ (60 % output power), and high efficiency over 95 % can be maintained in the power range 1 kW–2.5 kW (40 %–100 % output power) due to the wide range of soft switching operation. The efficiency drop from the LLC converter is suppressed within 0.4 % through the whole load power. It can be said no significant power loss emerges from the anti-resonant tank, thereby effectiveness of the design process which is introduced in Section IV is

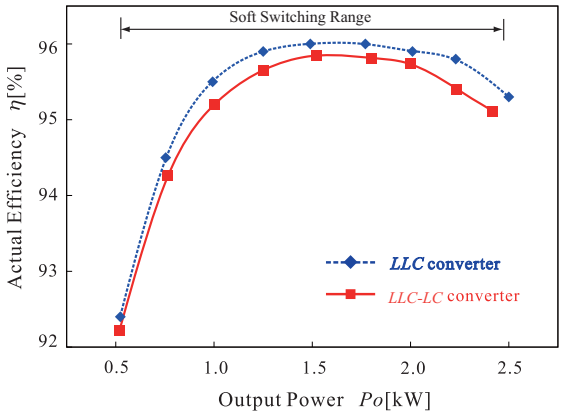


Fig. 21. Comparison on the actual efficiencies between LLC and LLC-LC converters ($V_o = 240\,\mathrm{V}$).

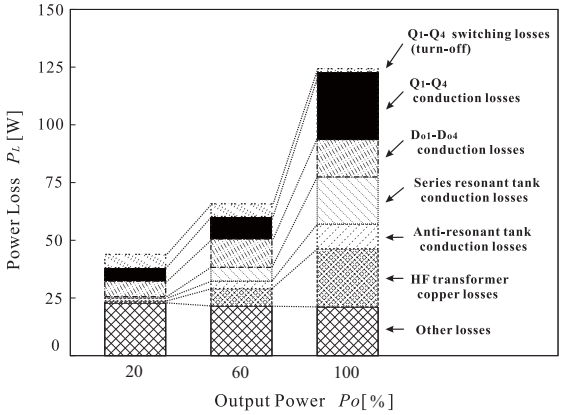


Fig. 22. Power loss analysis of the LLC-LC converter prototype ($V_o = 240\,\mathrm{V}$).

verified.

The power loss analysis of the LLC-LC converter prototype is depicted in Fig. 22. Note here the turn-on power loss of the active switch is neglected due to the ZVS & ZCS commutation, so is the turn-on power loss of rectifying diode due to the ZCS operation. The iron power loss of the HF planar transformer and wire copper loss of the prototype are included in the "Other losses". It can be observed from the power loss breakdown the turn-off power losses of $\mathrm{Q_1}$–$\mathrm{Q_4}$ keep in a low profile by the effect of ZVS, and the turn-off power losses of $\mathrm{D_{o1}}$–$\mathrm{D_{o2}}$ as well as the reverse recovery currents can also be minimized owing to the ZCS over the wide range of load power. The turn-off power loss at the full load condition which corresponds with the boundary of inductive and capacitive load regions accounts for a small part of the total amount as pointed out in Fig. 18. The conduction loss of the anti-resonant tank is measured 3 %–9 % of the total power loss at each output power setting when the converter operates in the ZVS area 1.

E. State-Plane Analysis of Resonant Tanks

The power and energy levels of each resonant tank can be portrayed by the state-plane trajectory, which helps to understand the proprieties of the LLC-LC resonant tanks.

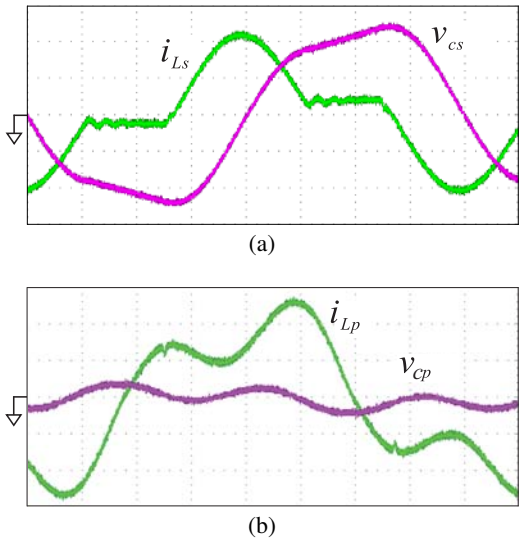


Fig. 23. Observed waveforms of the series and anti-resonant tanks in the LLC-LC converter at $P_o = 2\,\mathrm{kW}$, $M = 1.1$, and $f_s = 61\,\mathrm{kHz}$: (a) series resonant tank, and (b) anti-resonant tank ($100\,\mathrm{V/div}, 10\,\mathrm{A/div}, 2\,\mu\mathrm{s/div}$).

The observed voltage and current waveforms in the series and anti-resonant tanks are shown in Fig. 23 under the condition $P_o = 2\,\mathrm{kW}$, $f_s = 61\,\mathrm{kHz}$ and $M = 1.1$. The relevant state-plane trajectories of series and anti-resonant tanks are depicted in Fig. 24 as compared to the calculation result which is obtained from TABLE I and (16). Fig. 24 (a) exhibits the elliptical trace with respect to v_{cs}, which verifies the series resonance in the LLC-LC converter. Fig. 24 (b) displays the elliptical trace with respect to i_{Lp}, which represents the anti-resonance. The trajectory of Fig. 24 (a) is greater than that of Fig. 24 (b), accordingly it is proven the series resonant tank operates more effectively under the normal load condition.

The voltage and current waveforms of the series and anti-resonant tanks under the open-circuit load condition are depicted in Fig. 25. The state-plane trajectories corresponding to those waveforms are shown in Fig. 26. It can be confirmed from the results that the trajectories shrink both in the series and anti-resonant tanks as compared to those of the normal load condition in Fig. 24.

The voltage and current waveforms of the series and anti-resonant tanks under the short-circuit load condition are depicted in Fig. 27. In addition, the state-plane trajectories corresponding to those waveforms are shown in Fig. 28. It can be observed from those figures the trajectories of series resonant tank are reduced well under that of the normal load condition in Fig. 24 (a). On the other hand, the trajectories of the anti-resonant tank swell out as compared to those of Fig. 24 (b), which verifies the performance of the anti-resonant tank under the short-circuit load condition.

It should also be remarked in the state-plane analysis that no dc voltage appears in either v_{cs} or v_{cp} of Figs.24,26 and 28, accordingly high efficiency can keep through the entire load conditions in the LLC-LC converter.

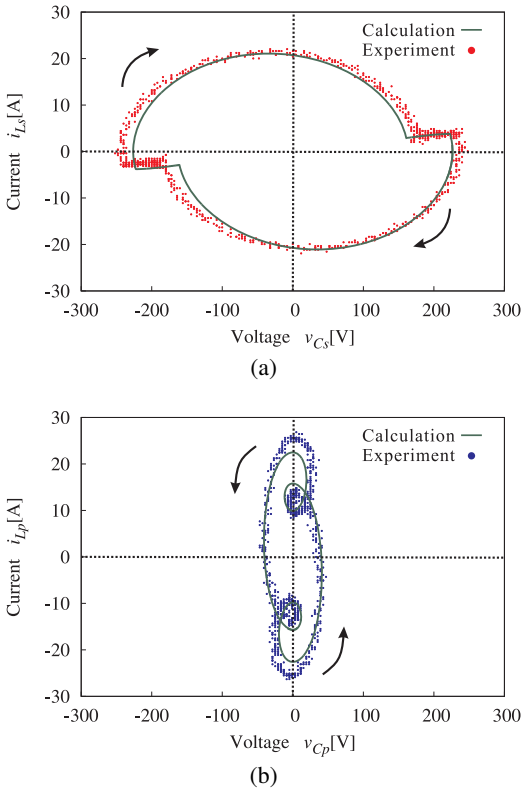


Fig. 24. Measured and calculated state-plane trajectories of the resonant tanks in the LLC-LC converter at $P_o = 2\,\mathrm{kW}$, $M = 1.1$, and $f_s = 61\,\mathrm{kHz}$: (a) series resonant tank, and (b) anti-resonant tank.

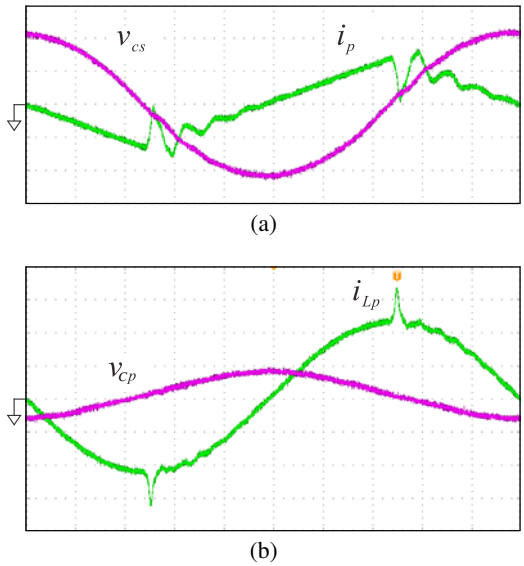


Fig. 25. Observed waveforms of the series and anti-resonant tanks under the open-circuit load condition at $f_s = 100\,\mathrm{kHz}$: (a) series resonant tank, and (b) anti-resonant tank ($10\,\mathrm{V/div}, 5\,\mathrm{A/div}$).

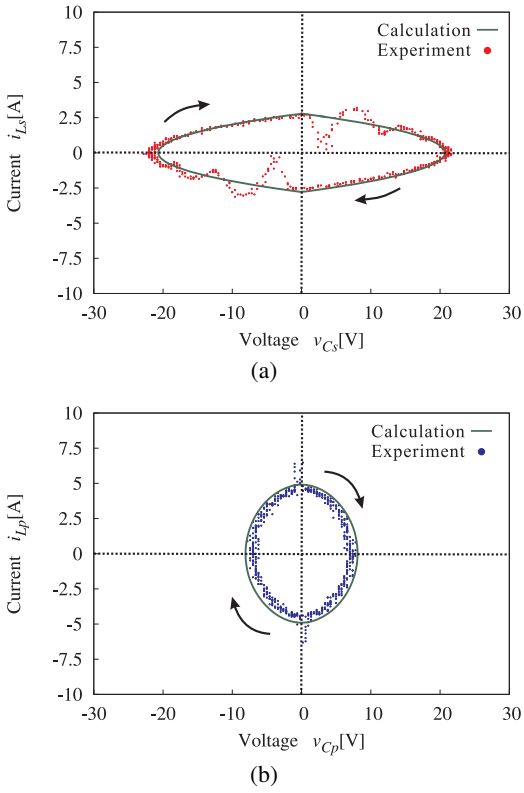


Fig. 26. Measured and calculated state-plane trajectories of the series and anti-resonant tanks under the open-circuit load condition: (a) series resonant tank, and (b) anti-resonant tank.

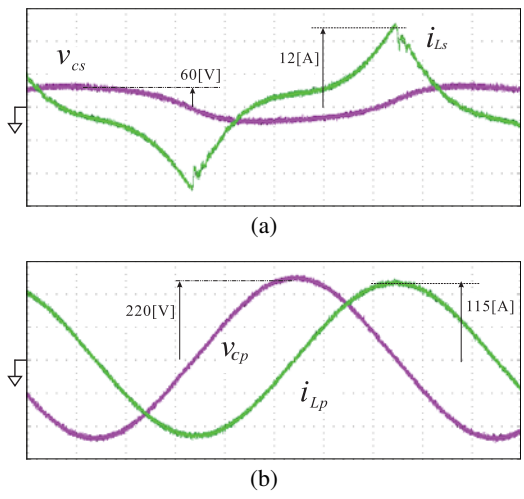


Fig. 27. Observed waveforms of the series and anti-resonant tanks under the short-circuit load condition at $f_s = 131\,\mathrm{kHz}$: (a) series resonant tank ($100\,\mathrm{V/div}, 5\,\mathrm{A/div}$), and (b) anti-resonant tank ($100\,\mathrm{V/div}, 50\,\mathrm{A/div}$).

VI. Conclusions

This paper presents a LLC-LC resonant soft-switching dc-dc converter with the sensitivity-improved PFM scheme. The over-current protection for the short-circuit load condition as well as a start-up interval can be ensured in a smaller band of switching frequency which is designed on the basis of the series and anti-resonant frequencies. The circuit topology and the PFM scheme are also effective for extending the voltage regulation area especially in the buck mode, which is advantageous for realizing a single-stage buck and boost

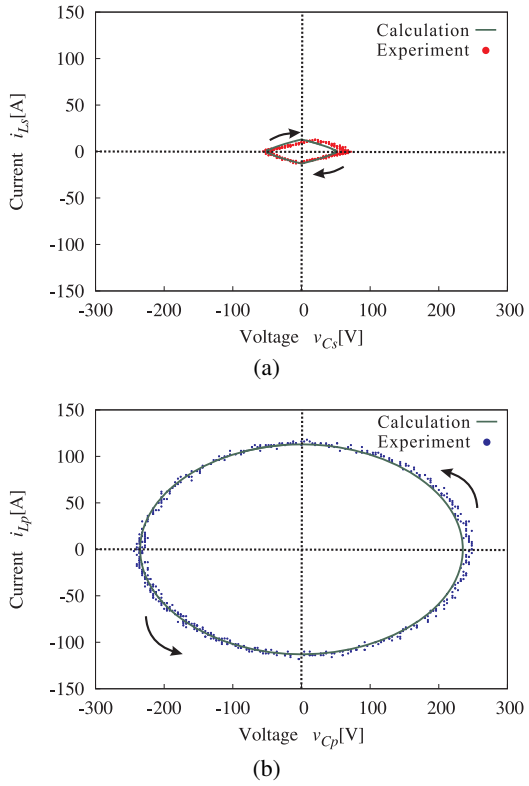


Fig. 28. Measured and calculated state-plane trajectories of the series and anti-resonant tanks under the short-circuit load condition: (a) series resonant tank, and (b) anti-resonant tank.

voltage regulations in the resonant converter.

The steady-state characteristics of a voltage conversion ratio and output power have been theoretically described in the frequency domain analysis with the FHA strategy. In addition, the design guideline of series and anti-resonant tanks as well as the resonant frequencies for the LLC-LC converter has been introduced with consideration for the input impedance and the resonant tank characteristics impedances.

The performances of the LLC-LC converter have been demonstrated in experiment of the $2.5\,\mathrm{kW}$ prototype under the open-loop control. The excellent characteristics of the proposed converter have been clarified as follows:

- A voltage conversion ratio M can be extended to the wider range between $M = 0.2$ and $M = 1.2$, thereby enlarging the output power regulation range between $2.5\,\mathrm{kW}$ and $0.1\,\mathrm{kW}$ in the LLC-LC converter. The voltage step-down ratio increases by triple, and the output power range can improve by $30\,\%$ as compared to a LLC converter.
- The current though the power devices and components under the short-circuit load condition are reduced $44\,\%$ as compared to the full load condition owing to the effect of the anti-resonant tank in the LLC-LC converter, where the anti-resonant frequency is designed in just $50\,\%$ higher than the first resonant frequency.
- Energy of the anti-resonant tank as well as the series resonant tank is visualized by the state-plane trajectories of the resonant inductor currents and resonant capacitor voltage. The observed trajectories actually demonstrate the practical effect of the anti-resonant tank, which helps to design the circuit parameters with consideration for the power loss in the resonant tanks.
- Wide-range soft commutations in the active switches and rectifier diodes attain from the full load ($Po = 2.5\,\mathrm{kW}$) to no load condition, keeping the same switching-performance as the LLC converter. This excellent property contributes for achievement of the maximum efficiency $95.9\,\%$ at $Po = 1.5\,\mathrm{kW}$, even by taking power consumption of the anti-resonant tank into account.
- The efficiency of the LLC-LC converter is comparative with the LLC converter, and it might be more advantageous over the two-stage LLC converter with a front-end dc voltage regulator.

Implementation of a high-performance controller and evaluations on the transitional behaviors of the LLC-LC converter will be a future challenge of this research.

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