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(Citation)
IEEE Transactions on Industrial Electronics,64(3):2054-2061

(Issue Date)
2017-03

(Resource Type)
journal article

(Version)
Accepted Manuscript

(URL)
https://hdl.handle.net/20.500.14094/90004791

ZVS Phase Shift PWM-Controlled Single-Stage Boost Full Bridge AC-AC Converter for High Frequency Induction Heating Applications

Tomokazu Mishima, *Senior Member*, *IEEE*, Shuichi Sakamoto, *Student Member*, *IEEE*, and Chiaki Ide

***Abstract*—This paper presents a new single-stage utility frequency ac (UFAC) – high frequency ac (HFAC) resonant power converter for high frequency induction heating(IH) applications. The newly-proposed ac-ac converter features a boost converter and full bridge resonant inverter integrated circuit with a source voltage sensorless control system. The experimental results of a $3.0\,\mathrm{kW}$-$40\,\mathrm{kHz}$ prototype are demonstrated on zero voltage soft switching (ZVS) and steady-state characteristics, then the validity of the proposed ac-ac converter is revealed from a practical viewpoint.**

***Index Terms*—AC-AC converter, boost full bridge (BFB), bridgeless, high frequency induction heating (IH), phase-shift pulse width modulation (PS-PWM), single-stage power conversion, zero voltage soft-switching (ZVS).**

I. Introduction

HIGH frequency induction heating (IH) has been widely applied to the industrial facilities such as metal surface heat treatment power supplies because of the partial heating capability and excellent response for load power variations as well as clean and pollution-less energy conversion [1]. Power loss reduction of the power converter stage is a preliminary requisite for the high efficiency of electrical-thermal energy conversion process.

Aimed at improving a power conversion efficiency, single-stage power converter topologies suitable for the IH applications have been developed last decade [2]- [7]. Fig. 1 schematically shows the multi-stage and single stage power conversions in the industrial IH applications.

All of the previously proposed single-stage ac-ac converters are based on a half-bridge voltage-fed resonant inverter. In particular, the boost half bridge (BHB) single-stage ac-ac converter as indicated in Fig 2, which is proposed in [6], has some attractive features such as a full bridge rectifier-less ("bridgeless") topology and power factor correction (PFC) of the utility current with the aid of a non-smoothed dc (NSDC) link. However, the voltage stress across the power device may increase under the higher load power condition due to the half-bridge structure. In addition, a voltage sensor for detecting the polarity of utility voltage is necessary for employing the asymmetrical pulse-width-modulation (PWM) as a power control strategy [3]- [6]. Consequently, power conversion efficiency of the main circuit may deteriorate under the higher power condition, and the simplicity as well as reliability of the controller cannot be ensured. The pulse-frequency-modulation (PFM) or pulse-density-modulation (PDM) is also available for the single-stage ac-ac converters [2], [5]. However, the circuit parameter design and selection might be involved with a complicated process for attaining the wide range of power regulation for IH loads as compared to the constant frequency PWM.

As a solution for overcoming the disadvantages of the BHB topology, a new single-stage boost full bridge (BFB) ZVS ac-

Manuscript received April 15, 2016; revised July 10, 2016; accepted August 2, 2016.

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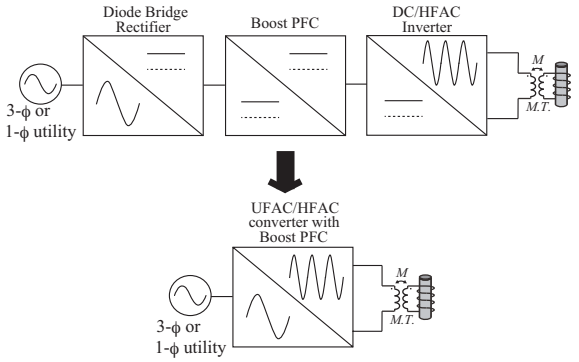


Fig. 1. Multi-stage and single-stage power conversion processes for industrial high frequency IH applications.

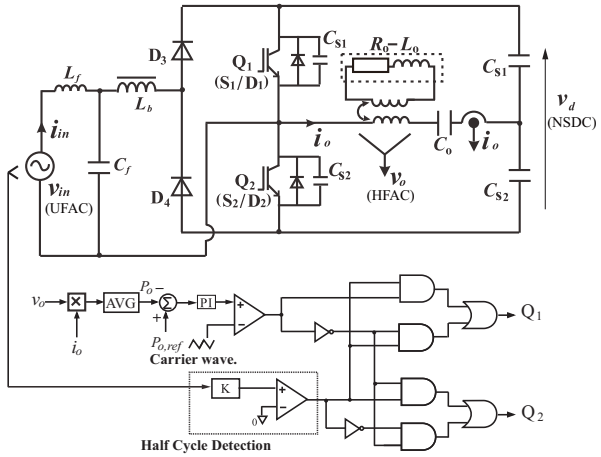


Fig. 2. ZVS PS-PWM single-stage BHB ac-ac converter [6].

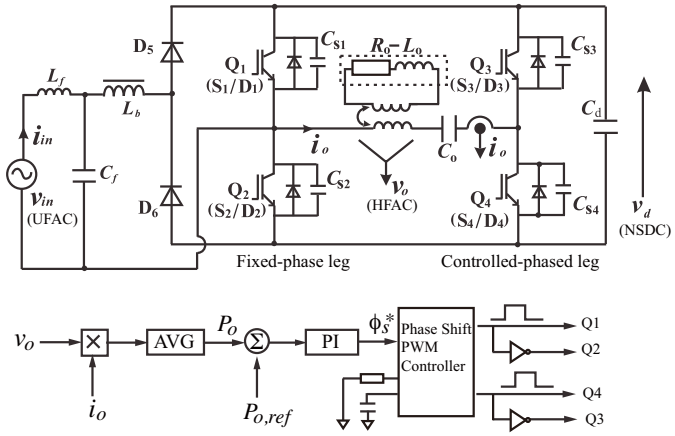


Fig. 3. Proposed ZVS PS-PWM single-stage BFB ac-ac converter.

ac converter controlled by the constant frequency PS-PWM is proposed in this paper. The remainder of this paper is organized as follows; the proposed circuit topology and its power control method are described together with the ZVS operating principle in Section II. The comparison between the BHB and BFB topologies are presented by a theoretical analysis in Section III. The feasibility of the proposed ac-ac converter is demonstrated by experiment results of a 3.0 kW-40 kHz prototype in Section IV, then the practical advantages are summarized in Section V.

II. Circuit Topology and Operation

A. Circuit Configuration and Power Control

The main circuit topology and control system of the proposed ac-ac converter are illustrated in Fig. 3. The theoretical voltage and current waveforms of the proposed ac-ac converter are displayed in Fig. 4. The main power consists of the boost converter (totem-pole bridgeless boost rectifier) and full bridge resonant inverter-integrated circuit topology "BFB" with the active switches Q_1–Q_4, while maintaining the bridgeless topology by Q_1–Q_2 and D_5–D_6. The inductor L_b contributes for boosting the utility voltage v_{in} under the high frequency switching condition of Q_1–Q_4. The lossless snubber capacitors C_{s1}–C_{s4} are implemented in parallel with Q_1–Q_4, thereby ZVS operation can achieve with the equivalent inductance of the IH load both at their turn-on and turn-off transitions. The switching frequency component is eliminated from the utility current i_{in} by the low-pass filter L_f-C_f.

The PS-PWM switch-gate signal patter applied into the proposed ac-ac converter is shown in Fig. 5. The output power of BFB can be regulated by the phase shift (PS)-PWM for Q_1–Q_4; the left side leg Q_1 / Q_2 operates as the fixed-phase (leading phase) switches, while the right side leg Q_4 / Q_3 performs as the controlled-phase (lagging phase) switches under the condition of constant and symmetrical on-duty ratio ($\simeq 50\,\%$ including the dead time t_d). The switching pulse patterns for Q_1–Q_4 depend upon the PS-PWM regardless of the polarity of v_{in}; the phase shift angle ϕ_s and its time interval $t_\phi\,(=\,T_s \cdot \phi_s/360\,^\circ)$ are regulated in the unique sequence through the whole UFAC cycle. Accordingly,

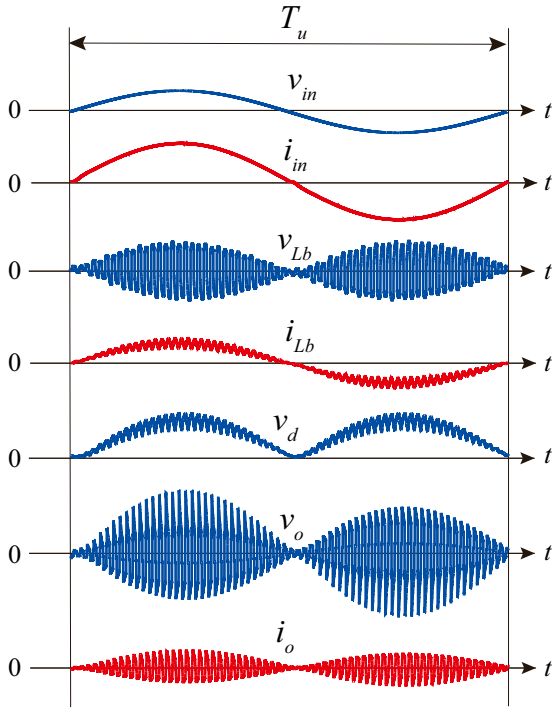


Fig. 4. Relevant voltage and current waveforms for one UFAC cycle.

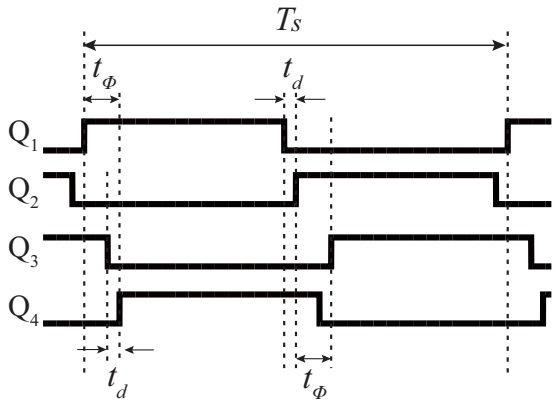


Fig. 5. PS-PWM pulse pattern for Q_1–Q_4.

a sensor for detecting the half cycles of v_{in} can be eliminated, which results in simplification of the system configuration as compared to the BHB topology.

The boost inductor current i_{L_b} sustains the continuous conduction mode (CCM) with the properly designed L_b [6]. Referring to Fig. 6, the volt-second balance of L_b yields the average value of the NSDC-link voltage v_d for the HFAC cycle as

$$\int_0^{T_s} v_{L_b}(t)dt = 0 \Rightarrow \overline{v_d} \simeq 2|v_{in}|. \tag{1}$$

This equation indicates the proposed BFB topology performs as the totem-pole bridgeless boost rectifier regardless of the control variable ϕ_s.

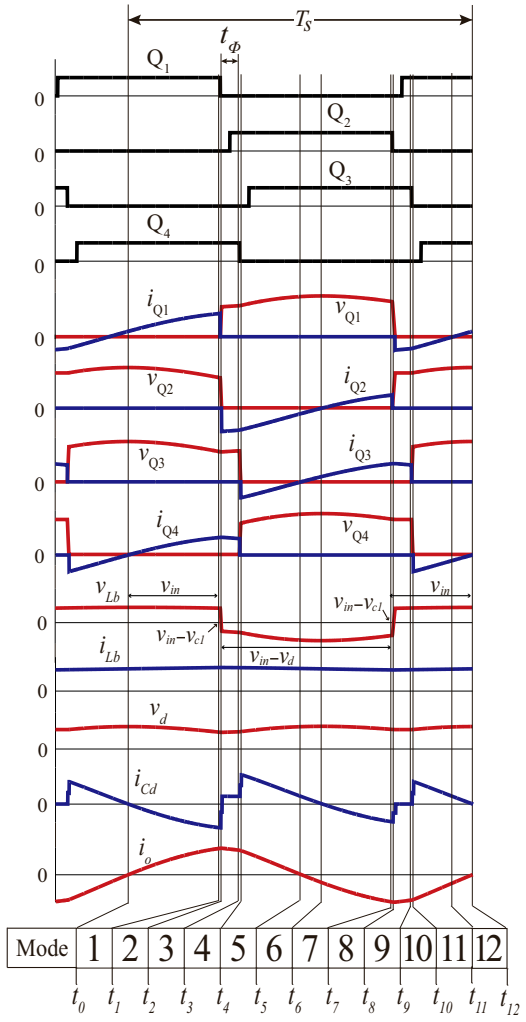


Fig. 6. Operating waveforms for a HFAC cycle ($v_{in} > 0$).

The output power P_o of the main circuit is expressed by

$$P_o = V_{o,u} I_{o,u} \cos\theta_u + V_{o,h1} I_{o,h1} \cos\theta_{h1} + \sum_{3,5,\ldots}^{\infty} V_{o,hn} I_{o,hn} \cos\theta_{hn}, \quad (2)$$

where the first, second and third terms represent twice the UFAC, the fundamental HFAC and its odd-numbered frequency components, respectively. The second term component primarily contributes for the high frequency heating, thereby the voltage and current are defined by RMS under the ideal condition as

$$V_{o,h1} = \frac{2\sqrt{2}V_{in}}{\pi} \cos\left(\frac{\phi_s}{2}\right), \quad I_{o,h1} = \frac{V_{o,h1}}{Z_o} \quad (3)$$

$$Z_o = \sqrt{{R_o}^2 + {X_o}^2}, \quad X_o = \omega_s L_o - \frac{1}{\omega_s C_o}, \quad (4)$$

where ω_s is the angular switching frequency. Therefore, the output power can be controlled by changing ϕ_s under the high frequency condition.

B. Switching Mode Transitions and ZVS Condition

The key operating waveforms during the one HF cycle are depicted in Fig. 6 for the positive half-cycle of v_{in}. In addition, the corresponding mode transitions and equivalent circuits are illustrated in Fig. 7 (a).

The proposed ac-ac converter is comprised of the twelve modes as explained below, where only the case of $v_{in} > 0$ is treated for the sake of paper length limitation. For the simplicity of discussion, the utility side filter L_f-C_f is neglected herein:

[Mode 1: steady-state power transfer] ($t_0 \leq t < t_1$) The active switches Q_1–Q_4 are on-state, and the UFAC source current i_{in} flows through the network of v_{in}–L_b–D_5–S_1. During this interval, the magnetic energy is stored in the boost inductor L_b. At the same time, the output current i_o flows through the network of S_1–R_o–L_o–C_o–S_4–C_d. During this interval, the NSDC-link capacitor C_d discharges.

[Mode 2: fixed-phase leg edge resonance] ($t_1 \leq t < t_2$) The active switch Q_1 is turned off at t_1, then the lossless snubber capacitors C_{s1}, C_{s2} and equivalent inductance L_o make the edge resonance. Accordingly, the voltage v_{Q_1} rises with a certain slope from zero, and the ZVS turn-off commutation starts in Q_1. At the same time, the voltage v_{Q_2} declines gradually from v_d.

[Mode 3: ZVS in Q_1 and ZVZCS in Q_2] ($t_2 \leq t < t_3$) The voltage v_{Q_1} reaches v_d at t_2, thereby the ZVS turn-off commutation is completed in Q_1. At the same time, the voltage v_{Q_2} decreases to zero, then the anti-parallel diode D_2 of Q_1 is foward-biased. The output current i_o flows through the network of S_4–D_2–R_o–L_o–C_o. During this interval, the gate signal is supplied to S_2, whereby zero voltage and zero current soft switching (ZVZCS) turn-on can be performed in Q_2.

[Mode 4: controlled-phase leg edge resonance] ($t_3 \leq t < t_4$) The active switch Q_4 is turned off at t_3, then the lossless snubber capacitors C_{s3}, C_{s4} and the IH load inductance L_o create the edge resonance. Accordingly, the voltage v_{Q_4} rises with a certain slope from zero voltage, and ZVS turn-off operation in Q_4 starts. At the same time, the voltage v_{Q_3} decline gradually from v_d.

[Mode 5: ZVS in Q_4 and ZVZCS in Q_3] ($t_4 \leq t < t_5$) The voltage v_{Q_4} reaches v_d at t_4, thereby ZVS turn-off operation in Q_4 is completed. At the same time, the voltage v_{Q_3} reaches zero, accordingly the anti-parallel diode D_3 of Q_3 is forward-biased. The output current i_o flows through the network of D_3–C_d–D_2–R_o–L_o–C_o. During this interval, the gate signal is supplied to S_3, whereby the ZVZCS turn-on commutation can be performed in Q_3.

[Mode 6: controlled-phase Q_3 naturally commutated] ($t_5 \leq t < t_6$) The current through Q_3 commutates naturally from D_3 to S_3 at t_5 due to the edge resonance. Accordingly, the output current i_o reverses its polarity, and the boost inductor L_b releases the magnetic energy to the NSDC-link capacitor C_d.

[Mode 7: steady-state power transfer] ($t_6 \leq t < t_7$) The NSDC-link capacitor C_d begins to discharge and supply power to the IH load as well as v_{in}.

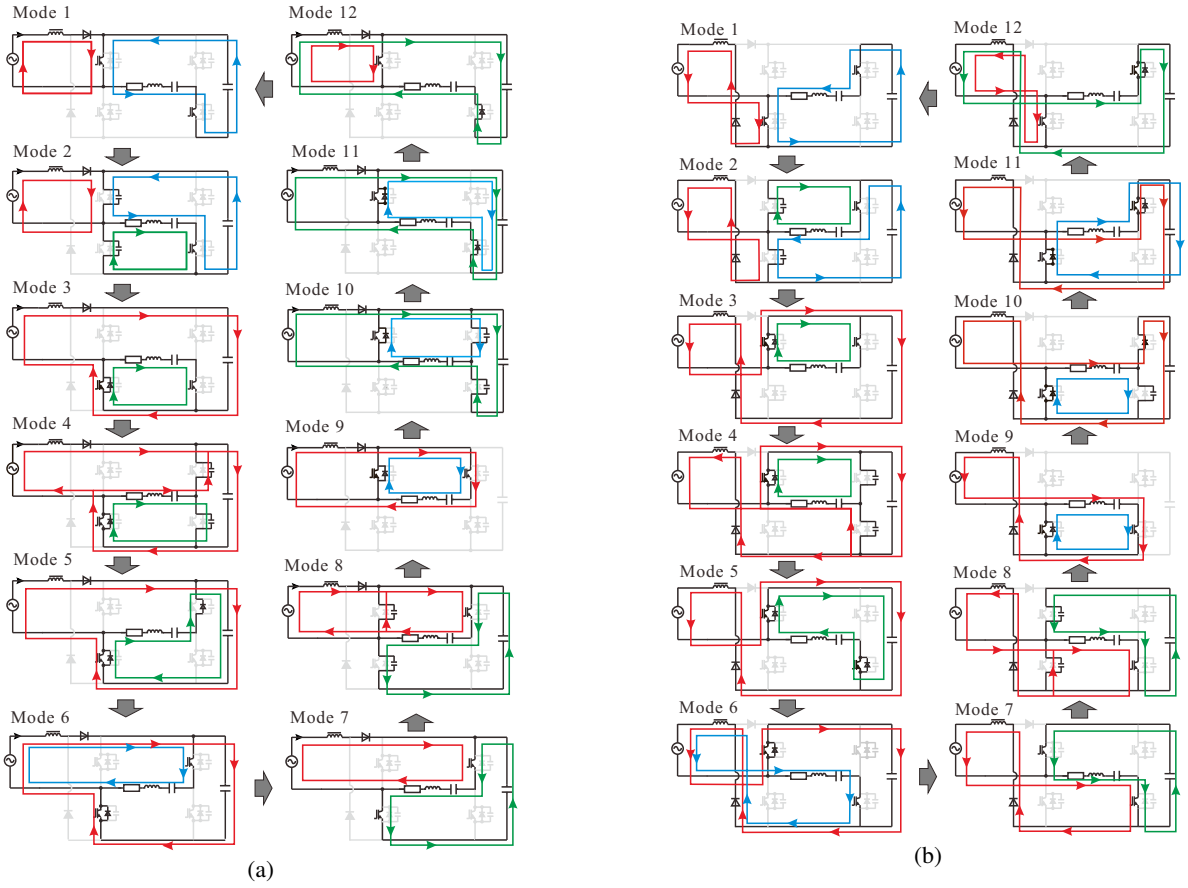


Fig. 7. Switch-mode transitions and equivalent circuits: (a) $v_{in} > 0$, and (b) $v_{in} < 0$

[Mode 8: fixed-phase leg edge resonance] ($t_7 \leq t < t_8$) The active switch Q_2 is turned off at t_7, accordingly the lossless snubber capacitors C_{s1}, C_{s2} and the IH load inductance L_o make the edge resonance. The voltage v_{Q_2} rises with a certain slope from zero, and ZVS turn-off operation in Q_2 starts. At the same time, the voltage v_{Q_1} declines gradually from v_d.

[Mode 9: ZVS in Q_2 and ZVZCS in Q_1] ($t_8 \leq t < t_9$) The voltage v_{Q_2} reaches v_d at t_8, and ZVS turn-off operation in Q_2 is completed. At the same time, the voltage v_{Q_1} reaches zero, then the anti-parallel diode D_1 of Q_1 is forward-biased. Accordingly, i_o flows through the network of D_1–S_3–C_o–L_o–R_o. During this interval, the gate signal is supplied to Q_1, the ZVZCS turn-on can be performed in Q_1.

[Mode 10: controlled-phase leg edge resonance] ($t_9 \leq t < t_{10}$) The active switch Q_3 is turned off at t_9, then the lossless snubber capacitors C_{s3}, C_{s4} and equivalent effective inductor L_o make the edge resonance. Accordingly, the voltage v_{Q_3} rises with a certain slope from zero voltage, and the ZVS turn-off operation in Q_3 starts. At the same time, the voltage v_{Q_4} declines gradually from v_d.

[Mode 11: ZVS in Q_3 and ZVZCS in Q_4] ($t_{10} \leq t < t_{11}$) The voltage v_{Q_3} reaches v_d at t_{10}, and ZVS turn-off operation in Q_3 is completed. At the same time, the voltage v_{Q_4} reaches zero. Accordingly, the output current i_o reverses its polarity and flows through the network of D_4–C_o–L_o–R_o–v_{in}–L_b–D_5–C_d. During this interval, the gate signal is supplied to S_4, whereby the ZVZCS turn-on can attain in Q_4.

[Mode 12: fixed-phase Q_1 naturally commutated] ($t_{11} \leq t \leq t_{12}$) The current through Q_1 commutates naturally from D_1 to S_1 at t_{11} due to the edge resonance. Consequently, the boost inductor L_b begins to store the magnetic energy from v_{in}. The output current i_o changes its polarity at t_{12}, and the circuit operation initiates the next cycle from Mode 1.

In case of the negative half-cycle of v_{in}, the conduction pathways interchange between Q_1 and Q_2, Q_4 and Q_3, C_{s1} and C_{s2}, C_{s4} and C_{s3}, respectively as drawn in Fig 7 (b).

The ZVS conditions of Q_1-Q_4, which depend on the instantaneous value of v_{in} well as the phase shift angle ϕ_s, i.e. output power, are expressed as

$$i_{Q1,off} > \frac{v_{Q2,off}}{Z_{r,fixed}}, \quad i_{Q2,off} > \frac{v_{Q1,off}}{Z_{r,fixed}} \tag{5}$$

$$Z_{r,fixed} = \sqrt{\frac{L_o}{C_{s1} + C_{s2}}} \tag{6}$$

$$i_{Q3,off} > \frac{v_{Q4,off}}{Z_{r,cont.}}, \quad i_{Q4_o ff} > \frac{v_{Q3,off}}{Z_{r,cont.}} \tag{7}$$

$$Z_{r,cont.} = \sqrt{\frac{L_o}{C_{s3} + C_{s4}}}, \tag{8}$$

where $i_{Q1,off}$–$i_{Q4,off}$ are the switch currents at the turn-off transitions, and $v_{Q1,off}$–$v_{Q4,off}$ are the voltages of the counter-side switches, respectively. The controlled-phase currents $i_{Q3,off}$,$i_{Q4,off}$ are smaller than the fixed-phase $i_{Q1,off}$,$i_{Q2,off}$ due to the PS-PWM principle. Therefore, the resonant characteristics impedances are set as $Z_{r,cont.} >$

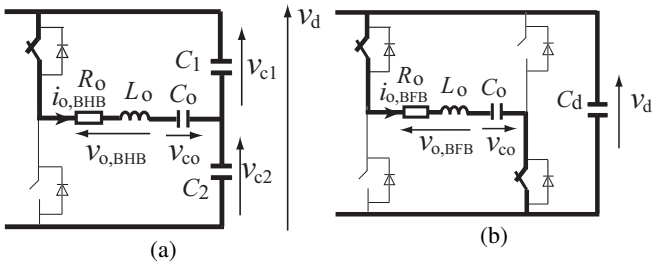


Fig. 8. Series load resonant networks: (a) BHB and (b) BFB topologies.

$Z_{r,fixed}$ for extending the ZVS range of Q_3 and Q_4 without any auxiliary circuits and dead time control.

III. Comparison of Voltage and Current Ratings

The series load resonant networks of the BHB and BFB topologies are depicted in Fig. 8. The inductive load voltages of the BHB and BFB topologies, $v_{o,BHB}$, $v_{o,BFB}$ can be respectively expressed as

$$v_{o,BHB}(t) = v_{c1} + v_{co} \tag{9}$$

$$v_{o,BFB}(t) = v_d + v_{co}. \tag{10}$$

The output currents of the BHB and BFB topologies, $i_{o,BHB}$, $i_{o,BFB}$ can be written respectively as

$$i_{o,BHB}(t) = C_{r1}v_{c1}(0)e^{-\alpha(t)}\left(\gamma_1 - \frac{\alpha}{\gamma_1}\right)\sin\gamma_1 t \tag{11}$$

$$\alpha = \frac{R_o}{2L_o}, \gamma_1 = \sqrt{\left(\frac{1}{\sqrt{L_oC_{r1}}}\right)^2 - \alpha^2}, C_{r1} = \frac{C_oC_1}{C_o + C_1} \tag{12}$$

$$i_{o,BFB}(t) = C_{r2}v_d(0)e^{-\alpha(t)}\left(\gamma_2 - \frac{\alpha}{\gamma_2}\right)\sin\gamma_2 t \tag{13}$$

$$\gamma_2 = \sqrt{\left(\frac{1}{\sqrt{L_oC_{r2}}}\right)^2 - \alpha^2},\ C_{r2} = \frac{C_oC_d}{C_o + C_d}, \tag{14}$$

where $v_{c1}(0)$ and $v_d(0)$ denote the initial capacitor voltages.

The ratios of output voltages and currents for the two topologies are obtained from (9), (10), (11), and (13) under the condition of equal natural angular frequency $\gamma_1 = \gamma_2$ as

$$\frac{v_{o,BFB}}{v_{o,BHB}} = \frac{1}{1 - \frac{v_{c2}}{v_d + v_{co}}} > 1 \tag{15}$$

$$\frac{i_{o,BFB}}{i_{o,BHB}} = \frac{1}{1 - \frac{v_{c2}}{v_d}} > 1. \tag{16}$$

Considering the voltage stress of each switch is equal to the NSDC-link voltage v_d in both the BHB and BFB topologies, it can be understood from (15) and (16): i) the output power can increase effectively in the BFB topology under the same NSDC-link voltage, and ii) the voltage stress of switches can be reduced in the BFB topology for the same output power.

IV. Experimental Verification

The feasibility of the proposed ac-ac converter is verified by experiment of a laboratory prototype. The exterior appearance of the prototype assembly is shown in Fig. 9. The circuit parameters and experimental condition are as follows: utility source voltage $v_{in} = 150\,\mathrm{Vrms}$, output power rating $P_{o,rate} = 3.0\,\mathrm{kW}$, utility frequency $f_u = 60\,\mathrm{Hz}$, switching frequency $f_s = 40\,\mathrm{kHz}$, series resonant frequency $f_r = 25\,\mathrm{kHz}$, boost inductor $L_b = 500\,\mu\mathrm{H}$, utility filter inductor $L_f = 200\,\mu\mathrm{H}$, utility filter capacitor $C_f = 750\,\mathrm{nF}$, lossless snubber capacitors (fixed-phase leg) $C_{s1} = C_{s2} = 22\,\mathrm{nF}$, lossless snubber capacitors (controlled-phase leg) $C_{s3} = C_{s4} = 18\,\mathrm{nF}$, NSDC-link film capacitor $C_d = 4\,\mu\mathrm{F}$, and series resonant capacitor $C_o = 3\,\mu\mathrm{F}$. A ferromagnetic steel object is adopted for the IH load with its equivalent resistance $R_o = 1.2\,\Omega$ and equivalent inductance $L_o = 24\,\mu\mathrm{H}$. The active switches Q_1–Q_4 are implemented with high-frequency switching IGBT modules (CM100DUS-12F, 600 V, 60 A) suitable for IH applications, while fast recovery diodes (DSEI 2x31-06C, 600 V, 60 A) are adopted for D_5 and D_6.

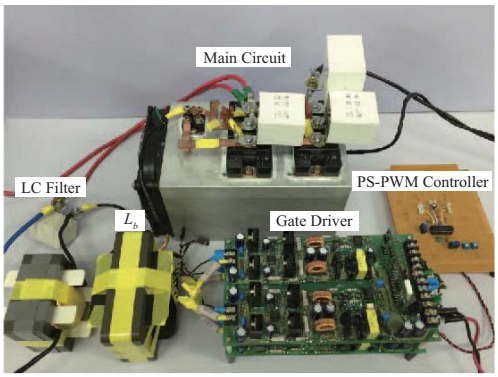


Fig. 9. Exterior appearance of the proposed converter prototype.

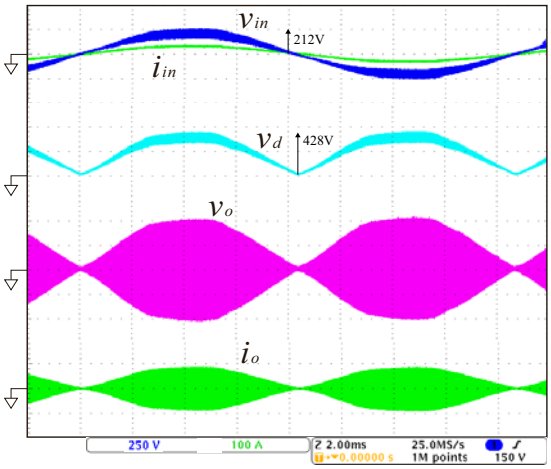
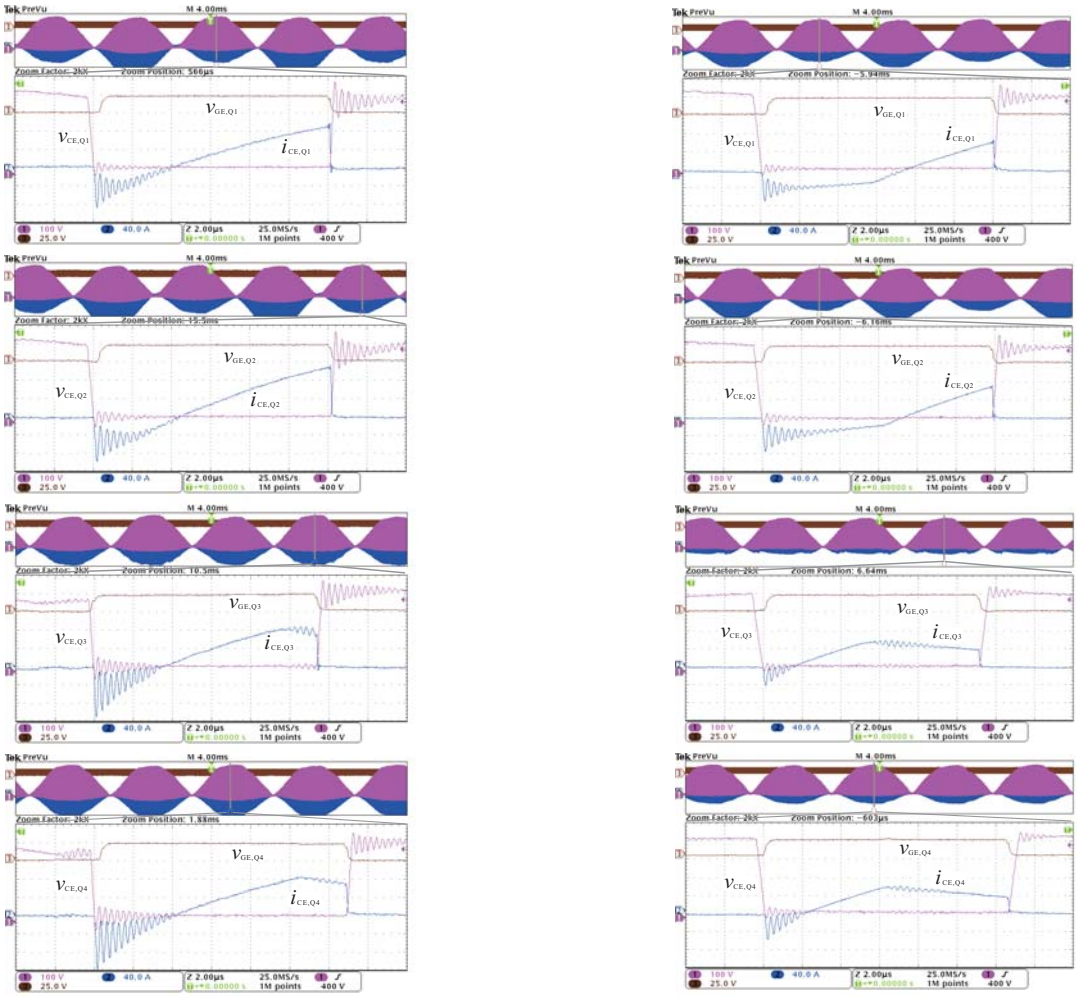


Fig. 10. Observed waveforms for the UFAC-HFAC power conversion(250 V/div, 100 A/div, 2 ms/div).

A. Operating Waveforms for UFAC and HFAC Cycles

The key waveforms for the UFAC cycle are depicted in Fig. 10. The single-stage power conversion from UFAC to HFAC can be observed under the condition of PFC. The boost operation can also be confirmed as indicated in v_{in} and v_d.

The enlarged collector-emitter voltage and current waveforms of Q_1–Q_4 are indicated at their turn-on and turn-off



(a) (b)

Fig. 11. Switching waveforms of Q_1–Q_4 at $v_{in,peak} = 212\,\mathrm{V}$: (a) $\phi_s = 30\,^\circ$ and $P_o = 2.8\,\mathrm{kW}$, (b) $\phi_s = 90\,^\circ$ and $P_o = 1.4\,\mathrm{kW}$ ($v_{GE,Qx}$: $25\,\mathrm{V/div}$, $v_{CE,Qx}$: $100\,\mathrm{V/div}$, $i_{CE,Qx}$: $40\,\mathrm{A/div}$, $2\,\mu\mathrm{s/div}$).

transitions with the gate-emitter voltages in Fig. 11. All the switching transitions are evaluated at the peak source voltage $v_{in,peak} = 212\,\mathrm{V}$, where the ZVS condition is most critical for satisfying (5) and (7). The collector-emitter voltage falls and rises gradually at both the transitions. No residual voltage, which refers to [6], appears in the lossless snubber capacitors, accordingly ZVZCS turn-on and ZVS turn-off operations can be achieved over the wide range of ϕ_s.

B. Steady-State Characteristics

The output power characteristics are displayed under the open loop control in Fig. 12, which exhibits the validity of the PS-PWM-based power regulation for the proposed ac-ac converter. The ZVS operations of Q_1 and Q_2 are observed in the whole power range while those of Q_3 and Q_4 are confirmed in the power range $1.4\,\mathrm{kW}$–$3.0\,\mathrm{kW}$ as proven in Fig 11.

The HFAC cycle averages of the NSDC-link voltage are evaluated at $v_{in,peak} = 212\,\mathrm{V}$, and the measured characteristics are shown in the Fig. 13. As expressed in (1), the NSDC-link voltages are regulated at almost two times as high as $v_{in,peak}$ regardless of the PS angle. Thus, the validity of (1) is clearly proven herein.

The actual efficiency curve of the proposed BFB topology is shown in Fig.14, compared with the BHB topology of the same power rating [6]. The maximum efficiency records as $97.1\,\%$ at $P_o = 3.0\,\mathrm{kW}$ in the BFB topology. It is also verified that the proposed BFB topology is more suitable for the higher power conditions. In this comparison, the source voltage v_{in} is set to $150\,\mathrm{Vrms}$ in the BFB converter while that of the previously developed BHB prototype is $200\,\mathrm{Vrms}$ for evaluating the efficiency under the fair condition of power rating. Therefore, it is worth noting that the efficiency of the BFB prototype will increase furthermore through the whole range of output power under the condition of the equivalent source voltage.

V. Conclusion

The new soft-switching PWM-controlled single-stage ac-ac coveter with a BFB topology has been proposed for the single-phase industrial IH applications, and its performances have been demonstrated by experiment of a prototype.

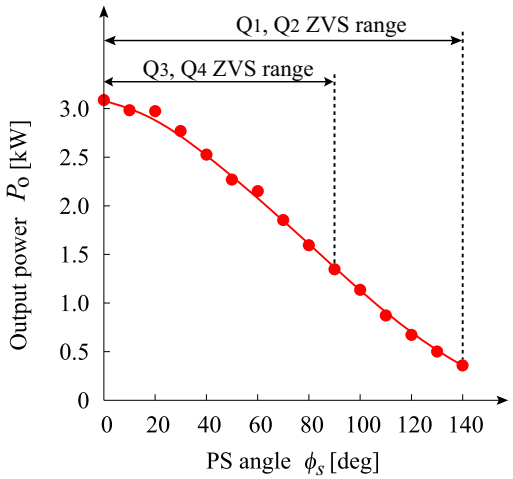


Fig. 12. Measured steady-state characteristics of output power regulation versus PS angle with the open loop control.

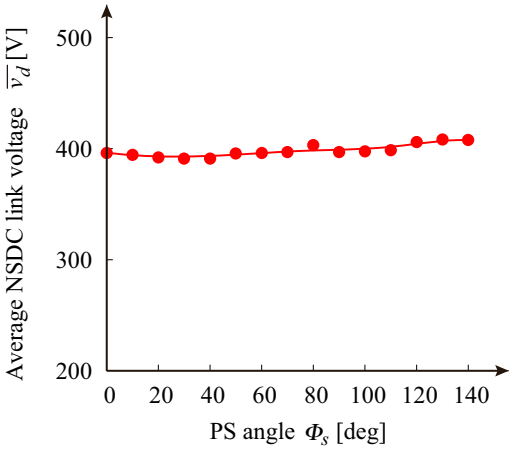


Fig. 13. Measured steady-state characteristics of the average NSDC-link voltage versus PS angle at $v_{in,peak} = 212\,\mathrm{V}$.

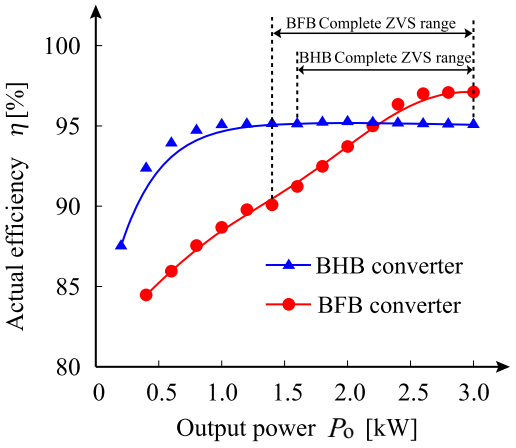


Fig. 14. Actual efficiency curves ($v_{in} = 150\,\mathrm{Vrms}$ for BFB, $v_{in} = 200\,\mathrm{Vrms}$ for BHB).

The wide-range ZVS operation and high frequency power regulation based on the PS-PWM scheme have been proven by the measured characteristics, and the single-stage UFAC-HFAC power conversion with boost PFC has been clarified by the observed waveforms. It has been originally demonstrated that the BFB topology is quite effective for improving a power conversion efficiency in the higher output power with the source voltage sensorless controller; The high-reliability and cost-effective power converter can be expected widely for the industrial IH systems.

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