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High-Frequency Bridgeless Rectifier-based ZVS Multi-Resonant Converter for Inductive Power Transfer Featuring High-Voltage GaN-HFET

Tomokazu Mishima, *Senior Member*, *IEEE*, and Eitaro Morita

***Abstract*—This paper presents a novel zero voltage soft-switching (ZVS) bridgeless active rectifier-based multi-resonant dc-dc power converter with high breakdown-voltage Gallium Nitride Heterojunction-Field-Effect-Transistor (GaN-HFET) for inductive power transfer (IPT) systems. The excellent performances such as high efficiency, low switching noises and normally-off operation are originally demonstrated in experiment of a $700\,\mathrm{W}$ prototype by comparing with a Si super-junction (SJ)-MOSFET-based prototype under the fair condition of voltage and current ratings. It is revealed from the experimental the low resistance and high speed operation of the GaN power transistor is effective for improving the power and energy conversions in IPT systems.**

***Index Terms*—high-frequency bridgeless rectifier (HF-BLREC), high-frequency resonant inverter (HF-R INV), inductive power transfer (IPT), Gallium Nitride Heterojunction-Field-Effect-Transistor (GaN-HFET), synchronous rectification (SR), zero voltage soft-switching (ZVS).**

Nomenclature

- f_s : Switching frequency of active switches
- f_{r1} : Resonant frequency of sending-side series compensation circuit
- f_{r2} : Resonant frequency of receiving-side series compensation circuit
- D : ON duty cycle of secondary-side switches
- L_1 : Self-inductance of sending coil
- L_2 : Self-inductance of receiving coil
- M : Mutual inductance of sending and receiving coils
- L_r : Leakage inductance of high-frequency transformer model (see in Fig. 7)
- L_m : Magnetizing inductance of high-frequency transformer model (see in Fig. 7)
- k : Coupling coefficient (see in Fig. 7)
- R_{ac} : Equivalent load ac resistance
- ω_s : Angular switching frequency ($\omega_s = 2\pi f_s$)
- ω_1 : Resonant angular frequency in power transfer intervals
- ω_2 : Natural angular frequency of simplified equivalent circuit (see in Fig. 9)
- ω_3 : Resonant angular frequency in circulating intervals
- I_p : RMS current of sending coil
- I_s : RMS current of receiving coil

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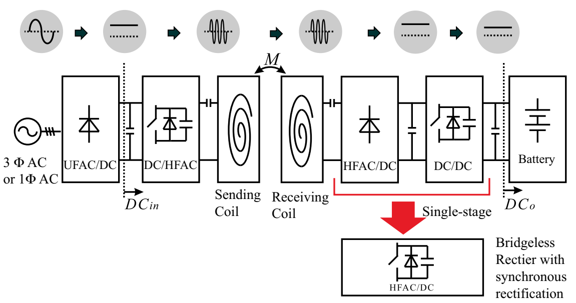

Fig. 1. Power and energy conversion process for vehicular and mobility battery charger applications.

I. Introduction

THE IPT systems have drawing much attention in a wide variety of industrial and automotive, and transportation electric power applications such as battery chargers in Automated Guided Vehicle (AVG), Electric Vehicles and railways these days [1]– [8]. A high frequency resonant inverter (HF-R INV) [9] as drawn in Fig. 1 generates resonant current to the sending coils. The output frequency depends on the switching frequency which is based on industry science medical (ISM) band, so that $85\,\mathrm{kHz}$ is applied for kW-class IPT systems while $13.56\,\mathrm{MHz}$ and its integer multiples for low power applications such as home appliances. Reduction of switching and conduction power losses is the most critical concern of technology for a high efficiency in the IPT systems.

The conventional circuit configuration for the receiving coil comprises of the diode rectifier and dc-dc converter for accommodating a wide range of the battery voltage variation. The two stage power converter induces a large amount of power dissipations, then deteriorates the power conversion efficiency. An effective solution for the technical problem is to employ an active rectifier for the secondary side as reported in [10]- [12], which is truly beneficial due to the less number of switches and components.

Wide-band-gap (WBG) power devices, especially, enhancement-mode (e-mode) normally-off GaN power transistors are promising semiconductor power devices for improving the converter efficiency by superseding a super junction (SJ) power MOSFET. The cascode-type GaN power transistors have been evaluated in LLC resonant power converters for switching power supplies [13] and buck

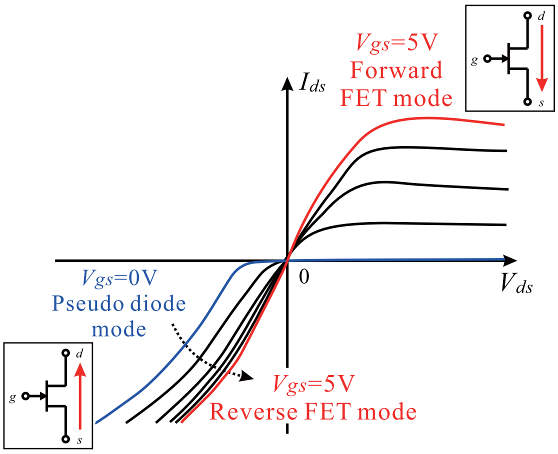

Fig. 2. Static voltage-current characteristics in the forward and reverse FET modes.

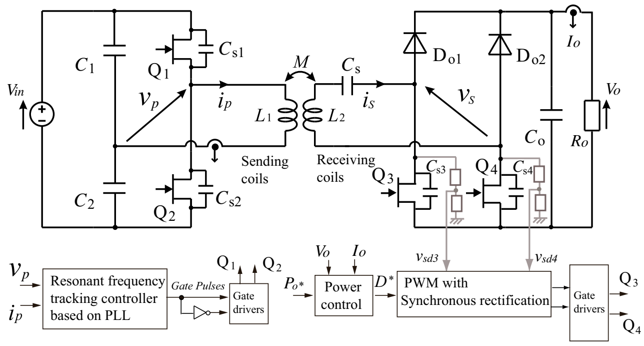

Fig. 3. Proposed IPT-ZVS converter topology and control system.

converters. The stray inductance within the two dies induces the parasitic ringing at the switching transitions, which results in emission of radiation noises. The low-voltage e-mode GaN power transistor has also been applied into synchronous rectifier in LLC dc-dc converters and non-isolated buck converters [14], however evaluation of the high voltage type in the practical converter has not yet been matured.

The e-mode GaN-HFET with a high voltage rating such as 600 V is effective for application of voltage-source HF-R INV with the minimized stray inductances within the die chip. In particular, a 600 V GaN-HFET has been developed in the past decades [15] [16], which has attractive features such as high breakdown voltage and fast speed, and current-collapse-free in addition to zero-reverse-recovery switching performance. The low on-resistance of GaN-HFET is truly attractive for the active rectifier of IPT from the viewpoint of low conduction losses as illustrated in Fig. 2. The GaN-HFET of the tree-pin packages such as TO-220 and TO-247 suffer from the lead inductances around the gate and drain loop [17]. These stray inductances induce high dv/dt rate and surge voltages, which damages the GaN-HFET with a low threshold gate-source voltage. The lossless snubber capacitor-assisted edge resonant switching technique is quite effective for suppressing the hard-switching commutation by the complete edge resonant zero-voltage-soft switching (ZVS) for the high-voltage GaN-HFET even with a small and nonlinear output capacitance [18]. It should be notated that ZVS is defined as the slow dv/dt at the turn-off transition while the zero voltage instant for the turn-on transition.

The high-frequency ac (HFAC)-linked bridgeless active rectifier has unique operating principle and control scheme which have no similarity with a conventional bridgeless power-factor-correction (PFC) converter and a totem-pole rectifier interfacing with an utility-frequency ac (UFAC) power source [19]. A secondary-side phase shift-controlled HF active rectifier has been proposed in [20]. However, the phase-shift is not suitable for synchronous rectification (SR), thus hard to reduce the conduction power losses in the e-mode GaN-HFET rectifier. In addition, any communication of the control signal between the primary-side and secondary-side circuits is necessary for performing the secondary-side phase-shift PWM, which might cause complexity of controller design for IPT systems.

This paper presents a new GaN FET-applied ZVS edge- and load-resonant (multi-resonant) dc-dc converter for IPT applications. The lossless snubber-assisted GaN-HFET half-bridge HF-R INV and HF bridgeless rectifier (BLREC) are employed for IPT sending and receiving coils. The proposed circuit topology enables the dual control methodology between the sending and receiving coils; pulse frequency modulation (PFM) in the HF-R INV for the resonant frequency tracking, and pulse width modulation (PWM) hybridized with SR in the HF-BLREC for adjusting the input and load impedances as optimum values. The advanced feature of the GaN-HFET for the IPT converter exists in the low ON-resistance and low gate charge that are superior to SJ-MOSFET in the equivalent voltage rating.

The rest of this paper is organized as follows: The circuit topology and operating principle are explained in Section II. The theory of secondary-side (receiving coil-side) PWM is described with a time-domain analysis in Section III. Experimental results of a 700 W IPT converter prototype based on a 600 V GaN-HFET are demonstrated in Section IV by comparing with a SJ-MOSFET-based prototype under the hard switching and ZVS conditions, then the practical advantages of the proposed converter are summarized in Section V.

II. Circuit Topology and Operation

A. Circuit Configuration

The circuit topology of the proposed converter is presented in Fig. 3.

The primary-side (sending coil-side) HF-R INV generates the resonant current through the series compensation network L_1-C_1-C_2, while the HF-BLREC regulates the resonant current via the series compensation network L_2-C_s in the receiving side. All the active switches Q_1–Q_4 of GaN-HFET operate with the edge-resonant ZVS based on the lossless snubber capacitors C_{s1}–C_{s4}. The edge-resonant ZVS is effective for the 600 V GaN-HFET since the output capacitance (C_{oss}) is nonlinear and too small to reduce the dv/dt rate at the turn-on/-off transitions for the several hundred dc voltage. The current phase of i_p should be lagged for the voltage v_p in the HF-R INV in order to attain ZVS, whereby the switching frequency of Q_1 and Q_2 can be controlled by the principle of phase-locked-loop (PLL) as shown in Fig. 3.

The SR and secondary-side PWM is applied into Q_3 and Q_4, which is advantageous to the delay time control based on the zero current detection of primary side [21]. The pseudo diode mode which is drawn in Fig. 2 can be minimized at the turn-on transitions of Q_3 and Q_4, consequently the conduction power loss is minimized for the GaN-HFET in the HF-BLREC.

The HF-R INV operates with the inductive load condition for achieving ZVS, while the secondary-side HF-BLREC deals with the fundamental frequency components of sending and receiving coil currents. The resonant frequencies f_{r1} and f_{r2} of the primary- and secondary-side series resonant tanks are determined with respect to the switching frequency f_s of Q_1–Q_4 as

$$f_{r1} < f_{r2} = f_s \tag{1}$$

$$f_{r1} = \frac{1}{2\pi\sqrt{L_1 C_r}} \tag{2}$$

$$f_{r2} = \frac{1}{2\pi\sqrt{L_2 C_s}} \tag{3}$$

where the primary-side resonant capacitors C_1, C_2 are the same value and combined as $C_r = C_1 + C_2$.

B. Operating Mode Transitions

The key voltage and current waveforms are illustrated in Fig. 4. The corresponding mode transitions and equivalent circuits are depicted in Fig. 5. The switching one-cycle is divided into fourteen modes as follows:

[Mode 1: steady-state power transfer in series load resonant] ($t_0 \le t < t_1$) The current i_{Q_1} through Q_1 naturally changes its direction at t_0 due to the series load resonant in the HF-R INV, then power is fed from the dc input to the dc load through the sending and receiving coils.

[Mode 2: ZCS turn-off in D_{o1} and edge resonant in HF-BLREC] ($t_1 \le t < t_2$) The current $i_{\mathrm{D}_{o1}}$ through D_{o1} decreases naturally to zero at t_1 by the series load resonant, whereby the ZCS turn-off without any reverse recovery current can be achieved in D_{o1}. At the same time, the lossless snubber capacitor C_{s3} begins to discharge with the edge resonant.

[Mode 3: SR turn-on in Q_3] ($t_2 \le t < t_3$) The voltage v_{Q_3} across the secondary-side GaN-HFET Q_3 descends to zero level at t_2, after which the gate signal is immediately supplied to Q_3 by SR. Accordingly, the reverse FET conduction starts in Q_3. The ON-term of the secondary-side GaN-HFET Q_3 and Q_4 are overlapped in this interval.

[Mode 4: edge resonant in HF-BLREC] ($t_3 \le t < t_4$) The gate signal of Q_4 is removed at t_3, then the voltage v_{Q_4} across Q_4 starts to rise gradually with the receiving-coil current i_s.

[Mode 5: ZVS turn-off in Q_4 and D_{o2} forward biased] ($t_4 \le t < t_5$) The voltage v_{Q_4} across Q_4 reaches to the same level as the output voltage V_o. Accordingly, the high-side diode D_{o4} is naturally forward-biased and the magnetic energy stored in the receiving coil is released to the load. On the other hand, the magnetic energy is stored in the sending coil.

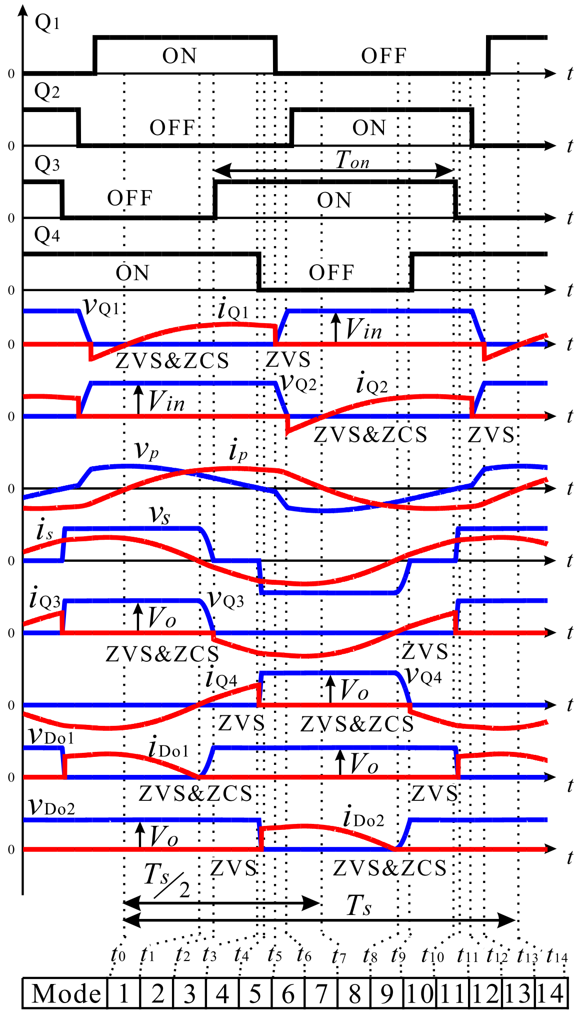

Fig. 4. Key voltage and current waveforms during one switching-cycle.

[Mode 6: edge resonant in HF-R INV] ($t_5 \le t < t_6$) The gate signal of Q_1 is removed at t_5, then the lossless snubber capacitor C_{s1} charges while the counterpart snubber capacitor C_{s2} discharges. Accordingly, the voltage v_{Q_1} starts to rise gradually while v_{Q_2} declines with a certain slope.

[Mode 7: ZVS turn-off in Q_1 and ZVZCS turn-on in Q_2] ($t_6 \le t < t_7$) The voltage v_{Q_1} reaches to V_{in} at t_6, whereby the ZVS turn-off attains in Q_1. The voltage v_{Q_2} decreases to zero at t_6, after which the gate signal is supplied to Q_2; Thus, ZVZCS turn-on can be attained in Q_2 by SR.

[Mode 8: steady-state power transfer in series load resonant] ($t_7 \le t < t_8$) The current i_{Q_2} through Q_2 changes its polarity at t_7 due to the series load resonant in the HF-R INV. Accordingly, power is fed to the dc load through the primary and secondary-side circuits.

[Mode 9: ZCS turn-off in D_{o2} and edge resonant in HF-BLREC] ($t_8 \le t < t_9$) The current $i_{\mathrm{D}_{o2}}$ through D_{o2} decreases naturally to zero at t_8 by the series load resonant, whereby the ZCS turn-off can be achieved in D_{o2} without any reverse recovery current. At the same time, the lossless snubber capacitor C_{s4} begins to discharge in the edge resonant.

[Mode 10: SR turn-on in Q_4] ($t_9 \le t < t_{10}$) The voltage

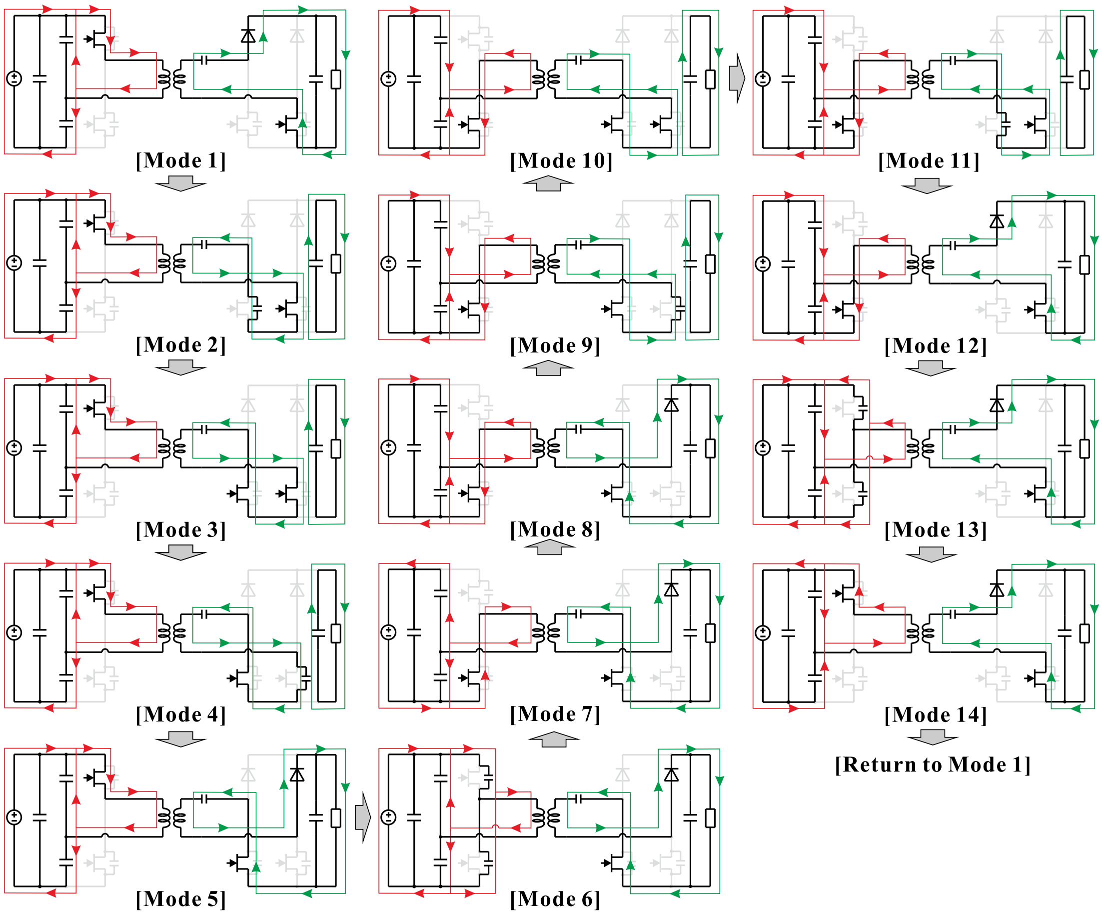

Fig. 5. Operating mode transitions and equivalent circuits during one switching-cycle.

v_{Q_4} across the secondary-side GaN-HFET Q_4 descends to zero level at t_9, after which the gate signal is immediately supplied to Q_4 by SR. Thus, the reverse FET conduction is initiated in Q_4. The ON-term of the secondary-side GaN-HFET Q_3 and Q_4 are overlapped in this interval.

[Mode 11: edge resonant in HF-BLREC] ($t_{10} \le t < t_{11}$) The gate signal of Q_3 is removed at t_{10}, then the voltage v_{Q_4} begins to rise gradually with the receiving coil current i_s.

[Mode 12: magnetizing energy released and power fed to load] ($t_{11} \le t < t_{12}$) The low-side switch Q_2 of the HF-R INV is on-state and the magnetizing inductance releases its energy to the load through sending and receiving coils. The diode D_{o1} are forward-biased while the active switch Q_4 are in the reversely conducting FET mode of GaN HFET.

[Mode 13: edge resonant in HF-R INV] ($t_{12} \le t < t_{13}$) The gate signal to the low-side switch Q_2 is removed at $t = t_{12}$, then the lossless snubber capacitor C_{s2} is charged while C_{s1} is discharged simultaneously by the sending coil current i_p. The voltage v_{Q_2} across Q_2 starts to rise gradually while the voltage v_{Q_1} across Q_1 decreases gradually.

[Mode 14: ZVS turn-off in Q_2 and ZVZCS turn-on in Q_1] ($t_{13} \le t < t_{14}$) The voltage v_{Q_2} reaches V_{in} at t_{13}, thereby the ZVS turn-off is completed in Q_2. The voltage v_{Q_1} decreases to zero at t_{13}, after which the gate signal is supplied to Q_1; Thus, ZVZCS turn-on can be attained in Q_1 by SR.

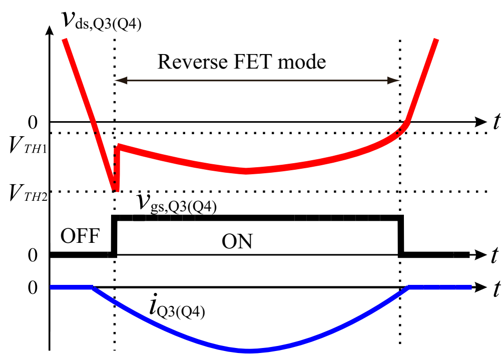

Fig. 6. Synchronous switching of secondary-side GaN-HFET Q_3, Q_4 with gate signals.

The voltage and current waveforms of the secondary-side Q_3 and Q_4 with SR are illustrated in Fig. 6. The reversely conduction intervals Modes 14→1→4, for Q_4 and Modes 6→11 for Q_3 are comprised of the reverse FET conduction from source to drain with the gate-driven ON. Accordingly, conduction losses are well reduced owing to the low ON-resistance of GaN-HFET.

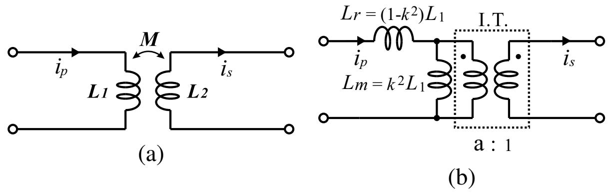

Fig. 7. Extension of the lumped-parameter sending and receiving coils: (a) magnetically coupled model, and (b) L-type HF transformer model.

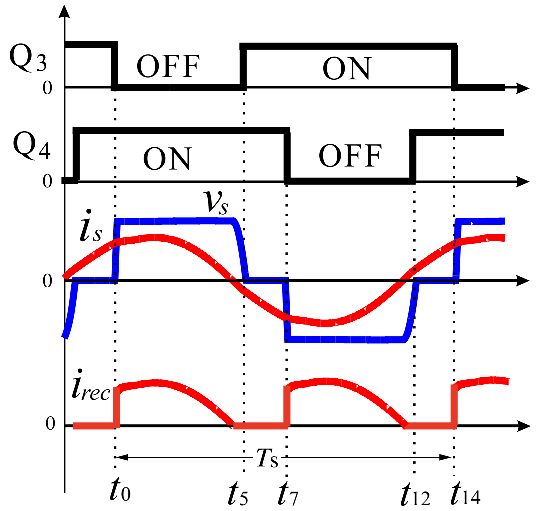

Fig. 8. Secondary-side voltage and current waveforms with PWM gate signals.

III. Analysis on Secondary-side PWM Power Control

The sending and receiving coils can be modeled by using the HF transformer of the lumped-parameter circuit in the frequency band less than several-hundred kHz. Fig. 7 displays the magnetically coupled inductor model and the HF transformer model of the sending and receiving coils. The leakage and magnetizing inductances which depend on the gap length between the two coils are uniquely expressed by L_r and L_m in Fig. 7 (b), where the winding turns ratio a of ideal transformer (I.T.) is defined with the coupling coefficient k as

$$a = \frac{M}{L_2} = k\sqrt{\frac{L_1}{L_2}}. \tag{4}$$

The key waveforms of the HF-BLREC with the PWM patterns of Q_3 and Q_4 are depicted in Fig. 8. The corresponding equivalent circuits based on the sinusoidal approximation are introduced in Fig. 9. The equivalent ac resistance R_{ac} (see the Appendix A) can be determined as

$$R_{ac} = \left\{\frac{\sqrt{2}a}{\pi}(1+\cos\alpha)\right\}^2 R_o \tag{5}$$

$$\alpha = 2\pi\,(D-0.5) \tag{6}$$

where D denotes the ON-duty cycle of Q_3 and Q_4 as

$$D = \frac{T_{on}}{T_s} \quad (0.5 \leq D \leq 1.0). \tag{7}$$

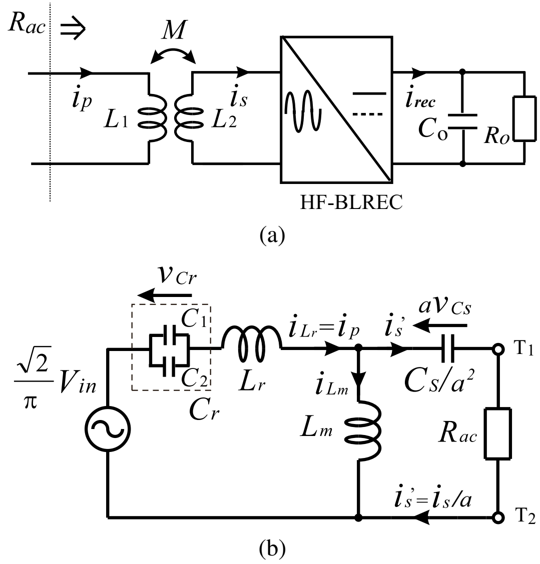

Fig. 9. Sinusoidal approximation diagrams based on Figs 7 and 8: (a) equivalent ac resistance R_{ac}, and (b) simplified equivalent circuit of proposed converter, the terminals T_1–T_2 shorted for the circulation intervals t_0–t_5, t_{12}–t_{14}.

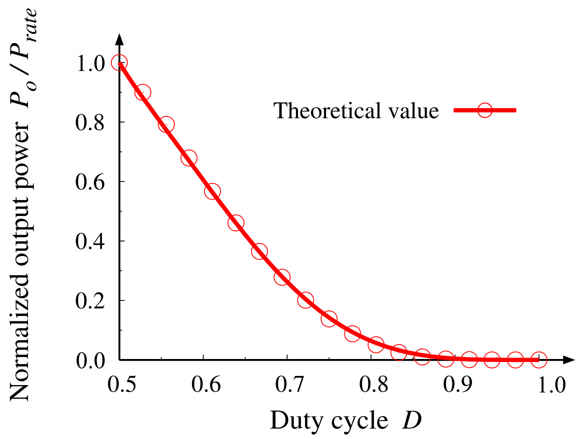

Fig. 10. Calculated output power characteristics based on the secondary-side PWM.

The output dc voltage V_o can be expressed with D under the ideal condition where only the fundamental component of the HF-BLREC input voltage v_s is considered due to the series resonance as

$$V_o = \sqrt{\frac{1}{T_s}\int_{t_0}^{t_{14}} {v_s}^2 dt} \simeq \frac{\sqrt{2}V_{in}}{\pi a}\cos^2\left(\frac{\alpha}{2}\right). \tag{8}$$

Considering the converter operation is symmetric in t_0–t_7 and t_7–t_{14} in Fig. 8, the sending- and receiving-coil currents i_p, i_s are expressed from Fig. 9 (b) during the power transfer interval $t_0 \leq t < t_5$ as

$$i_p(t) = \sqrt{{i_{L_r}}^2(t_0) + \{\omega_1 C_r v_{C_r}(t_0)\}^2}\,\sin\{\omega_1(t-t_0)-\alpha_1\} \tag{9}$$

$$i_s(t) = \sqrt{{i_{L_m}}^2(t_0) + \left\{\frac{\omega_2 C_s v_{C_s}(t_0)}{a^2}\right\}^2}\,\sin\{\omega_2(t-t_0)-\alpha_2\} \tag{10}$$

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where the load resonant angular frequency ω_1, natural angular frequency ω_2 with the reflected load resistance, and the initial phase angles α_1, α_2 are defined by

$$\omega_1 = \frac{1}{\sqrt{(L_r + L_m)C_r}} = \frac{1}{\sqrt{L_1 C_r}} \quad (11)$$

$$\omega_2 = \sqrt{\frac{a^2}{L_m C_s} - \left(\frac{R_{ac}}{2L_m}\right)^2} \quad (12)$$

$$\alpha_1 = \tan^{-1}\left(\frac{i_{L_r}(t_0)}{\omega_1 C_r v_{C_r}(t_0)}\right) \quad (13)$$

$$\alpha_2 = \tan^{-1}\left(\frac{a^2 i_{L_m}(t_0)}{\omega_2 C_s v_{C_s}(t_0)}\right). \quad (14)$$

The two coil currents can be expressed for the freewheeling interval $t_5 \leq t < t_7$ as

$$i_p(t) = \sqrt{{i_{L_r}}^2(t_5) + \{v_{C_r}(t_5)C_r\omega_1\}^2}\sin\{\omega_1(t - t_5) - \alpha_3\} \quad (15)$$

$$i_s(t) = \sqrt{{i_{L_m}}^2(t_5) + \left\{\frac{\omega_3 C_s v_{C_s}(t_5)}{a^2}\right\}^2}\sin\{\omega_3(t - t_5) - \alpha_4\} \quad (16)$$

where the resonant angular frequency ω_3 of receiving coil current circulating mode and initial phase angles α_3, α_4 are defined by

$$\omega_3 = \frac{a}{\sqrt{L_m C_s}} \quad (17)$$

$$\alpha_3 = \tan^{-1}\left(\frac{i_{L_r}(t_5)}{\omega_1 C_r v_{C_r}(t_5)}\right) \quad (18)$$

$$\alpha_4 = \tan^{-1}\left(\frac{a^2 i_{L_m}(t_5)}{\omega_3 C_s v_{C_s}(t_5)}\right). \quad (19)$$

Eliminating the interval $t_5 \leq t < t_7$ which is irrelevant to the power transfer, the output power P_o can be written with RMS value I_s of i_s from (10) and (16) as

$$P_o = R_{ac}{I_s}^2 = R_{ac}\left(\frac{\int_{t_0}^{t_5} i_s(t)dt}{T_s/2}\right)^2 \quad (20)$$

where the time instant t_5 is expressed by $t_5 = (1 - D)T_s$. The steady-state characteristics based on (20) are illustrated in Fig. 10, whereby the wide range of power regulation is theoretically demonstrated. Thus, the principle of the secondary-side PWM scheme is theoretically proven hereby.

IV. Experimental Verification

A. Specification of Prototype

The practical effectiveness of the proposed converter and control scheme is investigated by experiment of the prototype. The exterior appearance of a 700 W prototype is shown in Fig. 11. The circuit parameters and specifications are summarized in TABLE I. It should be remarked here the dc input voltage V_{in} is set as 230 V for the sake of experimental constrain, therefore the power rating is scaled down as 700 W. The secondary-side high speed SR controller *IR1167* is adopted for the HF-BLREC for self-driving of Q_3 and Q_4 respectively.

The sending and receiving coils are assembled in a circular shape with high frequency LITZ wires that are attached with ferrite cores as portrayed in Fig. 12. The double-ring circular coils are adopted for both the sending and receiving coils to maximize the cross-section area of magnetic flux. Specifications of the coils are indicated in TABLE II. In order to focus on the performance evaluation of the converter topology with GaN-HFET, the gap length and coupling coefficient between the two coils are fixed in the experiment.

The fundamental frequency of the sending and receiving coils is determined as 85 kHz for harmonizing with the ISM frequency band of practical IPT systems. The primary-side resonant frequency f_{r1} is set as 79 kHz on the basis of (1) for achieving ZVS in the HF-R INV. The secondary-side resonant frequency f_{r2} and the switching frequency f_s of all the active switches are decided at 85 kHz; the practical switching frequency suitable for kW-class IPT systems with a high voltage GaN-HFET. As a result, the resonant capacitors

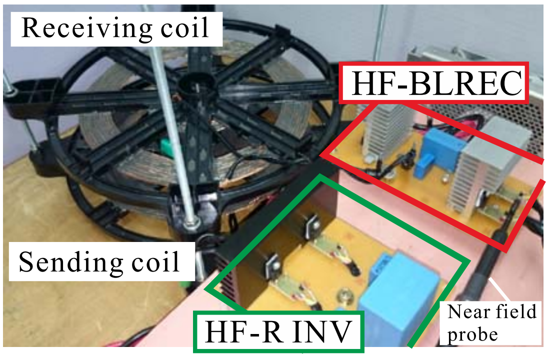


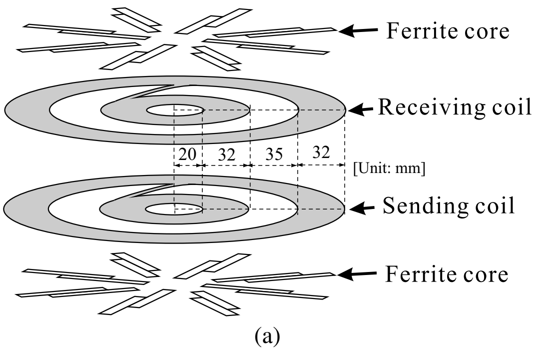
Fig. 11. Exterior appearance of a proposed IPT-ZVS converter prototype.

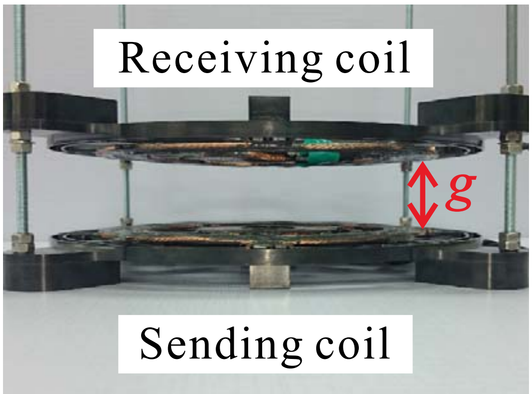
TABLE I
CIRCUIT PARAMETERS AND EXPERIMENTAL CONDITIONS OF MAIN CIRCUIT

Item	Symbol	Value [unit]
DC input voltage	V_{in}	230 [V]
DC output voltage	V_o	130 [V]
Output power rating	P_o	700 [W]
Nominal switching frequency	f_s	85 [kHz]
Input smoothing capacitor	C_{in}	50 [μF]
Resonant capacitors	C_1, C_2	33 [nF]
Resonant capacitor	C_s	56 [nF]
Lossless snubbing capacitors	C_{s1}-C_{s4}	5.6 [nF]
Output smoothing capacitor	C_o	10 [μF]
Dead time interval	t_d	500 [ns]

TABLE II
CIRCUIT PARAMETERS AND EXPERIMENTAL CONDITIONS OF SENDING AND RECEIVING COILS

Item	Symbol	Value [unit]
Winding turns	N_1/N_2	20/20 [turn]
Self inductance of sending coil	L_1	62 [μH]
Self inductance of receiving coil	L_2	65 [μH]
Mutual inductance of L_1 and L_2	M	23 [μH]
Coupling coefficient of L_1 and L_2	k	0.36
Air gap length between L_1 and L_2	g	50 [mm]





(b)

Fig. 12. Structure of sending and receiving coils: (a) schematic view, and (b) assembly view.

of the primary and secondary-side compensation networks can be designed from (2) and (3) as $C_1 = C_2 = 33\,\mathrm{nF}$ and $C_s = 56\,\mathrm{nF}$, respectively.

The electrical characteristics of GaN-HFET and SJ-MOSFET are summarized for comparison in TABLE III. The voltage and current ratings are identical as 600 V and 15 A, which is the basis of the power device selection for the comparative experiment. In contrast, the ON-resistance $R_{ds,on}$ and gate charge of GaN-HFET are much lower than those of SJ-MOSFET in the equivalent package size.

B. Experimental Results

The operating waveforms of the GaN-HFET -based HF-R INV are displayed together with the sending and receiving coils in Fig. 13. The ZVZCS turn-on and ZVS turn-off operations are observed in each of the active switches that are assisted with the lossless snubber capacitors C_{s1} and C_{s2}.

The operating waveforms of the HF-BLREC are depicted in Fig. 14 for $D = 0.75$ and $P_o = 190\,\mathrm{W}$. The surge voltages emerge at the turn-off transitions of Q_3 and Q_4 in the case of non-edge resonant (without lossless snubber capacitors) and hard switching due to the tiny output capacitance of GaN-HFET. In addition, the turn-on transitions of D_{o1} and D_{o2} appear with a high dv/dt rate as observed in Fig. 14 (a). The ZVS turn-off and ZVZCS turn-on operations maintain in Q_3 and Q_4 due to the effect of the edge resonant ZVS as observed in Fig. 14 (b). The ringing currents occur at

TABLE III
ELECTRICAL CHARACTERISTICS OF GAN-HFET AND SJ-MOSFET IN COMPARISON

Item	Symbol	GaN-HFET (GaN-GIT) PGA26C09DV (Panasonic)	SJ-MOSFET IXKC-15N60C5 (IXYS)
Drain-source voltage	V_{ds}	600 [V]	600 [V]
Drain current	I_d	15 [A]	15 [A]
Gate threshold voltage	V_{th}	1.2 [V]	3.0 [V]
Drain-source ON-resistance	$R_{ds,on}$	71 [mΩ]	150 [mΩ]
Gate charge	Q_g	9 [nC]	40 [nC]
Input capacitance	C_{iss}	115 [pF]	1100 [pF]
Output capacitance @$V_{ds} = 230$ [V]	C_{oss}	80 [pF]	70 [pF]

D_{o1}-D_{o2} : VS-15ETL06FPPbF , 600V - 15A, 0.85 V (Vishay)

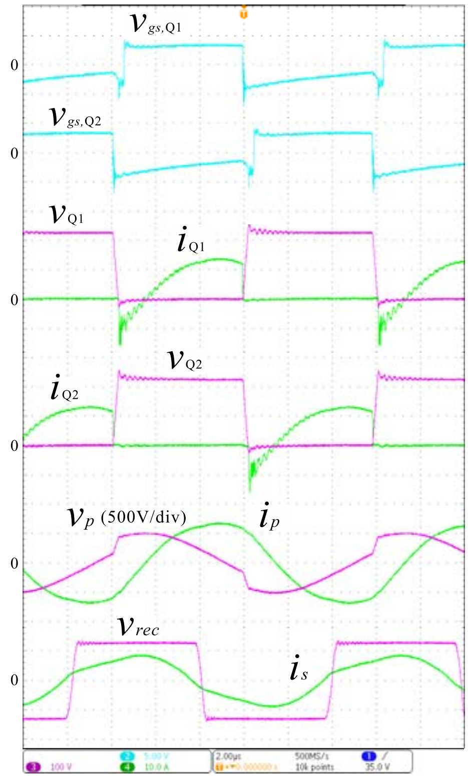
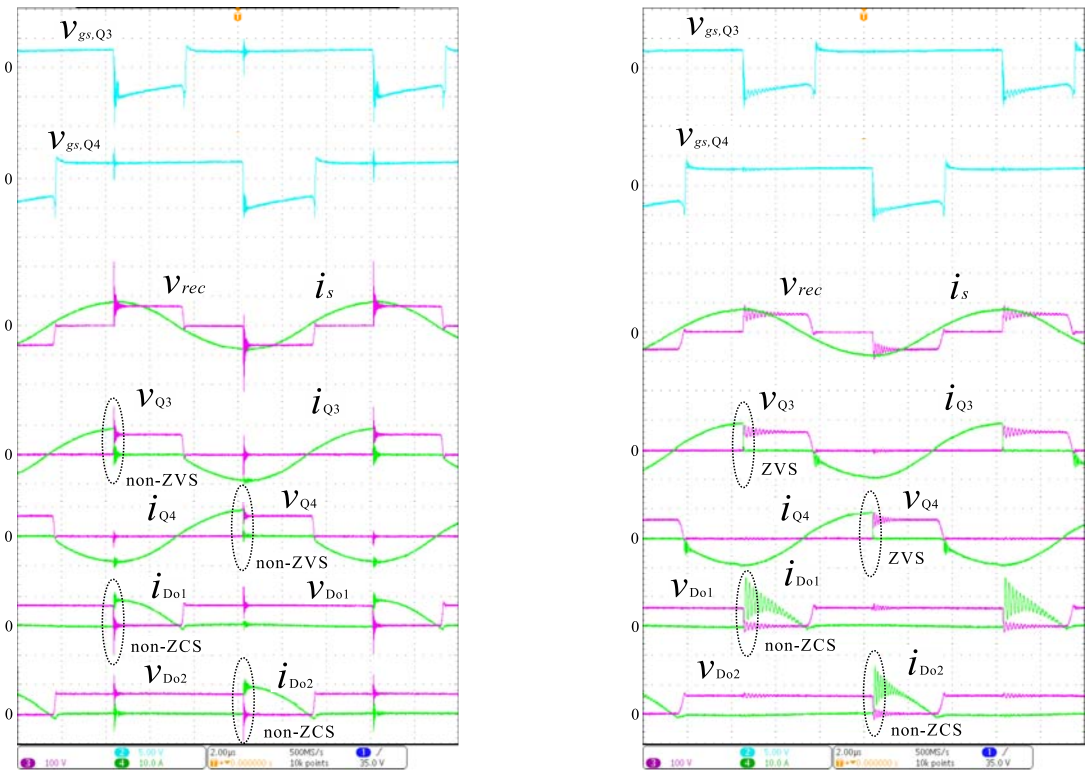


Fig. 13. Observed waveforms of the HF-R INV at $D = 0.5$ and $P_o = 700\,\mathrm{W}$ ($v_{gs,x} = 5\,\mathrm{V/div}$, $v_{Q,x} = 100\,\mathrm{V/div}$, $v_p = 500\,\mathrm{V/div}$, $v_{rec} = 100\,\mathrm{V/div}$, $i_{Q,x}$, i_p and $i_s = 10\,\mathrm{A/div}$, $2\mu\mathrm{s/div}$).

the turn-on transitions of D_{o1} and D_{o2}, which derive from the oscillation of the lossless snubbers C_{s3}, C_{s4} and stray inductances of the HF-BLREC. However, the slow dv/dt rate can be attained at the turn-on transitions due to C_{s3} and C_{s4}, thereby soft commutation can maintain for D_{o1} and D_{o2}.

The radiation noise spectrums from the HF-BLREC are compared in Fig. 15 for non-edge resonant and edge resonant ZVS conditions. The noise emission levels are measured with a near-field-noise probe at the distance of 10 mm from Q_3 and Q_4, as portrayed with Fig. 11. The noise emission is relatively



(a) (b)

Fig. 14. Observed waveforms of HF-BLREC at $D = 0.75$ and $P_o = 190\,\mathrm{W}$: (a) non-edge resonant (hard switching), and (b) edge resonant ZVS ($v_{gs,x} = 5\,\mathrm{V/div}$, v_{rec}, $v_{Do,x}$ and $v_{Q,x} = 100\,\mathrm{V/div}$, $i_{Q,x}$, $i_{Do,x}$ and $i_s = 10\,\mathrm{A/div}$, $2\mu\mathrm{s/div}$).

outstanding around $6\,\mathrm{MHz}$ in the ZVS condition. This is due to non-ZCS turn-on in $\mathrm{D_{o1}}$ and $\mathrm{D_{o2}}$ for the duty cycle $D > 0.5$, which is caused by the stray inductances of wire patterns on the printed board and junction capacitances of $\mathrm{D_{o1}}$ and $\mathrm{D_{o2}}$. In contrast, the radiation noises are reduced by ZVS over $10\,\mathrm{MHz}$ frequency band, thus the high-frequency noise emission can be minimized by the edge resonant ZVS in the HF-BLREC.

The steady-state characteristics of PWM-controlled output power are presented in Fig. 16. As theoretically discussed in Fig. 10, the output power is continuously regulated by the secondary-side PWM with the wide range of ZVS operations.

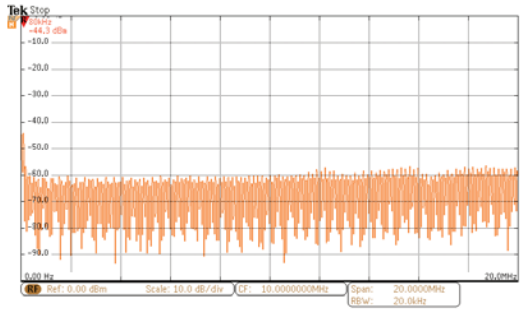
The actual efficiency curves are compared among the HF-BLREC -based prototypes with GaN-HFET and SJ-MOSFET operating as synchronous rectifier, and the conventional full-bridge diode rectifier (D-REC) in Fig. 17. Note here the output power is controlled by PFM (f_s variation: $85\,\mathrm{kHz}$-$130\,\mathrm{kHz}$) in the ZVS HF-R INV with GaN-HFET for all the prototypes. The higher efficiency is observed in the proposed converter with the GaN-HFET-based HF-BLREC over the whole range of output power, and the maximum efficiency is recorded as $93.4\,\%$ at $P_o = 700\,\mathrm{W}$.

The actual efficiency characteristics are compared between the hard switched and ZVS HF-BLREC -based prototypes with GaN-HFET and SJ-MOSFET respectively, all of which are controlled by the secondary-side PWM under the condition of constant switching frequency ($f_s = 85\,\mathrm{kHz}$). Note here the primary-side converter consists of the switching frequency GaN-HFET ZVS HF-R INV for all the prototypes. The higher efficiency can be observed in the ZVS HF-BLREC over the whole range of output power, and the maximum efficiency is recorded as $93\,\%$ at $P_o = 700\,\mathrm{W}$. The efficiency improvement will be more outstanding for higher switching frequency condition.

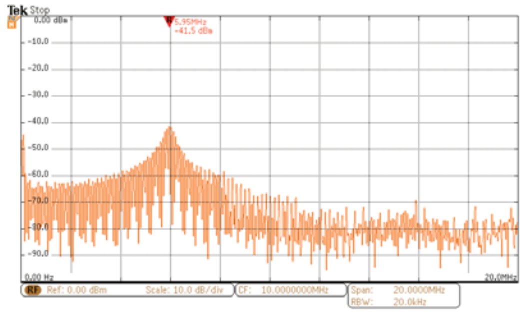
The power loss analysis of the prototype is shown in Figs. 19 (a) and (b) for the several output power settings. The switching power losses are eliminated completely from the breakdowns owing to the wide range of ZVS in $\mathrm{Q_1}$–$\mathrm{Q_4}$ and ZCS in $\mathrm{D_{o1}}$ and $\mathrm{D_{o2}}$. The power losses of the input and output filter capacitors are also precluded from the display of loss breakdowns; $6.2\,\mathrm{W}@100\,\%$ load, $4.6\,\mathrm{W}@60\,\%$ load, and $4.4\,\mathrm{W}@30\,\%$ load. Fig. 19 (a) displays the power loss breakdown of the primary-side HF-R INV. The conduction power losses of $\mathrm{Q_1}$ and $\mathrm{Q_2}$ make the smaller parts than the copper loss of the sending coil. The power loss breakdown of the HF-BLREC is revealed in Fig. 19 (b). The ratio of conduction power losses of $\mathrm{Q_1}$ and $\mathrm{Q_2}$ increases while that of $\mathrm{D_{o1}}$ and $\mathrm{D_{o2}}$ decreases according to the reduction of output power. Expansion of the overlapped time interval between $\mathrm{Q_3}$ and $\mathrm{Q_4}$ may cause increase of power consumption in the secondary-side active switches $\mathrm{Q_3}$ and $\mathrm{Q_4}$.

V. Conclusion

The high-frequency bridgeless rectifier-applied GaN-HFET ZVS multi-resonant dc-dc converter for IPT systems has been



(a)



(b)

Fig. 15. Radiation noise spectrums measured around the GaN-HFET Q_3 and Q_4 in the HF-BLREC: (a) non-edge resonant, and (b) edge resonant.

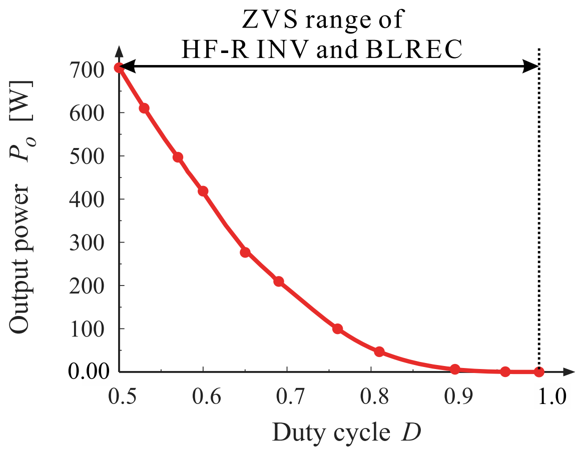


Fig. 16. Output power versus duty cycle curve in the open loop controller.

newly proposed and discussed in this paper. The secondary-side PWM is introduced in the proposed converter, then the output power regulation is verified by the experimental results independently from the primary-side GaN-HFET-based high-frequency resonant inverter. The power conversion efficiency can improve under the condition of loosely coupled coils by the effect of edge resonant and series load resonant operations as well as the low ON-resistance of GaN-HFET, compared to same ratings SJ-MOSFET-based prototype. The maximum efficiency over 93 % has been achieved in the dc-dc power conversion stage with assist of synchronous rectification, whereby the pseudo diode mode of GaN-HFET is eliminated

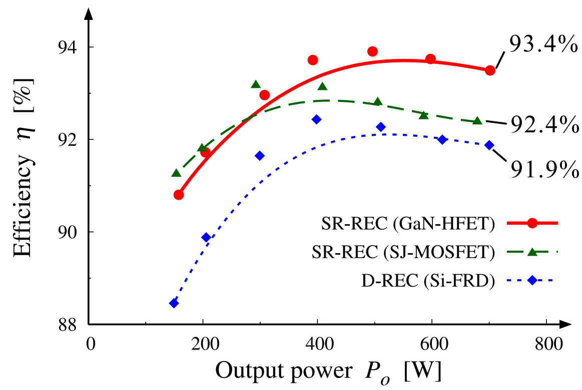


Fig. 17. Actual efficiency curves of dc-dc power conversion with synchronous rectification ($D = 0.5$ fixed).

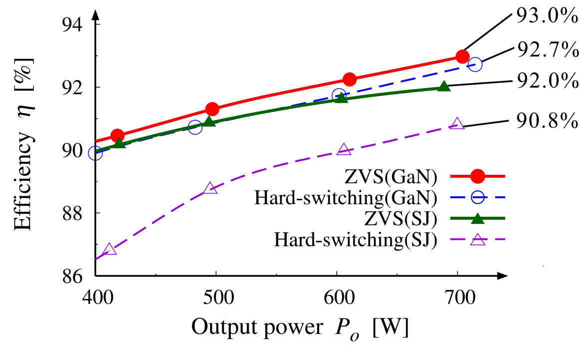


Fig. 18. Actual efficiency curves of dc-dc power conversion with secondary-side PWM.

and the low ON-resistance can maintain for the reversely conducting interval. The radiation noise has been reduced in the frequency band over 10 MHz by applying the edge resonant ZVS technique for all the GaN-HFET.

The closed loop controller design and the experiment evaluation will be a future research subject.

Appendix A
Derivation of Equivalent Resistance R_{ac}

The power balance of input and output sides are expressed under the ideal condition by referring to Fig. 9 (b) and (20) as

$$R_{ac}{I_s'}^2 = R_{ac}\left(\frac{I_s}{a}\right)^2 = R_o{I_o}^2 \tag{21}$$

where I_s' denotes the RMS value of the sending-side reflected current of i_s as

$$i_s = \sqrt{2}aI_s' \sin\omega_s t. \tag{22}$$

The dc output current I_o is expressed with the rectified current i_{rec} as

$$\begin{aligned} I_o &= \frac{1}{\pi}\int_\alpha^\pi i_{rec} d(\omega_s t) = \frac{1}{\pi}\int_\alpha^\pi |i_s|\, d(\omega_s t) \\ &= \frac{\sqrt{2}aI_s'}{\pi}(1+\cos\alpha). \end{aligned} \tag{23}$$

Substituting (22) and (23) into (21) yields the definition of R_{ac} in (5).

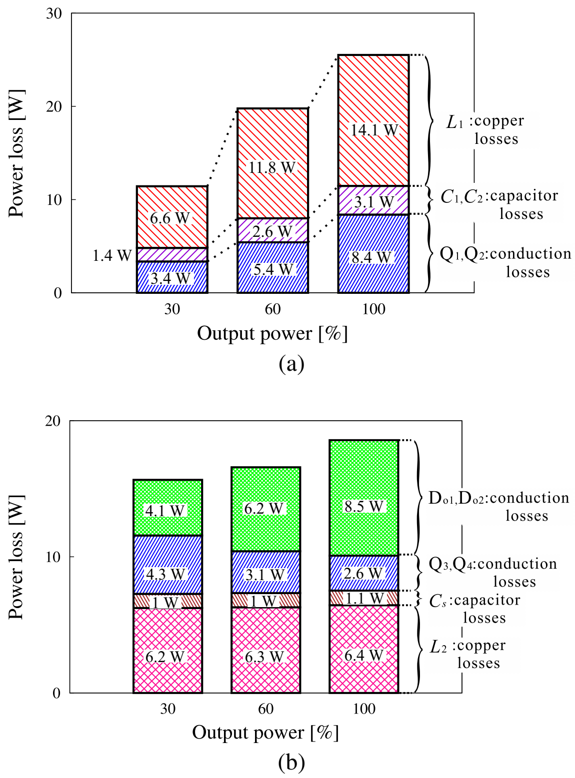


Fig. 19. Power loss breakdown of the prototype: (a) primary-side HF-R INV, and (b) secondary-side HF-BLREC.

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