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Takahashi, Hajime
Hanafusa, Yuki
Kimura, Yoshinari
Kitamura, Masatoshi

(Citation)
Japanese Journal of Applied Physics,57(3):03EH03-03EH03

(Issue Date)
2018-03

(Resource Type)
journal article

(Version)
Accepted Manuscript

Application of pentacene thin-film transistors with controlled threshold voltages to enhancement/depletion inverters

Hajime Takahashi, Yuki Hanafusa, Yoshinari Kimura, and Masatoshi Kitamura*

Department of Electrical and Electronic Engineering, Graduate School of Engineering, Kobe University, Kobe 657-8501, Japan

Oxygen plasma treatment has been carried out to control the threshold voltage in organic thin-film transistors (TFTs) having a SiO_2 gate dielectric prepared by rf sputtering. The threshold voltage linearly changed in the range of –3.7 to 3.1 V with the increase in plasma treatment time. Although the amount of change is smaller than that for organic TFTs having thermally grown SiO_2, the tendency of the change was similar to that for thermally grown SiO_2. To realize different plasma treatment times on the same substrate, a certain region on the SiO_2 surface was selected using a shadow mask, and was treated with oxygen plasma. Using the process, organic TFTs with negative threshold voltages and those with positive threshold voltages were fabricated on the same substrate. As a result, enhancement/depletion inverters consisting of the organic TFTs operated at supply voltages of 5 to 15 V.

*E-mail: kitamura@eedept.kobe-u.ac.jp

1. Introduction

Organic thin-film transistors (TFTs) have been intensively studied toward their application to flexible, large-area, light-weight, and low-cost electronic devices.[1-4] The performance of organic TFTs including field-effect mobilities has been progressing for over ten years.[5-7] From the progress of the performance in organic TFTs, it is expected that organic TFTs are practically applied to logic circuits[8-12] and active matrix displays.[13-20] Threshold voltage control is an important issue for such applications of organic TFTs.

The threshold voltage in metal-oxide-semiconductor field-effect transistors (MOSFETs) including organic TFTs is affected by the work functions of the gate electrodes and the semiconductor, charges in the gate dielectric, and dipole on the interface between the gate dielectric and the semiconductor.[21-23] Also, the voltage applied to an additional gate [24,25] and the parasitic resistance[26,27] change the threshold voltage. Some groups have demonstrated threshold voltage control in organic TFTs on the basis of these phenomena. Oxygen plasma[28] and UV ozone treatments[29-31] have been conducted to obtain a hydrophilic surface as pretreatment for gate dielectrics in organic TFTs. Such a treatment causes excess charges on or close to the surface of the gate dielectric. Thus, it is possible that such a treatment is used for threshold voltage control. In fact, oxygen plasma treatment leads to the change in threshold voltage in organic TFTs.[32-35]

We have demonstrated the control of the threshold voltage in pentacene[36] and dinaphthothienothiophene (DNTT)[37] TFTs fabricated on Si substrates with thermally grown SiO_2 using oxygen plasma treatment to the surface of the gate dielectric. The threshold voltage linearly changed in the range from −6.4 to 9.4 V with the increase in the plasma treatment time.[37] The relationship between the threshold voltage and the plasma treatment time is important for the design of actual circuits. In addition, p-channel organic TFTs having a negative or a positive threshold voltage serve as an enhancement- or a depletion-type PMOS, respectively. When p-channel organic TFTs having a negative threshold voltage are used for

logic circuit, four TFTs are required for constructing a stably operating inverter.[38,39] On the other hand, the use of enhancement- and depletion-type PMOS enables the construction of an inverter consisting of two PMOSs known as an enhancement/depletion (E/D) inverter.

In actual work, we have used DNTT TFTs having different threshold voltages fabricated on Si substrates for E/D inverters.[37] The E/D inverter operated at supply voltages of 5 to 20 V. However, the E/D inverter was constructed by externally connecting DNTT TFTs fabricated on different substrates. In addition, use of a silicon substrate having thermally grown SiO_2 is not suitable for practical application. Thus, it is necessary to clarify whether this method of threshold voltage control is applicable to organic TFTs having other gate dielectrics instead of thermally grown SiO_2.

In this paper, we report the characteristics of pentacene TFTs having a SiO_2 gate dielectric fabricated on glass substrates. The SiO_2 gate dielectric for the TFT was deposited by rf sputtering, and the surface was treated with oxygen plasma for control of the threshold voltage. We investigated the dependence of the threshold voltage in the TFT on treatment time. The treatment time for a TFT applied to a logic inverter was determined on the basis of the investigation. The characteristics of logic inverters consisting of TFTs having a threshold voltage adjusted are shown to evaluate the effectiveness of the threshold voltage control.

2. Enhancement/depletion inverters

Figure 1(a) shows the circuit for an E/D inverter consisting of an enhancement-type PMOS1 and a depletion-type PMOS2. In general, PMOS1 and PMOS2 have negative and positive threshold voltages, respectively. Figure 1(b) shows the ideal output characteristic for an E/D inverter, which is classified into four regions: I, II, III, and IV. The output voltage V_{OUT} can be given by

$$V_{\mathrm{OUT}}=\begin{cases} V_{\mathrm{IN}}-V_{\mathrm{TH1}}+\left[\left(V_{\mathrm{IN}}-V_{\mathrm{DD}}-V_{\mathrm{TH1}}\right)^2-\dfrac{\beta_2}{\beta_1}{V_{\mathrm{TH2}}}^2\right]^{\frac{1}{2}}, & \text{for } 0\le V_{\mathrm{IN}}\le V_{\mathrm{S}}, \\ \text{an indefinite value between } V_{\mathrm{TH2}} \text{ and } V_{\mathrm{S}}-V_{\mathrm{TH1}}, & \text{for } V_{\mathrm{IN}}=V_{\mathrm{S}}, \\ V_{\mathrm{TH2}}-\left[{V_{\mathrm{TH2}}}^2-\dfrac{\beta_1}{\beta_2}\left(V_{\mathrm{IN}}-V_{\mathrm{DD}}-V_{\mathrm{TH1}}\right)^2\right]^{\frac{1}{2}}, & \text{for } V_{\mathrm{S}}\le V_{\mathrm{IN}}\le V_{\mathrm{DD}}+V_{\mathrm{TH1}}, \\ 0, & \text{for } V_{\mathrm{DD}}+V_{\mathrm{TH1}}\le V_{\mathrm{IN}}\le V_{\mathrm{DD}}, \end{cases} \tag{1}$$

as a function of the input voltage V_{IN} under a supply voltage V_{DD}. Here, $\beta_i = \mu_i C_{\mathrm{OX}} W_i/L_i$ (i = 1 or 2), μ_i is the field-effect mobility, C_{OX} is the gate capacitance per unit area, W_i is the channel width, L_i is the channel length, and $V_{\mathrm{TH}i}$ is the threshold voltage for PMOS1 or PMOS2. Equation (1) can be derived from the standard equation of drain current in the quadratic model for MOSFETs. V_{S} is defined as

$$V_{\mathrm{S}}=V_{\mathrm{DD}}+V_{\mathrm{TH1}}-\sqrt{\frac{\beta_2}{\beta_1}}V_{\mathrm{TH2}}\,, \tag{2}$$

and represents the switching voltage for the inverter. Since V_{OUT} has an indefinite value at $V_{\mathrm{IN}} = V_{\mathrm{S}}$, the input-output gain, $\mathrm{d}V_{\mathrm{OUT}}/\mathrm{d}V_{\mathrm{IN}}$, is minus infinity at the input voltage. In contrast to a CMOS inverter, V_{OUT} for the E/D inverter is not equal to V_{DD} when $V_{\mathrm{IN}} = 0$ as seen in Fig. 1(b).

The low (NM_{L}) and high (NM_{H}) noise margins are defined as $NM_{\mathrm{L}} = V_{\mathrm{IL}} - V_{\mathrm{OL}}$ and $NM_{\mathrm{H}} = V_{\mathrm{OH}} - V_{\mathrm{IH}}$, respectively. Here, V_{IL} or V_{IH} is an input voltage when $\mathrm{d}V_{\mathrm{OUT}}/\mathrm{d}V_{\mathrm{IN}} = -1$, and V_{OH} or V_{OL} is an output voltage at $V_{\mathrm{IN}} = V_{\mathrm{IL}}$ or V_{IH}, as shown in Fig. 1(b). From Eq. (1), NM_{L} and NM_{H} are expressed as

$$NM_{\mathrm{L}}=V_{\mathrm{DD}}+V_{\mathrm{TH1}}+\left(\frac{1}{\sqrt{1+\gamma}}-1-2\sqrt{\frac{\gamma}{3}}\right)V_{\mathrm{TH2}}\,, \tag{3}$$

$$NM_{\mathrm{H}}=-V_{\mathrm{TH1}}+\left(\frac{\gamma}{\sqrt{1+\gamma}}-\sqrt{\frac{\gamma}{3}}\right)V_{\mathrm{TH2}}\,, \tag{4}$$

where $\gamma = \beta_2/\beta_1$. Equations (2)-(4) were used for the evaluation of fabricated E/D inverters.

3. Experimental methods

Figures 2(a) and 2(b) show the cross section of the pentacene TFTs examined and the illustration of the oxygen plasma treatment adopted in this study, respectively. The pentacene TFTs were prepared on glass substrates. The fabrication process of the pentacene TFTs is as follows. First, a Au layer with a Cr adhesive layer was deposited on a glass substrate for lines connecting between terminals of TFTs. After that, a Cr gate layer was deposited on the glass substrate by thermal evaporation. Then, a SiO_2 gate dielectric was deposited by rf sputtering using a SiO_2 target. The SiO_2 gate dielectric had a unit area capacitance of about 25 nF/cm^2, which corresponds to a thickness of about 150 nm. The SiO_2 surface was treated with oxygen plasma. The AC power for plasma generation was set at 5.4 W. The condition for the plasma treatment is similar to that reported in Ref. 36. For the fabrication of E/D inverters, the area for PMOS2 was exposed to the plasma through a shadow mask for a time t_{P1}, and the entire area was exposed for a time t_{P2} as shown in Fig. 2(b). Thus, the treatment time t_P is equal to t_{P2} for PMOS1, and (t_{P1}+t_{P2}) for PMOS2. For a reference transistor, UV/ozone treatment was performed instead of oxygen plasma treatment. UV/ozone treatment can be expected to have no large influence on threshold voltage. After the second plasma or UV/ozone treatment, the substrate was immediately exposed to hexamethyldisilazane (HMDS) vapor to obtain a hydrophobic surface. A 45-nm-thick pentacene was deposited on the SiO_2 surface, and a Au layer was deposited for drain/source electrodes. The channel width was 600 μm, and the channel length was 40 μm. The deposition processes were performed at room temperature, and all layers deposited were patterned by the use of shadow masks. The maximum temperature in the fabrication process is 120 °C for the HMDS treatment. Figures 2(c) and 2(d) show photographs of an E/D inverter and a circuit consisting of two E/D inverters, respectively. The characteristics of pentacene TFTs and circuits were examined in a dry-nitrogen glovebox at room temperature using a semiconductor parameter analyzer.

4. Transistor characteristics

Figure 3(a) shows the transfer characteristics of typical pentacene TFTs serving as PMOS1 and PMOS2 in an E/D inverter in the saturation regime at a drain voltage (V_D) of −15 V. Plasma treatment time was 60 s for the PMOS1 and 420 s for the PMOS2. The PMOS1 had a threshold voltage of −3.7 V, and worked as an enhancement-type transistor. On the other hand, the PMOS2 has a threshold voltage of 1.2 V, and worked as a depletion-type transistor. The field-effect mobilities for both transistors were about 0.01 $cm^2\ V^{-1}\ s^{-1}$. The value is relatively low in pentacene TFTs. The fabrication process including pretreatment for the glass substrate has not been optimized. The surface roughness of SiO_2 deposited on such a glass substrate may cause the low mobility. In fact, the pentacene layer had a small grain structure with a diameter of about 200 nm. Although the field-effect mobility is low, the result shown in Fig. 3(a) suggests that the plasma treatment is effective for threshold voltage control to SiO_2 gate dielectrics prepared by rf sputtering.

Threshold voltages of pentacene TFTs for t_P in the range of 60 to 600 s are summarized in Fig. 3(b). The pentacene TFTs for t_P of 60 to 180 s were used for PMOS1, and the pentacene TFTs for t_P of 300 to 600 s were used for PMOS2. The data at $t_P = 0$ represents the threshold voltage of pentacene TFTs having SiO_2 gate dielectrics treated by UV/ozone. The result indicates that UV/ozone treatment does not affect the threshold voltage. The threshold voltage linearly shifts to positive voltages with respect to plasma treatment time. The line fitting to experimental data is expressed as $V_{TH} = (0.012\ V/s)\ t_P - 4.0\ V$. As a result, the threshold voltage changed in the range of −3.7 to 3.1 V under the condition that SiO_2 gate dielectrics are treated by UV/ozone and by oxygen plasma for t_P in the range of 60 to 600 s.

The threshold voltage change can be explained by the generation of negative charges on or close to the surface of the SiO_2 gate dielectric. Under some assumptions, the negative charges are calculated from the following equation for the threshold voltage of organic TFTs:

$$V_{TH} = \frac{\Phi_M - \Phi_S}{e} - \frac{1}{C_{OX}} Q_S , \quad (5)$$

where e is the electron elementary charge, Φ_M and Φ_S are the work functions of the gate electrode and the organic semiconductor, respectively, and Q_S is the surface charge density at the interface between the gate dielectric and the semiconductor.[36,37] Here, it is assumed that the surface charge is dominant as compared with the charge inside the gate dielectric. By using Φ_M = 4.5 eV for Cr gate[40] and Φ_S = 5.0 eV for pentacene[6], an experimental Qs value is calculated by substituting an experimental V_{TH} value into

$$Q_S = C_{OX}\left(\frac{\Phi_M - \Phi_S}{e} - V_{TH} \right). \quad (6)$$

Figure 3(c) shows experimental Q_S values calculated for V_{TH} values in Fig. 3(b). In this study, it is assumed that the dependence of Q_S on t_P is expressed as

$$Q_S = Q_0 + q_P t_P , \quad (7)$$

where Q_0 is the intrinsic surface charge density and q_P is the surface charge density per unit time induced by plasma treatment. By fitting a line to Q_S in Fig. 3(c), Q_0 and q_P are estimated to be 81.2 nC cm^{-2} and –0.30 nC cm^{-2} s^{-1}, respectively. We have reported q_P values of –0.76 nC cm^{-2} s^{-1} for DNTT TFTs and –3.1 nC cm^{-2} s^{-1} for pentacene TFTs. The pentacene and DNTT TFTs were fabricated on Si substrates with thermally grown SiO_2 treated at an AC power of 5.8 W. The AC power is close to that for SiO_2 prepared by rf sputtering in this study. However, the absolute value of q_P estimated in this study, 0.30 nC cm^{-2} s^{-1}, is quite small as compared with those of previous reports. The difference suggests that a SiO_2 surface prepared by rf sputtering is not easily affected by oxygen plasma treatment as compared with a surface of thermally grown SiO_2. The reason has been under investigation.

5. Inverter characteristics

Enhancement/depletion inverters were fabricated as an application of pentacene TFTs having

controlled threshold voltages. To fabricate inverters on a glass substrate, the two-step oxygen plasma treatment explained in Sect. 3 was adopted. Figure 4(a) shows the input-output characteristics of an E/D inverter consisting of two pentacene TFTs whose transfer characteristics are shown in Fig. 3(a). The characteristics, which were measured at V_{DD} = 5, 10, and 15 V, have no large hysteresis in forward and reverse sweeps. The input-output characteristics for V_{DD} = 10 and 15 V exhibited typical transfer characteristics of an inverter circuit having noise margins. The characteristics for the E/D inverter are summarized in Table I. The value of NM_L increases with V_{DD}, and the value of NM_H has no dependence on V_{DD}. The increases in NM_L and the unchanged in NM_H can be explained by Eqs. (3) and (4), respectively. From the transfer characteristics in Fig. 4(a), the measured switching voltages for V_{DD} = 5, 10, and 15 V were 0.3, 4.8, and 10.0 V, respectively. On the other hand, the switching voltages for V_{DD} = 5, 10, and 15 V were calculated to be –0.1, 4.9, and 9.9 V, respectively. The values were calculated using the mobilities and threshold voltages for the individual TFTs. The measured switching voltages are close to calculated values.

To confirm the reproducibility, the measured and calculated switching voltages of sixteen E/D inverters are shown in Fig. 4(b). For an E/D inverter, three plots for V_{DD} = 5, 10, and 15 V are shown. Pentacene TFTs with various t_P values were used for the inverters. The t_P values were 0–180 s for PMOS1 and 300–600 s for PMOS2. By substituting measured mobilities and threshold voltages into Eq. (2), the calculated switching voltage was calculated. Since the gate electrode of PMOS2 for E/D inverters was connected to the source electrode of the PMOS2, the transfer characteristics of the PMOS2 cannot be directly measured. Thus, a pentacene TFT fabricated in the area for PMOS2 on the same substrate was measured for the evaluation of mobility and threshold voltage used for calculated switching voltage. The plots of three or four inverters are slightly far from a line representing a correspondence between the measured and calculated values. This is probably due to the non-uniformity in mobilities and threshold voltage on the same substrate. On the other hand, the plots for many inverters are

close to the line. The correspondence between the measured and calculated values is useful for deciding the plasma treatment time for individual TFTs used in a circuit.

The characteristics of a two-stage inverter were measured as the next step for application to a large-scale circuit. Figure 5 shows the input-output characteristics of a two-stage inverter. The t_P values were 60 s for PMOS1 and 420 s for PMOS2. The circuits operated at V_{DD} = 5, 10, and 15 V and exhibited typical input-output characteristics for a two-stage inverter. Switching voltages, maximum gain, and noise margin of the first-stage inverter, second stage inverter, and two-stage inverter are summarized in Table II. The maximum gain of the two-stage inverter is larger than those of the individual inverters. This is a feature of a multi-stage inverter. The increase in the gain leads to the increase in the noise margin. As a result, the two-stage inverter has noise margin larger than those of the individual inverters.

6. Summary

We investigated the effect of oxygen plasma treatment on the characteristics of pentacene TFTs having a SiO_2 gate dielectric prepared by rf sputtering. The threshold voltage linearly changed in the range of −3.7 to 3.1 V with the increase in plasma treatment time. We fabricated enhancement- and depletion-type pentacene TFTs on the same substrate by two-step oxygen plasma treatment. The fabrication process was applied for the construction of logic inverter circuits. The E/D inverters operated at supply voltages of 5 to 15 V, and exhibited switching voltage close to an expected value. The threshold voltage control in organic TFTs by oxygen plasma treatment will be applicable to circuits consisting of more TFTs.

Acknowledgement

This work was supported by a Grant-in-Aid for Scientific Research, Challenging Research (Pioneering), Grant Number 17H06229.

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Figure Captions

Fig. 1. (Color online) (a) Circuit of an E/D inverter constructed using two PMOSs. (b) Typical input-output characteristics of an E/D inverter for explaining switching voltage and noise margin.

Fig. 2. (Color online) (a) Cross section of a fabricated E/D inverter consisting of pentacene TFTs. (b) Schematic illustration of two-step oxygen plasma treatment. (c) Photograph of a fabricated E/D inverter. (d) Photograph of a fabricated two-stage E/D inverter.

Fig. 3. (Color online) (a) Transfer characteristics of enhancement- and depletion-type pentacene TFTs used for an E/D inverter. (b) Dependence of threshold voltages in pentacene TFTs on plasma treatment time for the SiO_2 surface. (c) Charge densities depending on plasma treatment time estimated from measured threshold voltages.

Fig. 4. (Color online) (a) Input/output characteristics of an E/D inverter measured at V_{DD} = 5, 10, and 15 V. (b) Relationship between measured switching voltages and calculated switching voltages.

Fig. 5. (Color online) Input/output characteristics of a two-stage inverter circuit measured at V_{DD} = 5, 10, and 15 V.

Table I. Switching voltages, maximum gain, and noise margin of the inverter consisting of PMOS1 with $V_{TH1} = -3.7$ V and PMOS2 with $V_{TH2} = 1.2$ V.

V_{DD} (V)	Measured V_S (V)	Calculated V_S (V)	Maximum gain	NM_H (V)	NM_L (V)
5	0.3	–0.1	–2.2	-	-
10	4.8	4.9	–9.5	2.3	2.8
15	10.0	9.9	–19.0	2.3	7.7

Table II. Switching voltages, maximum gain, and noise margin of first-stage inverter, second-stage inverter, and two-stage inverter.

	Measured V_S (V)	Maximum gain	NM_H (V)	NM_L (V)
First-stage inverter	11.0	–19.3	0.6	8.7
Second-stage inverter	10.0	–18.2	2.4	7.9
Two-stage inverter	10.6	47.4	4.9	10.5

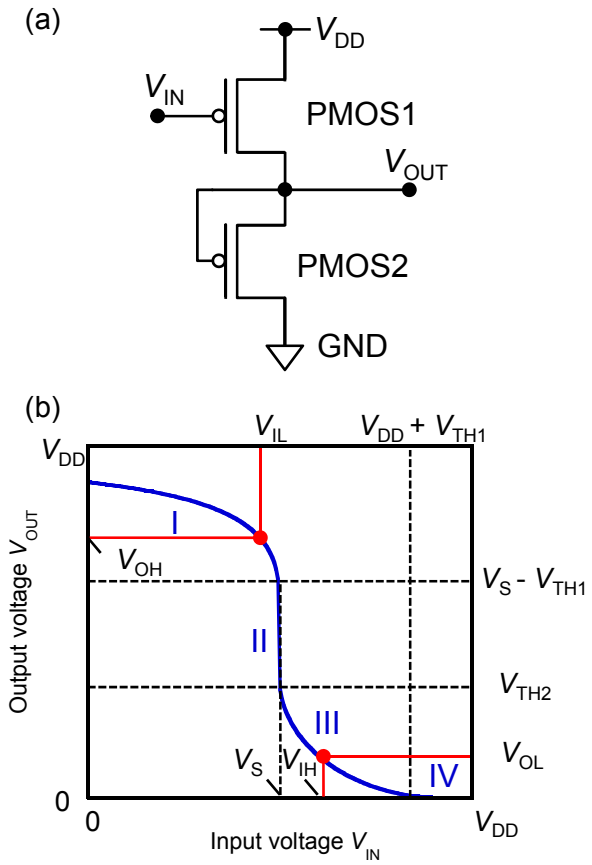

Figure 1
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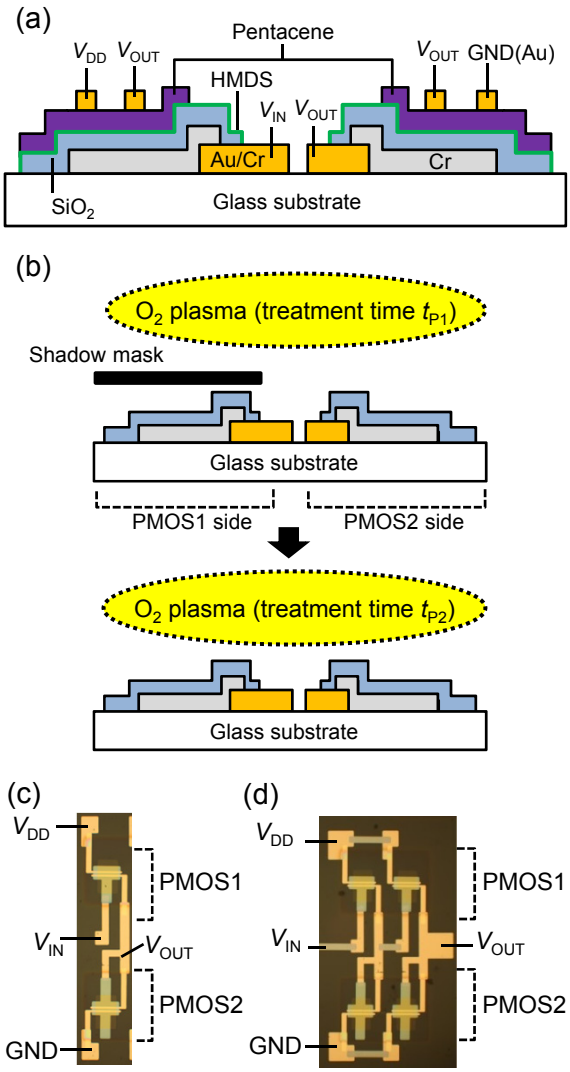

Figure 2
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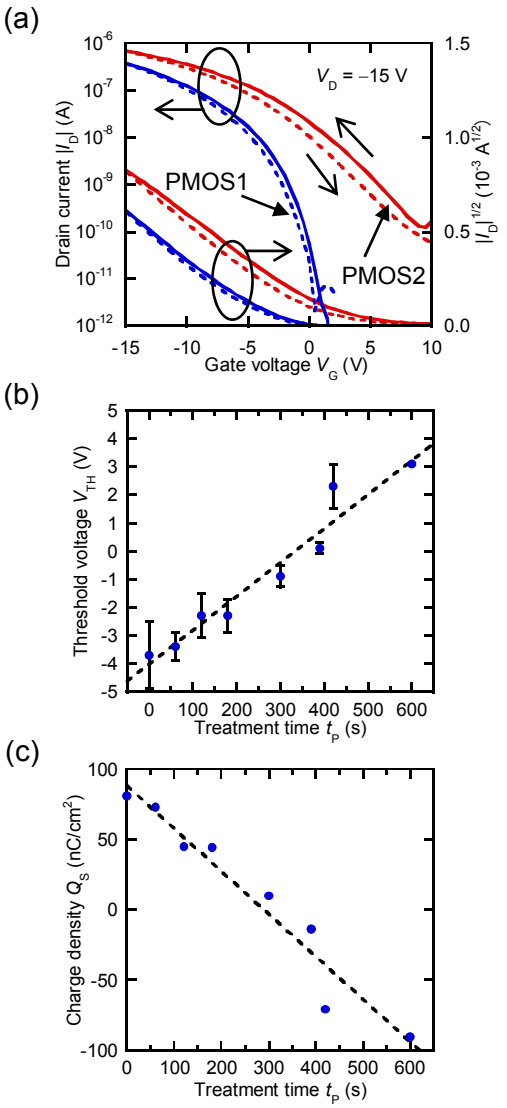

Figure 3
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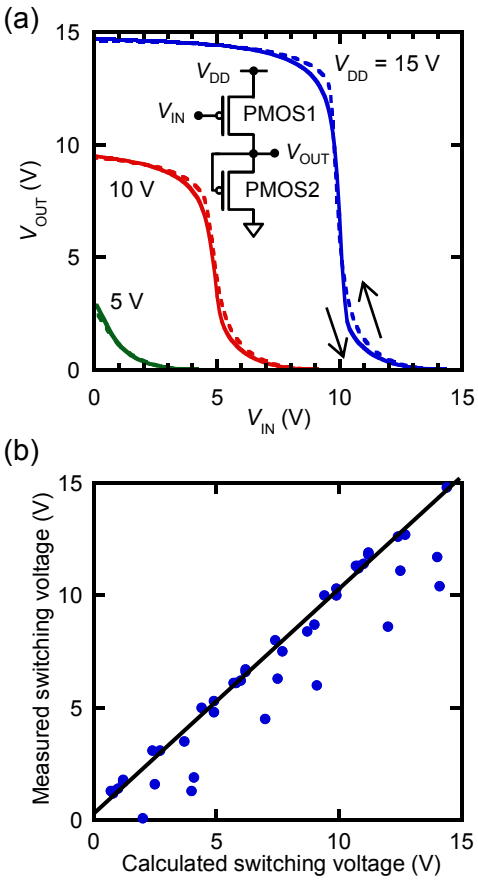

Figure 4
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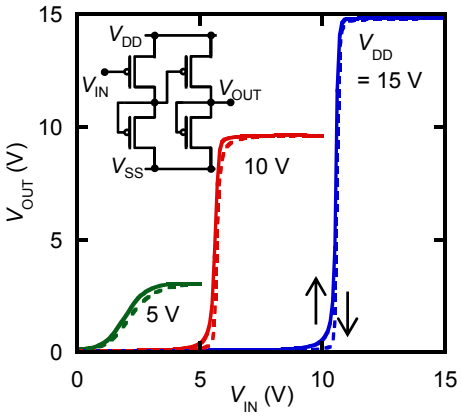

Figure 5
H. Takahashi et Al.