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A ring oscillator consisting of pentacene thin-film transistors with controlled threshold voltages

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Pentacene thin-film transistors (TFTs) with controlled threshold voltages have been applied to a ring oscillator consisting of enhancement/depletion inverters for evaluation of the dynamic characteristics. The threshold voltage control was demonstrated by using oxygen plasma treatment to the SiO_2 gate dielectric prepared by rf sputtering. The surface roughness of the SiO_2 gate dielectric depended on the sputtering condition. The use of flat SiO_2 gate dielectrics contributed to the improvement of the field-effect mobilities in pentacene TFTs. As a result, the ring oscillator operated at supply voltages of 15 to 25 V. The oscillation frequency was consistent with the result of circuit simulation for the ring oscillator.

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1. Introduction

Organic thin-film transistors (TFTs) have been expected to be used for applications such as flat-panel displays[1-9] and logic circuits.[10-15] The control of the threshold voltage in organic TFTs is a critical issue for the applications. As well as metal-oxide-semiconductor field-effect transistors (MOSFETs) of inorganic materials, the threshold voltage in organic TFTs is affected by the work functions of the gate electrodes[16-18] and the semiconductor[19,20], charges in the gate dielectric[21,22], dipole on the interface between the gate electrode and semiconductor[23-26], and potential change induced by voltage applied to additional electrodes.[27-29] Some groups have been attempting the control of the threshold voltage in organic TFTs on the basis of the effect mentioned above. Also, the change in parasitic resistance has been used for the control of threshold voltage.[30,31]

Oxygen plasma[32] and UV ozone treatments[33-35] have conducted to obtain a hydrophilic surface as pre-treatment for gate dielectrics in organic TFTs. Such a treatment causes excess charges on or close to the surface of the gate dielectric. Thus, it is possible that such a treatment is used for threshold voltage control. In fact, we have demonstrated the control of the threshold voltage in pentacene[36] and dinaphthothienothiophene (DNTT) [37] TFTs fabricated on Si substrates with thermally grown SiO_2 using oxygen plasma treatment to the surface of the gate dielectric. The method has the feature that it can continuously change threshold voltage with treatment time and needs no additional structure. Also, we have applied the method to the fabrication of pentacene TFTs having different threshold voltages on a same substrate.[38] As a result, we confirm the operation of inverters consisting of an enhancement- and a depletion-type pentacene TFT which are known as enhancement/depletion (E/D) inverters. However, the pentacene TFTs exhibited low mobilities of the order of 0.01 $cm^2\ V^{-1}\ s^{-1}$. In addition, the dynamic properties have not been clear, though the static input-output characteristics were observed. Thus, it is necessary to enhance the field-effect mobilities and confirm the dynamic properties. We have reported the operation of a ring oscillator consisting

of pentacene based E/D inverters without showing the reason of the improvement in the field-effect mobility and the stability of the operation.[39)]

In this paper, we report the improvement of the field-effect mobilities in pentacene TFTs having a SiO_2 gate dielectric fabricated on glass substrates. For realization of the improvement, the relationship between the surface flatness and the field-effect mobilities has been investigated. The SiO_2 gate dielectric was deposited by rf sputtering, and the surface was treated by oxygen plasma for control of the threshold voltage. Also, the relationship between the threshold voltage shift and the surface roughness was investigated. We fabricated ring oscillators consisting of E/D inverters and investigated the stability of the dynamic characteristics. The two-step surface treatment for the SiO_2 gate dielectrics was applied to fabrication of enhancement- and depletion-type pentacene TFTs on a same substrate. The frequency measured is compared with results of circuit simulation.

2. Experimental methods

Figure 1 shows the fabrication process of pentacene TFTs prepared for the investigation of the relationship between the surface flatness and the transistor characteristics. The pentacene TFT was fabricated on a glass substrate with a buffer layer. The buffer layer of SiO_2 or benzocyclobutene (BCB) polymer was adopted to obtain a flat surface. The SiO_2 layer was deposited at room temperature by rf sputtering using a SiO_2 target with 150 mm in diameter. The rf power was set at 400 W. The Ar and O_2 gases were used as sputtering gases. The flow rates of Ar and O_2 were set at 12 and 4 sccm (which denotes standard cubic centimeter per minute), respectively. The thickness of SiO_2 was about 140 nm. The BCB layer was deposited by spin coating. The coating condition was adjusted so that the BCB thickness would be close to the SiO_2 thickness. A Cr layer for the gate electrode was deposited on the glass substrate by thermal evaporation. Then, a SiO_2 gate dielectric was deposited using the same sputtering system as the SiO_2 buffer layer. Some deposition conditions were attempted to obtain flat

surface. The gas flow rates were mainly changed. The SiO_2 surface was treated with oxygen plasma. The AC power for plasma generation was set at 5.4 W. The treatment time t_P was set in the range between 10 and 120 s. After the oxygen plasma treatment, the substrate was immediately exposed to hexamethyldisilazane (HMDS) vapor to obtain a hydrophobic surface. A 45-nm-thick pentacene was deposited on the SiO_2 surface, and a Au layer was deposited for drain/source electrodes. The channel width was 1 mm, and the channel length was 40 μm. The deposition processes were performed at room temperature, and each layer deposited was patterned by use of a shadow mask.

The circuit for ring oscillators fabricated in this study was composed of five inverters for the oscillator and two inverters for an output buffer as seen in Fig. 2(a). The inverter consisted of an enhancement- and a depletion-type pentacene TFT respectively denoted by PMOS1 and PMOS2 in Fig. 2(b). Figure 2(c) shows cross section of the pentacene TFTs for the inverter. The circuit needs metal lines connecting between terminals of TFTs. In addition, it is necessary to fabricate TFTs with different threshold voltages on a same substrate. For the metal line, a Au layer with a Cr adhesive layer was deposited on a glass substrate with a BCB buffer layer before a Cr layer is deposited for a gate electrode. For fabrication of TFTs with different threshold voltage, two-step surface treatment for the SiO_2 gate dielectrics was adopted as shown in Fig. 2(d). The area for PMOS2 was exposed to the oxygen plasma through a shadow mask for a time t_P, and the entire area was exposed to UV/ozone for a time t_U. We have reported the similar method in reference 38. Other processes were the same as those mentioned in the paragraph above. The channel width was 600 μm, and the channel length was 40 μm.

The electric characteristics were measured in a dry-nitrogen glovebox at room temperature. The static characteristics of individual TFTs and inverters were examined using a semiconductor parameter analyzer. The output voltages of the ring oscillator were measured with using a digital oscilloscope with an active probe having an input impedance of 1 MΩ in parallel with 2 pF.

3. Surface morphology

To obtain flat surface, a SiO_2 or BCB layer was coated on a glass substrate. Figure 3(a) and 3(b) show atomic force microscope (AFM) images of glass substrates coated by SiO_2 and BCB layers, respectively. The surface of the glass substrate coated by the SiO_2 layer had grain structure with a size of about 50 nm. On the other hand, the surface of the glass substrate coated by the BCB layer exhibited no specific structure. The root mean square (RMS) of surface roughness was 0.69 nm for SiO_2 and 0.40 nm for BCB. The result indicates that the use of a BCB layer contributes to obtaining a flat surface. On the other hand, the use of a SiO_2 layer seems to have no effect on flatness. However, the sputtering condition for the SiO_2 buffer layer has not been optimized. Thus, the result does not preclude the use of a SiO_2 layer as a buffer layer.

Figures 4 shows AFM images of the SiO_2 gate dielectric deposited on a glass substrate with a Cr gate and a BCB buffer layer. The SiO_2 gate dielectric was deposited under some conditions. The rf power for the sputtering was fixed at 400 W. The Ar and O_2 flow rates were changed as seen in Table I. The sputtering time was not fixed at a certain time, and 10 or 15 min. The different sputtering time was adopted to confirm that the influence of sputtering time is not dominant. The morphology of the SiO_2 surface depends on the sputtering condition as seen in Fig. 4. The RMS surface roughness is shown with the sputtering time and the SiO_2 thickness in Table I. Reducing total gas flow rate seem to enhance the surface flatness regardless of SiO_2 thickness. The change of the morphology also appears in the difference of the RMS roughness. As a result, the minimum surface roughness of 0.32 nm was obtained under the conditions C3 and C4 of low gas flow rates.

In general, the properties of a film deposited by sputtering strongly depend on the sputtering system used. On the other hand, it has been reported that the surface roughness of a SiO_2 layer decreases by reducing the Ar flow rate.[40] Thus, it is possible that the relationship

between the gas flow rate and the surface roughness is an intrinsic phenomenon in sputtering deposition.

4. Transistor characteristics

To investigate the relationship between the surface roughness and the field-effect mobility, pentacene TFTs were fabricated on substrates of SiO_2 gate dielectrics with different surface roughness. The deposition conditions C1, C2, C3, and C4 shown in Table I were adopted for the investigation. The oxygen plasma treatment time t_P was fixed at 60 s. Figure 5 shows the field-effect mobility in the saturation regime (μ_{SAT}) versus surface roughness. The mobility was estimated by fitting a line to the $|I_D|^{1/2}$–V_G curves in the saturation regime. The plots shown in Fig. 5 show the average for five or more TFTs. The μ_{SAT} strongly depends on the deposition condition of the SiO_2 gate dielectric. The average μ_{SAT} values are 0.13 for C1, 0.27 for C2, 0.45 for C3, and 0.55 $cm^2\ V^{-1}\ s^{-1}$ for C4. The suppression of the surface roughness contributes to enhancement of the mobility regardless of the SiO_2 thickness. The μ_{SAT} of 0.55 $cm^2\ V^{-1}\ s^{-1}$ for C4 is close to that in the range of 0.57 to 0.85 $cm^2\ V^{-1}\ s^{-1}$of pentacene TFTs with controlled threshold voltages fabricated on Si substrate[36], and is close to a standard value of pentacene TFTs.[41]

To investigate the dependence of t_P on threshold voltages, pentacene TFTs were fabricated on substrates of SiO_2 gate dielectrics prepared under condition C4, and treated with different t_P. Figure 6(a) shows the transfer characteristics for pentacene TFTs with SiO_2 gate dielectrics with oxygen plasma for t_P = 10, 60, 90, and 120 s. The increase in t_P leaded to the shift of the transfer curve to positive gate voltage. The μ_{SAT} values estimated from transfer curves are shown in Fig. 6(b). The plots are the average value for ten or more TFTs, which are in the range of 0.43 to 0.58 $cm^2\ V^{-1}\ s^{-1}$. This indicates that oxygen plasma treatment in the range of t_P does not influence on the field-effect mobility. The tendency of the transfer curve and the field-effect mobility is similar to those of pentacene[36] and DNTT[37] TFTs fabricated on

Si substrates.

Figure 7(a) shows the threshold voltages estimated from transfer characteristics as a function of t_P. The closed or opened circles at $t_P = 0$ show the threshold voltage obtained from a pentacene TFT with a SiO_2 gate dielectric treated by UV/ozone instead of oxygen plasma. Since UV/ozone treatment does not affect threshold voltage, the value of the threshold voltage can be used as a reference.[38] The closed circles labeled as small roughness shows the threshold voltages of pentacene TFTs with SiO_2 gate dielectrics of a RMS roughness of 0.32 nm prepared under condition C4. The opened circle labeled as large roughness shows those of pentacene TFTs with SiO_2 gate dielectrics of a RMS roughness of 0.83 nm. The threshold voltage, for both cases, linearly shifts to positive voltages with respect to t_P. The line fitting to experimental data of closed and opened circles is expressed as V_{TH} = (0.058 V/s) t_P – 3.13 V and V_{TH} = (0.012 V/s) t_P – 4.03 V, respectively. Here, V_{TH} denotes the threshold voltage. The result indicates that threshold voltage shift is sensitive to oxygen plasma treatment in the case of SiO_2 gate dielectric with small roughness as compared with the case for large roughness. The sensitivity of the threshold voltage for small roughness is close to that of pentacene TFTs fabricated on Si substrates with thermally grown SiO_2.[36]

The threshold voltage shift can be explained by supposing that the oxygen plasma treatment induces negative surface charges on the SiO_2 gate dielectric. Figure 7(b) shows the surface charge density at the interface between the gate dielectric and pentacene as a function of t_P. The surface charge density Q_S was calculated from experimental V_{TH} using the following equation:

$$V_{TH} = \frac{\Phi_M - \Phi_S}{e} - \frac{1}{C_{OX}} Q_S , \quad (1)$$

where e is the electron elementary charge, C_{OX} is unit area capacitance of the gate dielectric, and Φ_M and Φ_S are the work functions of the gate electrode and the organic semiconductor, respectively.[41,42] The values of Φ_M = 4.5 eV for Cr gate [43] and Φ_S = 5.0 eV for pentacene [44]

were used for the calculation. Since the Qs linearly decreases with increases in t_P, it is assumed that the dependence of Q_S on t_P is expressed as

$$Q_S = Q_0 + q_P t_P, \quad (2)$$

where Q_0 is the intrinsic surface charge density and q_P is the surface charge density per unit time induced by oxygen plasma treatment. By fitting a line to Q_S in Fig. 7(b), Q_0 and q_P are estimated to be 81.4 nC cm^{-2} and –1.79 nC cm^{-2} s^{-1} for small roughness, and 88.3 nC cm^{-2} and –0.30 nC cm^{-2} s^{-1} for small roughness, respectively. On the other hand, the values of Q_0 = 113 nC cm^{-2} and q_P = –3.1 nC cm^{-2} s^{-1} have been obtained for pentacene TFTs fabricated on Si substrates with thermal oxide.[36] The RMS roughness of thermal oxide is about 0.2 nm. We have suggested that the origin of the surface charge induced by oxygen plasma treatment is electrons trapped at point defects with energy levels close to the valence band of SiO_2.[36] The surface roughness may suppress the generation of such point defects and decrease the density of electrons trapped. The origin of the surface charge has been under investigation.

5. Ring oscillator characteristics

We fabricated five-stage ring oscillators consisting of E/D inverters in order to confirm the dynamic properties and the stability of pentacene TFTs having controlled threshold voltages. A ring oscillator fabricated is shown in Fig. 2(e). The condition C4 shown in Table I was adopted for the gate dielectric of the pentacene TFTs in the ring oscillator. Transfer characteristics of typical pentacene TFTs are shown in Fig.S1 in the online supplementary data. The field-effect mobilities are 0.54 cm^2 V^{-1} s^{-1} for PMOS1 and 0.27 cm^2 V^{-1} s^{-1} for PMOS2. The values are close to those of the individual pentacene TFTs shown in Sect. 4. Also, the characteristics of an E/D inverter are summarized in Fig. S2 and Table SI.

Figure 8(a) shows the waveform of output voltage V_{OUT} measured and simulated for a ring oscillator operated at V_{DD} = 20 V. The blue line and red dotted one show measured and simulated waveform, respectively. The ring oscillator operated in the range of 15 to 25 V as

shown in Fig. S3. The oscillation frequency for V_{DD} = 15, 20, and 25 V were 252, 256, and 253 Hz, respectively. Although the frequency of a ring oscillator consisting of CMOS inverters increases with the supply voltage, that for E/D inverters generally does not exhibit such increase of the frequency. Thus, the tendency of the frequency measured in this study is not abnormal in a ring oscillator consisting of E/D inverters. Another concern is that the amplitude of V_{OUT} was less than the V_{DD}. This is because on-resistance for the output buffer was not sufficiently small with respective to the input impedance of the active probe. To confirm the validity of the frequency and output voltage, we conducted circuit simulation using a SPICE model. The condition of the simulation is shown in the supplemental data. The waveform of the simulation is similar to that of the measurement. Although the parasitic capacitance for the simulation was adjusted so that the frequency would be close to that of measurement, the value of the parasitic is not an unrealistic value. Thus, the frequency measured is in the reasonable range.

We also measured the change in the oscillation frequency of the ring oscillator to confirm the stability. Figure 8(b) shows the oscillation frequency as a function of measurement time. The oscillation frequency rapidly increased from about 250 Hz to about 290 Hz at the initial stage, and then gradually increased up to about 300 Hz for about 60 min. Probably, this is caused by changes in field-effect mobilities and/or threshold voltage. No large degradation in the frequency was observed at least.

6. Summary

We investigated the relationship between surface flatness and the characteristics of pentacene TFTs with controlled threshold voltages. Use of the flat SiO_2 gate dielectric contributed to enhancement of the field-effect mobilities and increased the sensitivity of threshold voltage shift to the oxygen plasma treatment time. We applied pentacene TFTs with improved characteristics for fabrication of ring oscillators. A ring oscillator operated at supply voltages in

the range of 15 to 25 V, and the frequency was about 250 Hz. The ring oscillator operated for about 60 min without large degradation at least. Thus, the threshold voltage control for organic TFTs by oxygen plasma treatment is expected to be used for more realistic circuits.

Acknowledgements

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Figure Captions

Fig. 1. (Color online) Fabrication process for pentacene TFTs with controlled threshold voltage fabricated on a glass substrate with a buffer layer.

Fig. 2. (Color online) (a) Circuit of a five-stage ring oscillator with an output buffer. (b) Circuit of an E/D inverter constructed using two PMOSs. (c) Cross section of a fabricated E/D inverter consisting of pentacene TFTs. (d) Schematic illustration of two-step surface treatment. (e) Photograph of a fabricated five-stage ring oscillator with an output buffer consisting of two inverters.

Fig. 3. (Color online) AFM images of glass substrates coated with (a) a SiO_2 buffer layer and (b) a BCB buffer layer.

Fig. 4. (Color online) AFM images of SiO_2 gate dielectrics deposited under conditions: (a) C1, (b) C2, (c) C3, and (d) C4 for which the sputtering gas flow rates of Ar and O_2 are 12/4, 9/3, 3/1, and 2/ 1 sccm, respectively.

Fig. 5. Field-effect mobilities in the saturation regime versus RMS surface roughness of the SiO_2 gate dielectrics for pentacene TFTs prepared under conditions of C1 to C4. The oxygen plasma treatment time was 60 s.

Fig. 6. (Color online) (a) Transfer characteristics and (b) field-effect mobilities in the saturation regime of TFTs prepared under a condition of C4. The oxygen plasma treatment times are between 10 and 120 s.

Fig. 7. (Color online) (a) Threshold voltages of TFTs fabricated on SiO_2 gate dielectrics with

small roughness and large roughness. The TFTs for small roughness corresponds to TFTs for Fig. 6(a). (b) Surface charge density estimated from the threshold voltage in (a) as a function of treatment time.

Fig. 8. (Color online) (a) Output voltages measured (blue line) and simulated (red dotted line) for a five-stage ring oscillator with an output buffer. The supply voltage V_{DD} is 20 V. (b) Oscillation frequency as a function of operation time of the ring oscillator.

Table I.

Thickness, unit area capacitance C_{OX}, and RMS surface roughness of SiO_2 layers deposited under different conditions.

Condition	Ar (sccm)	O_2 (sccm)	Time (min)	Thickness (nm)	C_{OX} (nF/cm^2)	Roughness (nm)
C1	12	4	15	140	27	0.63
C2	9	3	10	80	51	0.60
C3	3	1	10	90	46	0.32
C4	2	1	15	130	31	0.32

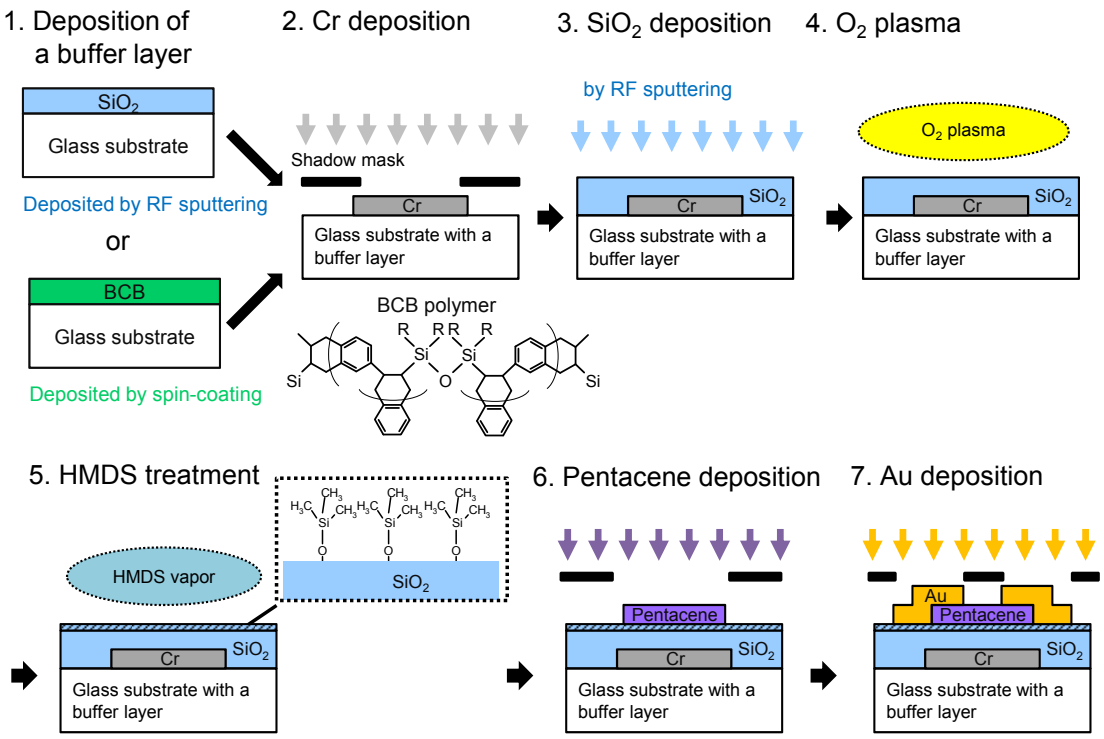

Fig. 1
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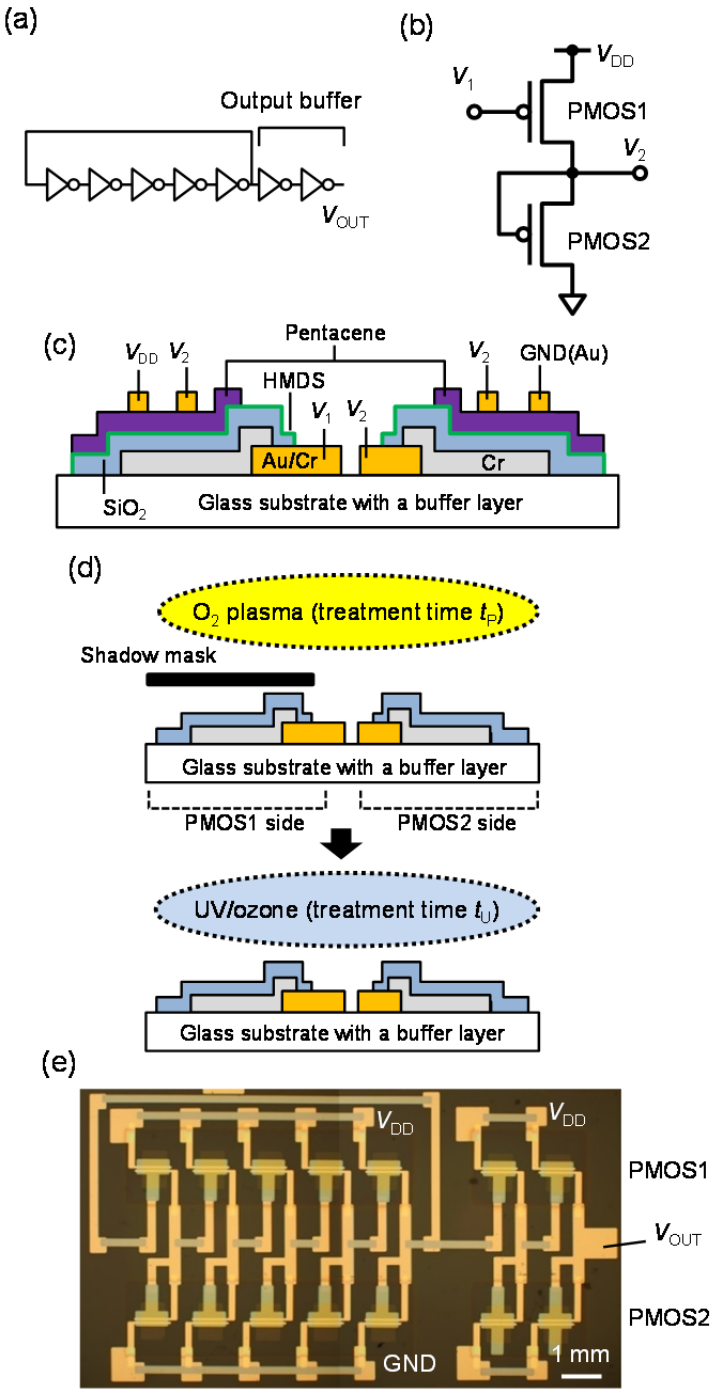

Fig. 2
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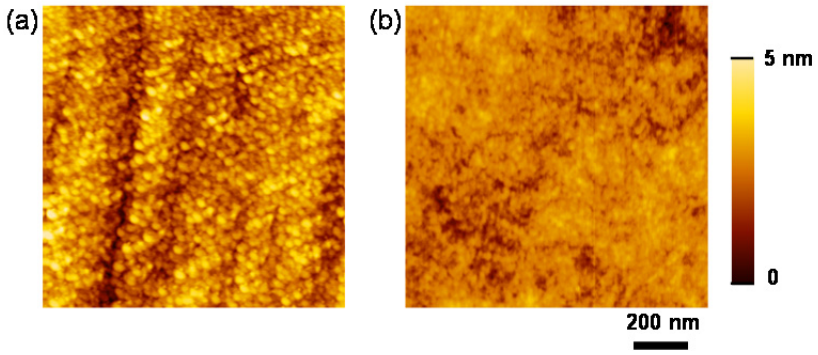

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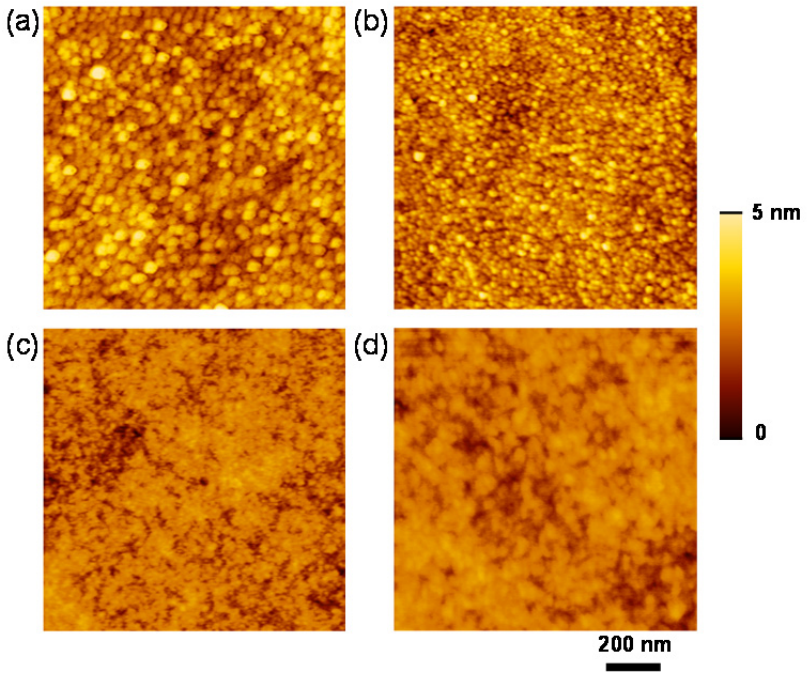

Fig. 4
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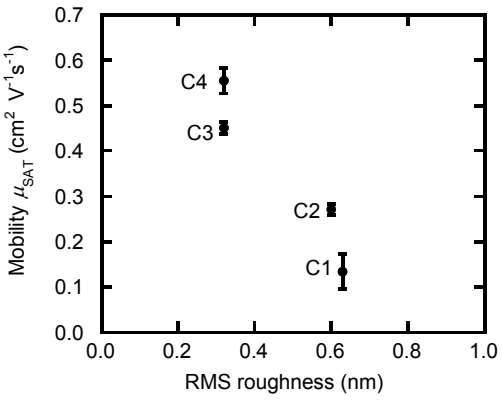

Fig. 5
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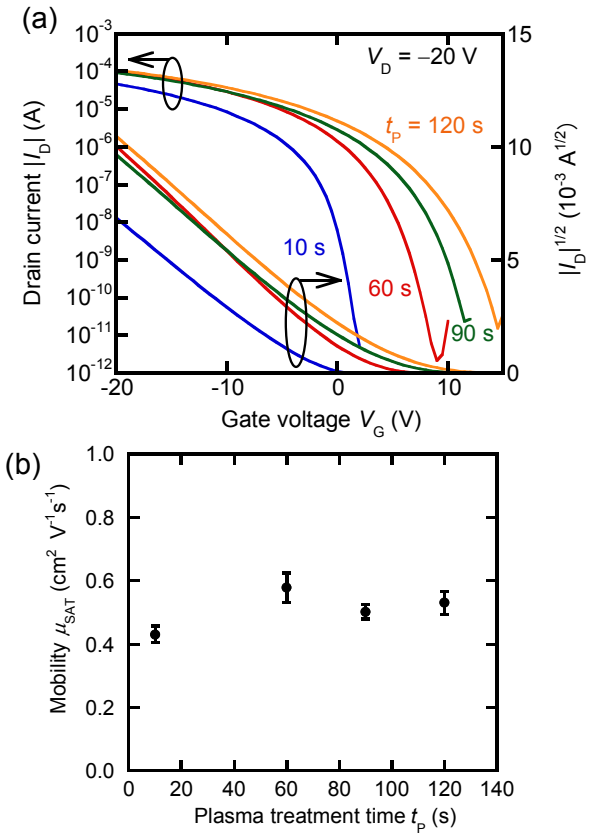

Fig. 6
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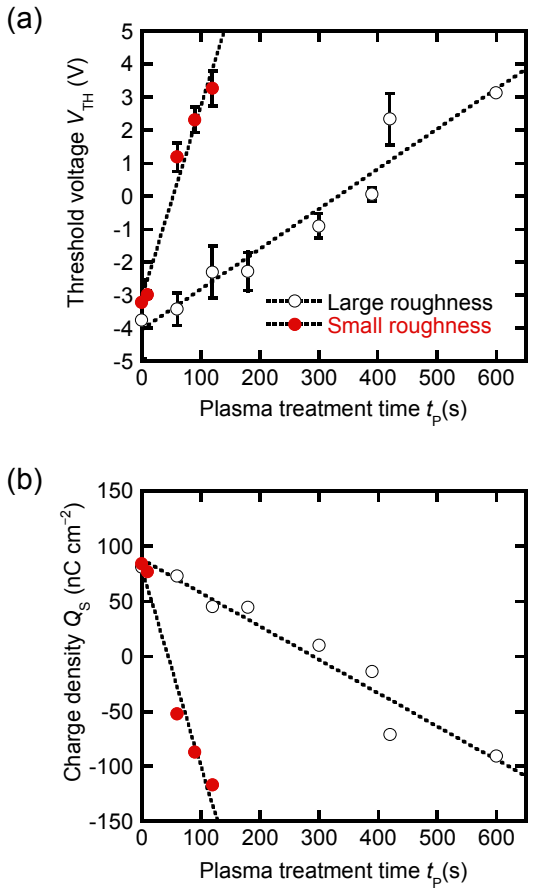

Fig. 7
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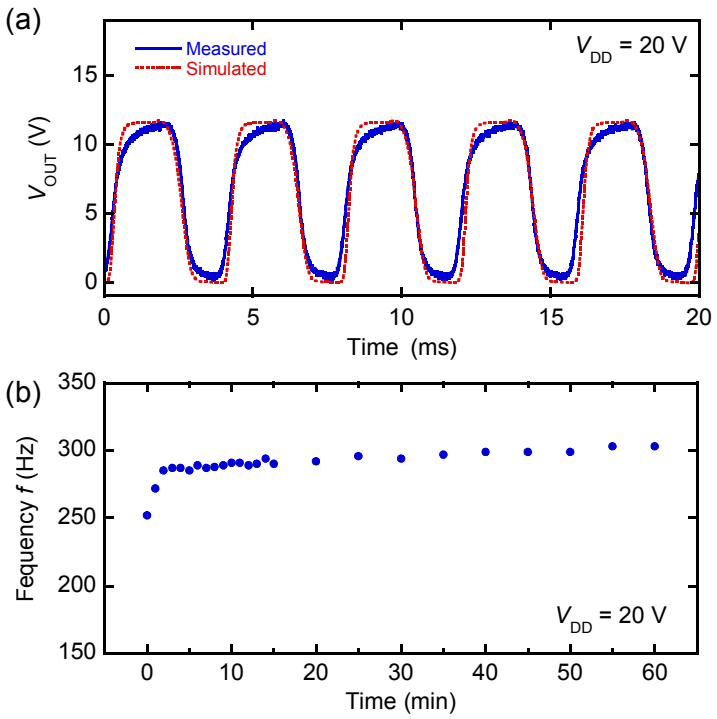

Fig. 8
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A ring oscillator consisting of pentacene thin-film transistors with controlled threshold voltages

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Supplementary data

1. Characteristics of pentacene TFTs for a ring oscillator

Figures S1(a) and S1(b) show the transfer characteristics of pentacene TFTs fabricated as an enhancement-type PMOS1 and a depletion-type PMOS2, respectively. The surface treatment for the SiO_2 gate dielectric was t_U = 15 min for PMOS1 and t_P = 180 s for PMOS2. The transfer characteristics exhibited no large hysteresis in forward and reverse sweeps as seen in Fig. S1. The field-effect mobility and threshold voltage estimated from the transfer characteristics are 0.54 cm^2 V^{-1} s^{-1} and –2.5 V for PMOS1, and 0.27 cm^2 V^{-1} s^{-1} and 8.8 V for PMOS2, respectively. The field-effect mobility for PMOS2 was slightly low as compared with those in Fig. 6(b). This may be caused by two-step surface treatment.

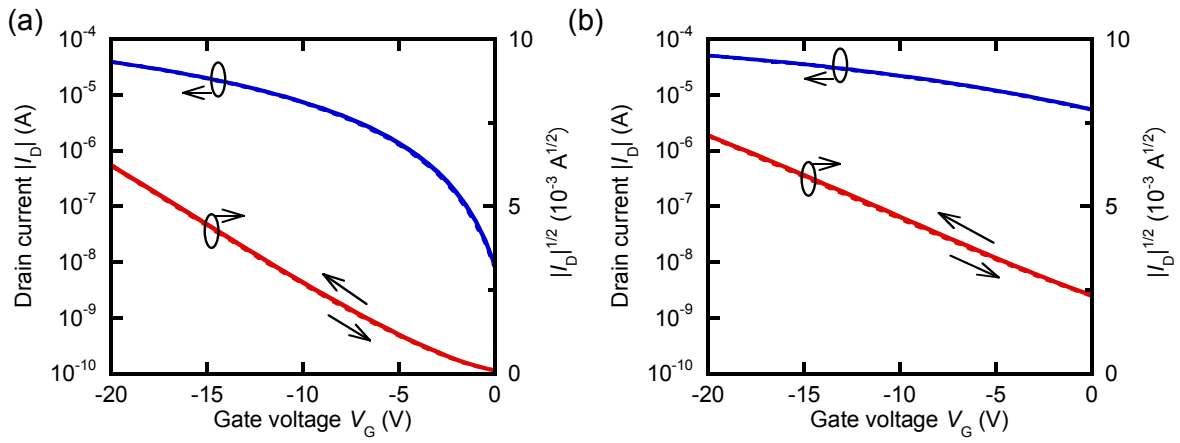

Fig. S1. The transfer characteristics of pentacene TFTs fabricated as (a) an enhancement-type PMOS1 and (b) a depletion-type PMOS2.

2. Characteristics of an E/D inverter

Figures S2 show the transfer characteristics of an E/D inverter measured at supply voltages of 5, 10, 15, and 20 V. The transfer characteristic did not exhibit no large hysteresis as well as those of individual pentacene TFTs. The characteristics for the E/D inverter are summarized in Table SI.

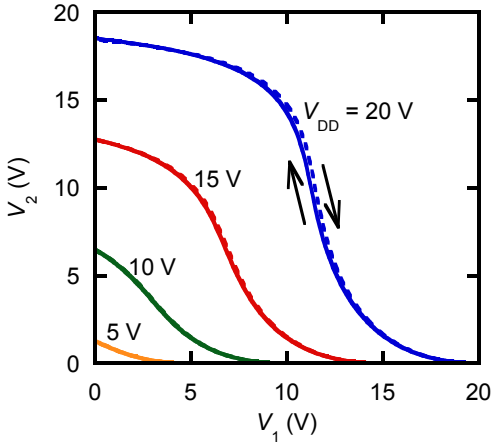

Fig. S2. Input/output characteristics of an E/D inverter measured at V_{DD} = 5, 10, 15, and 20 V.

Table SI. Switching voltages V_S, maximum gain, high noise margin NM_H, and low noise margin NM_L of the E/D inverter corresponding to Fig. S2.

V_{DD} (V)	V_S (V)	Maximum gain	NM_H (V)	NM_L (V)
5	-	-	-	-
10	1.8	–1.3	1.0	-
15	6.4	–2.6	1.1	2.6
20	11.3	–5.2	1.0	7.1

3. Output characteristics of a ring oscillator

Figure S3 shows the waveforms of output voltage V_{OUT} measured for a five-stage ring oscillator with an output buffer. The oscillation frequency for V_{DD} = 15, 20, and 25 V were 252, 256, and 253 Hz, respectively. The amplitude for V_{DD} = 15, 20, and 25 V were about 5.8, 11.5, and 16.2 V, respectively. The amplitude is quit small as compared with V_{DD}. This is because PMOS1 in the second stage of the output buffer did not have small on-resistance as compared with the input resistance of the active probe. Since the active probe with an input resistance of 1 MΩ was used for the measurement, the on-resistance was roughly estimated to be 1.6 MΩ for V_{DD} = 15 V, 700 kΩ for V_{DD} = 20 V, and 500 kΩ for V_{DD} = 25 V from the amplitude of V_{OUT} measured. The drain current of PMOS1 at V_D = –20 V is of the order of 10^{-5} A as seen in Fig. S1. Thus, the estimated value of the on-resistance for the output buffer is realistic.

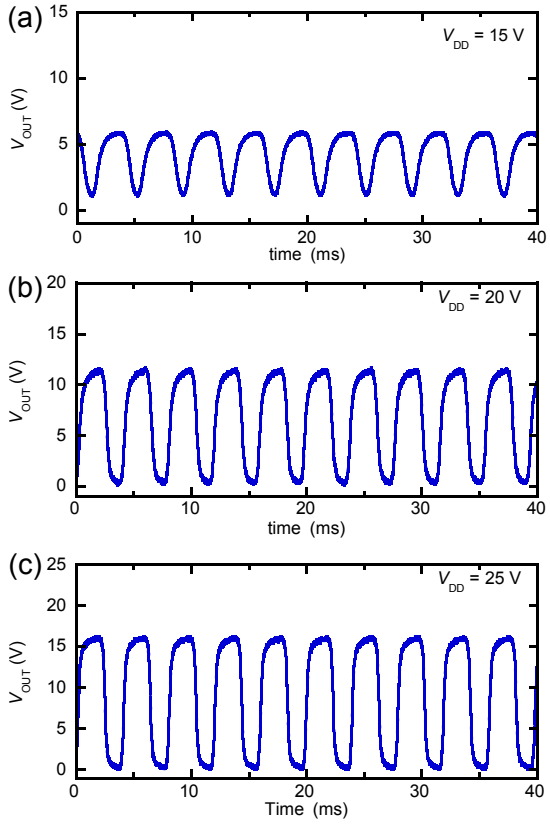

Fig. S3. Waveforms of output voltage V_{OUT} measured for a five-stage ring oscillator at V_{DD} = (a) 15, (b) 20, and (c) 25 V.

4. SPICE simulation

To conduct circuit simulation for a ring oscillator, we used a software, LTspice® XVII. We simulated a circuit corresponding to Fig 2(a) appending a resistance of 1 MΩ and a capacitor of 2 pF in parallel to the terminal for V_{OUT}. Level 3 was selected for MOSFET, which is a semi-empirical model. Thus, the simulation does not include characteristics in sub-threshold region. The parameters used are summarized in Table SII. The field-effect mobility and threshold voltage for the output buffer are different from those for ring the oscillator. This is because we considered the in-plane distribution of field-effect mobility and threshold voltage. The gate-source and gate-drain capacitances were adjusted so that the oscillation frequency simulated would be close to that measured. The value is equal to 82% of capacitance estimated from the area of gate electrode covered with a contact electrode and the organic layer on the contact electrode side. Since carriers are not always accumulated in the organic layer, the capacitance used for the simulation is relatively reasonable.

Table SII. Parameters used for the SPICE simulation.

Model parameter	Notation	Ring oscillator		Output buffer	
		PMOS1	PMOS2	PMOS1	PMOS2
Channel width (μm)	W	600	600	600	600
Channel length (μm)	L	40	40	40	40
Gate capacitance per unit area (nF/cm^2)	C_{OX}	31	31	31	31
Field-effect mobility (cm^2 V^{-1} s^{-1})	μ	0.54	0.27	0.41	0.33
Threshold voltage (V)	V_{TH}	–2.5	8.8	–3.0	10.8
Drain-source shunt resistance (GΩ)	R_{DS}	200	200	200	200
Gate-source overlap capacitance (pF)	C_{GS}	29.5	52.4	29.5	52.4
Gate-drain overlap capacitance (pF)	C_{GD}	52.4	29.5	52.4	52.4