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Dependence of Double Layer Capacitance on Pore Diameter of Carbon Coated Porous Si

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Carbon coated porous silicon with various pore sizes as a model of porous electrode was prepared for Electric double layered capacitors (EDLCs). Each carbon coated PSi has a diameter ranged from 7 to 72 nm. The specific capacitance was influenced the diameter of main chain observed surface SEM images. The calculated capacity of each electrode depends on the pore distribution which showed the overlapping the electronic double layer.

Introduction

Recent remarkable progress of various electric devices, there are much more demands on large electric energy. Electrochemical supercapacitors are rechargeable energy storage devices with high-speed charge and discharge characteristics, high power density and long cycling stability (1). Electric double layer capacitors (EDLCs) are a kind of supercapacitors. EDLC performs charging and discharging by adsorption and desorption of ions to the electrode surface and with no redox reaction of active material. Since the capacity of EDLC is expressed by this equation;

$$C = \varepsilon S / d \qquad (1)$$

Where C is capacitance, ε is permittivity, S is surface area of electrode d is the distance of electrodes, respectively. The capacity is proportional to the surface area of the electrode, a material with large specific surface area such as porous material is used for electrode of EDLC. However, it is known that the properties of porous electrode differ from planer electrode in terms of overlapping of double layer (2), concentration gradient, desolvation (3) and so on.

Porous silicon (PSi) can be fabricated by anodization of single crystal silicon wafers with hydrofluoric acid including electrolyte (4,5). Additionally, the pore size of porous silicon can be controlled by changing anodization parameters such as concentration of hydrofluoric acid and current density (6). For the various characteristics of porous silicon, applications for solar cells (7), biosensors (8), photoluminescence materials (9) and electrode of batteries (10). Since porous silicon surface is chemically unstable, utilization of porous silicon for energy storage using electric double layer is unfavorable. In order to solve this problem, in the past report, coating graphitic carbon on porous silicon through chemical thermal process was attempted, and improved chemical stability and electrochemical performance drastically (11, 12).

In this study, we used carbon coated porous silicon with various pore size as model system of porous electrode of EDLC, and researching dependence of double layer capacitance on pore diameter.

Experimental

Porous silicon preparation

Porous silicon (PSi) with various pore diameters were prepared by anodizing of highly antimony doped silicon wafers (~0.02 Ωcm^{-1}) in a homemade electrochemical etching cell using hydrofluoric acid/ethanol mixture as electrolyte for 3 minutes. The HF concentration was varied in 14.8-31.1 wt% and the current range was 100-200 mA cm^{-2}. After etching, PSi was rinsed with ethanol and dried under vacuum for overnight.

Carbon coated PSi preparation

For the carbon coating process, the PSi prepared above process was used. The carbon coating process was proceeded along the past reports (11, 12) using tube furnace with a quartz tube (Fig. 1). Samples were set on the quartz plate and placed in the center of the quartz tube. Samples were heated to 650 ˚C in 20 min in reductive atmosphere of flowing 1 $Lmin^{-1}$ of Ar and 200 mL min^{-1} of H_2 under atmospheric pressure. Then, 20 $mLmin^{-1}$ of C_2H_2 was added to gas mixture and samples were heated to 850 ˚C by 10˚C min^{-1}. When the temperature reached 850 ˚C, C_2H_2 was stopped and samples were cooled to room temperature. To observing surface morphology of the PSi and carbon coated PSi, we used field emission scanning electron microscopy (FESEM; JEOL Ltd., JSM-6335F). Raman spectroscopy measurement (Horiba Ramanor T-64000 spectrometer) was carried out to confirm carbon coating on PSi surface. Then, surface area of the carbon coated PSi was obtained from N_2 isotherm physisorption analysis (Quantachrome INSTRUMENTS, High speed gas sorption analyzer NOVA 2200e/2000e).

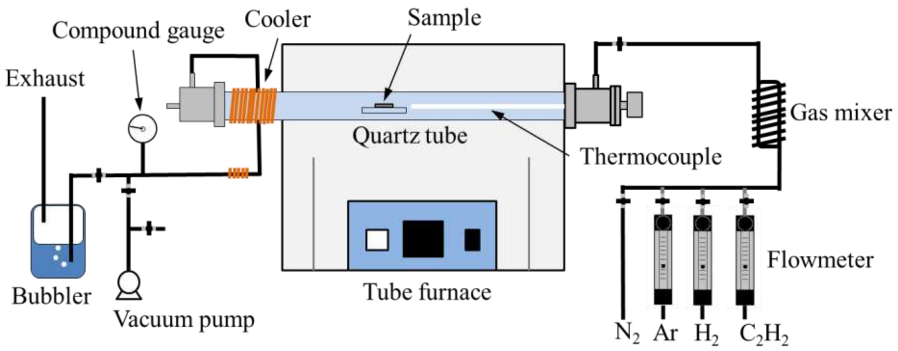

Fig. 1 Diagram of equipment used for CVD process.

Electrochemical measurement

Two electrode electrochemical supercapacitors were fabricated by using PSi and carbon coated PSi samples. Trimethylpropylammnium bis(trifluoromethane-sulfonyl) amide ionic liquid was synthesized following the past report (13), and it was used for electrolyte. To infiltration the electrolyte, electrolyte loaded samples were set to under vacuum for overnight. After that, samples were sandwiched into a homemade two electrode test cell separated by cellulose filter. Cyclic voltammetry was carried out at the scan rate of 25 mV sec^{-1} and sweep range -3.0 V to 3.0 V. And then, specific capacitance was calculated by these equations at the range of -2.0 to 2.0 V.

$$\Delta Q = \int C_{dif}\, V\, dV \qquad (2)$$

$$I = C_{dif}\, a \qquad (3)$$

Where ΔQ , V, C_{dif} and a are total capacity, applied potential, differential capacitance and scan rate, respectively. Electrochemical impedance spectroscopy was measured at 0 V with amplitude 10 mV and frequency 10 MHz to 0.01 Hz. All electrochemical measurement was performed at 25 ˚C. Compact Stat Plus (Ivium technologies) was used for electrochemical measurement.

Results and discussion

Characterization for prepared porous silicon samples

SEM images of porous silicon and carbon coated porous silicon material are shown in

Fig. 2. No obvious structural changes were confirmed after carbon coating. We carried out Raman spectroscopy to confirm carbon coating on porous silicon. In the Raman spectra of before carbon coated porous silicon, only Si peak around 520 cm^{-1} was observed. In the spectra of carbon coated porous silicon, the peak of Si almost disappeared, and two peaks attributable to sp^2 and sp^3 hybridized carbon orbits were observed at 1350 cm^{-1} and 1600 cm^{-1}, respectively, as shown in Fig.3. It is indicated that graphitic carbon with some structural defects was coated on porous silicon.

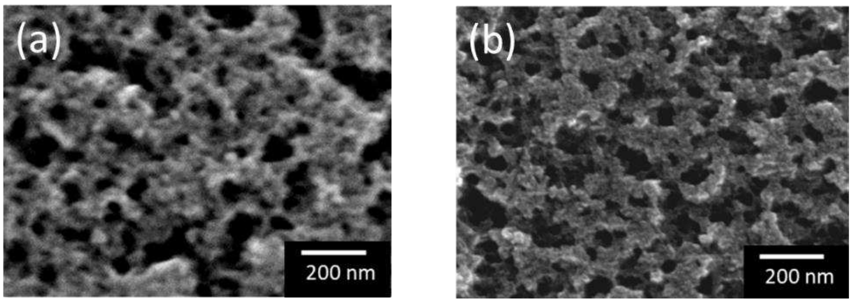

Fig. 2 SEM images of typical samples of (a) porous silicon and (b) carbon coated porous silicon.

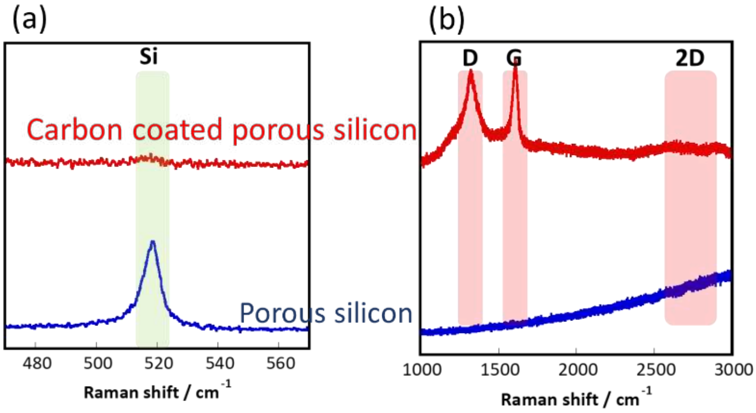

Fig. 3 Raman spectra for porous silicon and carbon coated porous silicon.

Surface SEM images and pore size distribution of carbon coated porous silicon with various pore diameter are shown in Figures 4 and 5. From the surface observation, it was confirmed each carbon coated porous silicon has 7 to 72 nm pore. On the other hand, these results of N_2 isotherm physisorption analysis indicate that there are many holes of about 4 nm in addition to the pores visible from the surface, and this is because the pores of porous silicon are not straight holes but have branched structure. The relationship between pore diameter and specific surface area is table I.

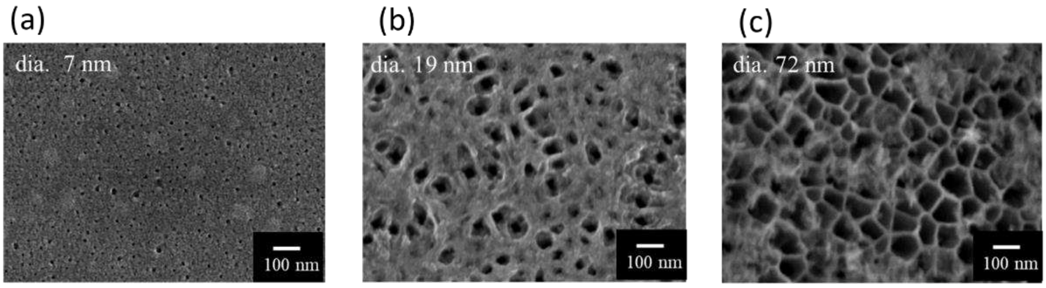

Fig. 4 SEM images of carbon coated porous silicon with various pore diameter.

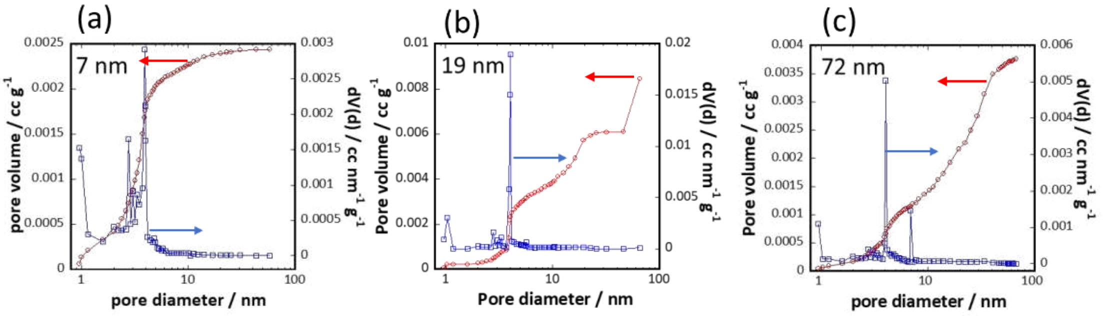

Fig. 5 Pore size distribution of carbon coated porous silicon with diameter 7 nm (a), 19 nm (b) and 72 nm, respectively.

Table I. Relationship between pore diameter and specific surface area.

Surface diameter / nm	Specific surface area / m^2 g^{-1}	Porous layer thickness /μm
7	2.74	20.9
11	2.34	23.2
19	3.42	28.3
33	0.78	12.6
43	2.20	20.1
72	1.43	22.7

Electrochemical measurement

Cyclic voltammograms for each samples and specific capacitance calculated from equation 1 are shown in figure 6a. In the case of pore diameter above 19 nm, specific capacitances of each samples were above 10 μF cm^{-2}. On the other hand, specific capacitance of pore diameter 7 and 11 nm were extremely low of 0.01 and 0.40 F cm^{-2}, respectively (Figure 6b). Even though each sample has pore around 4 nm, specific capacitance was affected by the pore size distribution by N_2 adsorption, i. e., micropore does not contribute to electric capacitance in the case of carbon coated porous silicon with diameter 7 nm indicated in Figure 5a. It is suggested that electronic double layer overlapped in the smaller pore (2). Specific capacitance will decrease as the electric field weakens due to overlapping of the electronic double layers. And the contribution to specific capacitance was not the branched structure confirmed N_2 adsorption but main chain observed surface SEM images. When the electronic double layer thickness larger than the radius of the pore, the electronic double layer will overlap. Thus, the electronic double layer in this case is considered to be longer than 5.5 nm and shorter than 9.5 nm. Then, to confirm the influence of pore size for specific capacitance, we performed electrochemical impedance spectroscopy measurement for the samples with pore diameter of 11 nm and 43 nm (Figure 7), and higher resistivity thought to solution resistance in the smaller pore was confirmed in smaller pore, 11 nm pore sample. Higher resistivity by solution resistance suggests overlapping of the double layer in nanopore, and it corresponds to the low specific capacitance calculated from cyclic voltammograms by eq. 2.

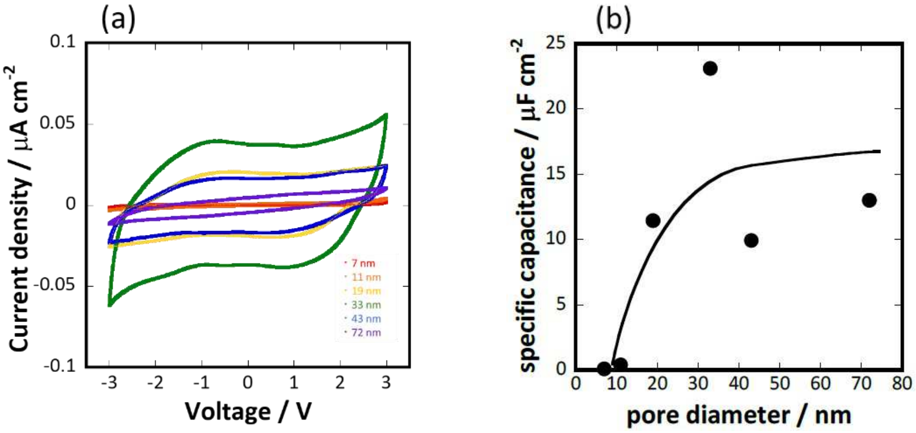

Fig. 6 cyclic voltammograms for carbon coated porous silicon at the scan rate of 25 mV sec^{-1} (a) and specific capacitance calculated from eq. 2 (b).

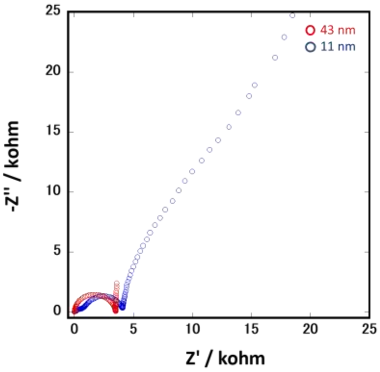

Fig. 7 Electrochemical impedance spectroscopy measurement for 11 nm and 43 nm pore.

Conclusions

We prepared carbon coated PSi with various pore diameter. Each carbon coated PSi had around the diameter of 4 nm derived branched structure in addition to the pore from observation of PSi surface. From the results of the electrochemical measurement, the specific capacitance was influenced the diameter of main chain observed surface SEM images. Therefore, it is suggested the thickness of the electronic double layer in this case is longer than 5.5 nm and 9.5 nm.

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