A 11.3-μA Physical Activity Monitoring System Using Acceleration and Heart Rate

Nakanishi, Motofumi ; Izumi, Shintaro ; Tsukahara, Mio ; Kawaguchi, Hiroshi ; Kimura, Hiromitsu ; Marumoto, Kyoji ; Fuchikami, Takaaki ;…

(Citation)
IEICE Transactions on Electronics,E101.C(4):233-242

(Issue Date)
2018-04-01

(Resource Type)
journal article

(Version)
Version of Record

(URL)
https://hdl.handle.net/20.500.14094/90007078

PAPER Special Section on Solid-State Circuit Design — Architecture, Circuit, Device and Design Methodology

A 11.3-μA Physical Activity Monitoring System Using Acceleration and Heart Rate

Motofumi NAKANISHI[†,††a)], ***Nonmember***, **Shintaro IZUMI**[††], ***Member***, **Mio TSUKAHARA**[††], ***Nonmember***, **Hiroshi KAWAGUCHI**[††], **Hiromitsu KIMURA**[†††], ***Members***, **Kyoji MARUMOTO**[†††], **Takaaki FUCHIKAMI**[†††], **Yoshikazu FUJIMORI**[†††], ***Nonmembers***, ***and*** **Masahiko YOSHIMOTO**[††], ***Fellow***

SUMMARY This paper presents an algorithm for a physical activity (PA) classification and metabolic equivalents (METs) monitoring and its System-on-a-Chip (SoC) implementation to realize both power reduction and high estimation accuracy. Long-term PA monitoring is an effective means of preventing lifestyle-related diseases. Low power consumption and long battery life are key features supporting the wider dissemination of the monitoring system. As described herein, an adaptive sampling method is implemented for longer battery life by minimizing the active rate of acceleration without decreasing accuracy. Furthermore, advanced PA classification using both the heart rate and acceleration is introduced. The proposed algorithms are evaluated by experimentation with eight subjects in actual conditions. Evaluation results show that the root mean square error with respect to the result of processing with fixed sampling rate is less than 0.22 [METs], and the mean absolute error is less than 0.06 [METs]. Furthermore, to minimize the system-level power dissipation, a dedicated SoC is implemented using 130-nm CMOS process with FeRAM. A non-volatile CPU using non-volatile memory and a flip-flop is used to reduce the stand-by power. The proposed algorithm, which is implemented using dedicated hardware, reduces the active rate of the CPU and accelerometer. The current consumption of the SoC is less than 3-μA. And the evaluation system using the test chip achieves 74% system-level power reduction. The total current consumption including that of the accelerometer is 11.3-μA on average.

key words: *adaptive sampling, normally off computing, physical activity classification, sensor fusion, SoC*

1. Introduction

Recently, lifestyle diseases have come to pose an important social issue, highlighting the importance of lifestyle disease prevention. To support prevention efforts, monitoring of physical activity intensity (PAI) during daily lifestyle activities has become extremely important. Such measurements must monitor PAI data continuously and longitudinally. Coleman *et al*. [1] reported that long-term monitoring can reveal differences deriving from changes in health status. Ensuring correct long-term PAI data and step counting is one method for monitoring and confirming lifestyle improvements. Such data can also improve health guidance to facilitate lifestyle disease prevention. Accordingly, strong demand persists for devices to monitor lifestyle habits in terms of PAI data.

Recently, many wearable devices have been proposed for PAI monitoring [2]–[4]. However, the size and battery life of such devices must be improved to enhance their usability. A tradeoff exists between device size and battery capacity. Especially, short battery life is an extremely important issue to address for long-term PAI monitoring and continuous recording. Reducing the power consumption is one means to lengthen battery life. So we develop a low-power and high-accuracy algorithm and a System-on-a-chip (SoC) to implement the algorithm.

Generally, an accelerometer is used for PAI estimation [5]–[9]. To improve the estimation accuracy, a physical activity (PA) classification algorithm incorporating heart rate and tri-acceleration signals was proposed in the previous work [10]. The previous algorithm classifies locomotive activities into a high-intensity group (HIG) and middle-intensity group (MIG) using percentage Heart Rate Reserved (%HRR). Algorithm results demonstrate its availability for improving the estimation accuracy of Metabolic Equivalents (METs).

To implement the previous algorithm [10], a low-power heart rate monitoring SoC using the normally-off computing technology was produced [11]. Although this SoC can reduce the stand-by power and heart rate sensing power, a difficulty arises: the power consumption of the external acceleration sensor remains high. To overcome this issue, an adaptive sampling method for acceleration signal processing was proposed in our earlier study [12]. As another adaptive sampling method, a US Patent [13] by Seiko has also been proposed. The adaptive acceleration sampling method can reduce the average power consumption without decreasing the PAI estimation accuracy. Results of PA classification and the standard deviation of the acceleration signal are used for sampling rate optimization.

This study proposes a PA classification and METs estimation algorithm combining the two algorithms described above [10], [12] to achieve both low power consumption and higher estimation accuracy. The proposed algorithm is implemented in a dedicated SoC to minimize the power consumption.

A preliminary version of this work has been published [14]. The Ref. [14] only proposed adaptive sampling implementation and evaluation with only a few subjects. On the other hand, this paper describes the novel algorithm using both the heart rate and the accelerometer and SoC im-

Manuscript received July 28, 2017.
Manuscript revised December 18, 2017.

[†]The author is with Omron Healthcare Co., Ltd., Muko-shi, 617–0002 Japan.
[††]The authors are with the Graduate School of System Informatics, Kobe University, Kobe-shi, 657–8501 Japan.
[†††]The authors are with Rohm Co. Ltd., Kyoto-shi, 615–8585 Japan.
a) E-mail: motofumi_nakanishi@ohq.omron.co.jp

DOI: 10.1587/transele.E101.C.233

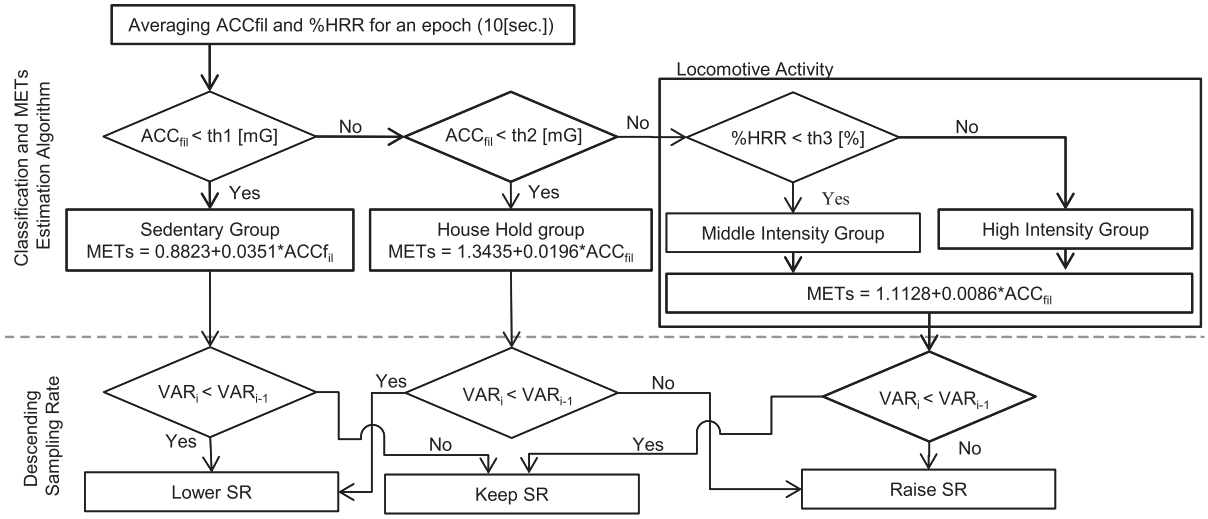


Fig. 1 Flow chart of PA classification, METs estimation and deciding sampling rate.

plementation, and presents evaluation results.

2. PA Classification and METs Estimation

The decision tree proposes in this study is shown in Fig. 1. The algorithm which classifies the PA group and estimates METs uses adaptive sampling. This algorithm uses two indexes: filtered synthetic acceleration (ACC_{fil}) and percentage heart rate reserve (%HRR). The PA is classified into three groups: sedentary, household, and locomotive. Using %HRR in addition to acceleration, the locomotive activity is classifiable further into two sub-groups: high intensity group (more than 6 METs) and middle intensity group (less than 6 METs). By doing that, a PA with lower estimation accuracy, such as stair ascent, is expected to be improved.

The measured triaxial acceleration is processed in the same manner as that described for our fundamental studies [15], [16]. First, each signal from the triaxial accelerometer was passed through a high-pass filter with a 0.7 Hz cutoff frequency to remove the gravitational acceleration component. Next, synthetic acceleration along the three axes (vector magnitude $\sqrt[2]{X^2 + Y^2 + Z^2}$) is calculated.

Then, ACC_{fil} was defined as the mean value of the synthetic acceleration in each epoch. An epoch is a period for conducting PA classification and METs estimation. For this study, it is defined as 10 [sec.]. Furthermore, to decide the sampling rate, VAR_i denotes the variance of the synthetic acceleration in the same epoch. VAR_{i-1} represents the value of VAR in the prior epoch.

Our methodology uses %HRR to increase the classification numbers, as presented in Eq. (1).

$$\%HRR = \frac{HR_{act} - HR_{rest}}{HR_{\max} - HR_{rest}} \times 100 \tag{1}$$

The heart rate beats per minute [bpm] was converted from the recorded R–R interval. The heart rate during activity (HR_{act}) represents the mean value of the averaged heart rate in every epoch. The heart rate at rest (HR_{rest}) was defined as the mean value of the averaged heart rate in a seating situation. The maximum heart rate ($HR_{\max}$) was calculated using the Karvonen formula (Eq. (2)).

$$HR_{\max} = 220 - Age \tag{2}$$

Although conventional methods [15], [16] have used a fixed sampling rate, they entail constant power consumption. This paper presents the adaptive acceleration sampling to reduce the active rate of a monitoring system and the average power consumption without decreasing its estimation accuracy. The lower sampling rate is acceptable if the PA intensity is low [12]. As presented in Fig. 1, the sampling rate is chosen automatically according to the past indexes of synthetic accelerations. The values of ACC_{fil}, VAR_i, and VAR_{i-1} respectively show that the system raises, lowers, and maintains the sampling rate for the subsequent epoch. The sampling rate during locomotive activity is defined as the base sampling rate (BSR). The variation of the sampling rate in the proposed adaptive sampling algorithm is chosen as 50%, 25%, or 12.5% of the sampling rate for that BSR. The sampling rate on each epoch changes to one of those at the end of epoch.

When the sampling rate is changed, coefficients and delay values in the high-pass filter should be adjusted for the subsequent sampling rate. Delay values in the Butterworth filter are calibrated by multiplying the coefficients directly to the delay values. Details are described in Sect. 3.

3. Hardware Implementation

The proposed algorithm is implemented into the SoC. Figure 2 portrays a block diagram of the SoC, which contains a heart rate sensor, an accelerometer interface, a non-volatile CPU (NV-CPU), oscillators, a timer block, and dedicated hardware intended for the proposed algorithm. The SoC is designed to maximize the effect of low active rate using

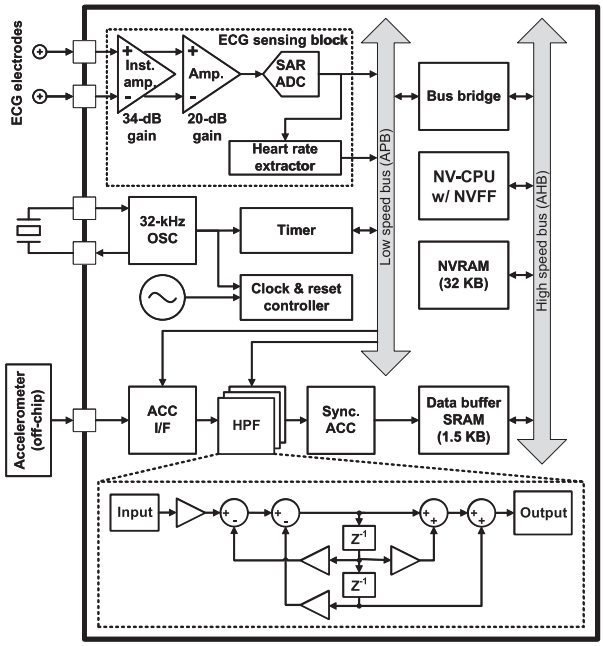


Fig. 2 Block diagram of the proposed SoC.

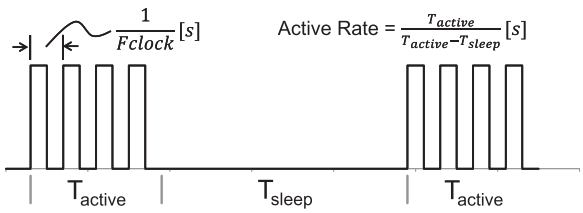


Fig. 3 Example of active state and sleep state.

the proposed algorithm in Sect. 2. To implement METs estimation and PA classification with the adaptive sampling algorithm into a small and low-power sensor device, a NV-CPU is introduced [11]. The NV-CPU, which integrates of a non-volatile memory (NVRAM) and a non-volatile flip-flop (NVFF) based on a ferroelectric capacitor, can retain memory and register data when its power source is gated. Figure 3 shows that T_{active} is the period of the active state in which power source is supplied. Furthermore, T_{sleep} is the period at which the power source is gated, so that the power consumption during T_{sleep} is zero. The active rate is calculated as shown in Eq. (3).

$$\text{Active Rate} = \frac{\text{T}_{\text{active}}}{\left(\text{T}_{\text{active}} + \text{T}_{\text{sleep}}\right)} \tag{3}$$

Reducing the active rate is an effective power reduction approach for biosignal monitoring because the biosignal including acceleration has much lower frequency than that of the CPU. Table 1 summarizes the active rate of each function block on the SoC. The active rate of NV-CPU and ADC in ECG sensing block are remarkably low, 0.1% and 2.14%, respectively. Especially, the low active rate of NV-CPU contributes to low power consumption because NV-CPU consumes higher power than other function blocks. To reduce

Table 1 Active rate of each function block

Function Block		*Power, Clock controller*	*Clock Frequency [Hz]*	*Active Rat [%]*
Clock				
Timer		Always on	32k	100
Power controller				
ECG sensing block	AFE	Always on	-	100
	ADC	Clock gating	24k	2.14
	Heart rate extractor	Clock gating	32k	100
Accelerometer	I/F	Clock gating	32k	64.7
	Filter	Clock gating	32	100
Buffer SRAM		Clock gating	write 32k read 24M	write 0.1 read 0.00014
NV-CPU NVRAM		Power gating (Normally Off)	24M	0.10

their active rate, the following two circuit configurations were newly developed and implemented into the SoC.

The one of additional circuit configurations include the Data buffer SRAM to store acceleration data. In the conventional implementation [11], the acceleration data were stored by the NV-CPU within the sampling cycle. On the contrary, a dedicated SRAM that can store the acceleration signal independently of the NV-CPU operations is introduced into the SoC. So, NV-CPU can maintain the sleep state independently from the data sampling and minimize the active rate of NV-CPU. This scheme contributes to lower the SoC power consumption.

The second additional circuit executes the high pass filtering and synthesis of tri-acceleration. In the conventional implementation [11], these were processed by the software. By adding the filtering and synthesizing hardware, active rate of NV-CPU can be reduced. An IIR filter is designed as a high-pass filter, as explained in Sect. 2. It is a second-order Butterworth high-pass filter with a cutoff frequency of 0.7 Hz. Only one digital filtering circuit can processing high pass filtering of tri-axial acceleration with time multiplexing manner, which can minimize the size of the filtering hardware.

To realize adaptive sampling, the high-pass filter block can change its coefficient dynamically according to the chosen sampling rate. Even though the sampling rate changes, the two delay values (Z^{-1}) inside the IIR filter (see Fig. 2) retain their values held before the sampling rate changes. Immediately after changing, large errors arise in the filtered signals because they are influenced strongly by those delay values. Figure 4 shows the IIR filter response for input of the gravitational acceleration component. For example, when changing from BSR to 50% BSR, drastic overshooting occurs immediately after the change. It takes time to stabilize for about 2.2 [sec.] thereafter. It decreases the estimation accuracy. To minimize this influence, the digital filter was designed to adjust the delay values when the sampling rate changes. Therefore the filtered signals are not influenced even if the sampling rate is changed, as shown in Fig. 4.

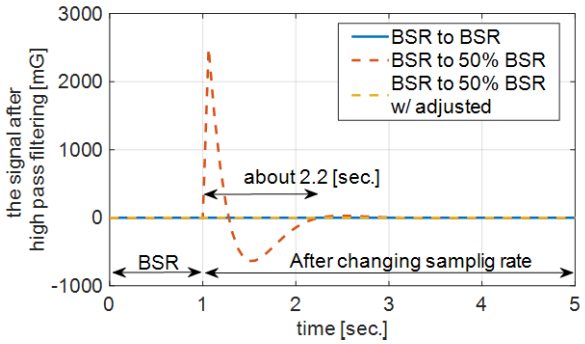


Fig. 4 Influence of sampling rate change.

Table 2 Physical activity list and time of experimental test

	Activity	PA Group	time [min]
Sequence 1	Sitting (activity as rest)	Sedentary	10
	Operating PC	Sedentary	3
	Cleaning desks	Household	1.5
	Moving Load	Household	1.5
	Stair Ascent	HIG	1.2
Sequence 2	Walking	MIG	3
	Jogging	HIG	3

4. Assessment of the Proposed Algorithm

To assess the proposed algorithm, in this study, the tri-axial accelerations and R–R intervals were measured by eight volunteer test subjects during various activities. The measurements were conducted according to guidelines presented in the Declaration of Helsinki. Details of this experimental purposes and procedures were explained to all subjects before measurements were taken. Then consent was obtained from each.

Test subjects performed six distinct activities, including resting in a seated position, during which their triaxial acceleration and R–R interval values were recorded using a device that includes an accelerometer and R–R interval sensor (Health Patch MD; VitalConnect Inc., San Jose, CA). Clinical validation of this device was described earlier [17]. The device was attached to the upper left-side chest ribs on the left of each subject. After the activities, the recorded acceleration and R–R interval are analyzed using software (MATLAB 2015b; The MathWorks, Inc.).

Experiments were conducted separately for Sequences 1 and 2. Table 2 presents activities performed in each sequence and time. Furthermore, an interval of about 1.5 min exists between activities. The interval includes walking to change the location. Each activity was classified into a PA group, as shown in Table 2.

According to the proposed algorithm, the measured signals are classified. The sampling rate was changed for each epoch. Table 3 presents threshold values chosen to classify the PA group. Thresholds of ACC_{fil} are the same as those used in an earlier study [14]. The threshold of %HRR is chosen according to an earlier classification algorithm [10]. The sampling rate during locomotive activities is defined as BSR which is 31.25 [Hz]. Table 4 presents the adjustment coefficient value to reduce the influence of sampling rate change with BSR of 31.25 [Hz]. For example, if sampling rate changes from BSR to 50% BSR, the delay values in IIR filter is multiplied by 0.248 (according to Table 4). The effect of coefficient is described in Sect. 3. Furthermore, METs estimation is done using estimation equations [16] which are shown in Fig. 1. Processing was also conducted when the sampling rate was fixed as BSR (Fixed BSR).

Table 3 Threshold for PA classification

th1 [mG]	th2 [mG]	th3 [%]
29.9	152.6	46

Table 4 Adjustment Coefficient Value for experimental test

		Next Sampling Rate			
		BSR	50%BSR	25%BSR	12.5%BSR
Sampling Rate	BSR	1	0.248	0.060	0.016
	50%BSR	4.034	1	0.241	0.063
	25%BSR	16.773	4.157	1	0.261
	12.5%BSR	64.155	15.902	3.825	1

Figure 5 illustrates the waveform processed with the proposed algorithm and the earlier reported algorithm with fixed sampling rate (Fixed BSR). There is an adequately small difference in the ACC_{fil} waveform. Table 5 presents the root mean square error from the case of processing with Fixed BSR. It can be judged that the root mean square errors for ACC_{fil} with all eight subjects were within 12 [mG]. The average is 4.86 [mG] of whole sequence 1. They are very small errors. Moreover, the estimated METs were evaluated simply using conventional estimation equations [16]. The root mean square error with respect to the result of Fixed BSR is less than 0.22 [METs], and the average is 0.14 [METs]. The mean absolute error is less than 0.06 [METs] in both of sequences. It is seen that no difficulty exists for practical usage.

The classification accuracy is calculated using only those results corresponding to each activity. Table 6 presents the classification accuracy of each activity. The proposed method, which combined the heart rate and acceleration, produced higher estimation accuracy than that of Fixed BSR method. This study assesses the classification accuracy in the Sequence 1. Because the Fixed BSR method can classify only the locomotive group, it is classified as middle intensity group (MIG) herein. Therefore, the classification results obtained using the Fixed BSR method in sequence 2 need not be considered. However, the classification accuracy remains sufficiently high, although the sampling rate changes. In the sequence 1, the classification accuracy is improved with the adaptive sampling algorithm, and it is higher than 90%. According to this result, sedentary and household activities can be classified with a lower sampling rate.

We focused on the classification results which are surrounded by a circle as shown in Fig. 5. After jogging, subjects waited for 30 seconds while standing and walked to

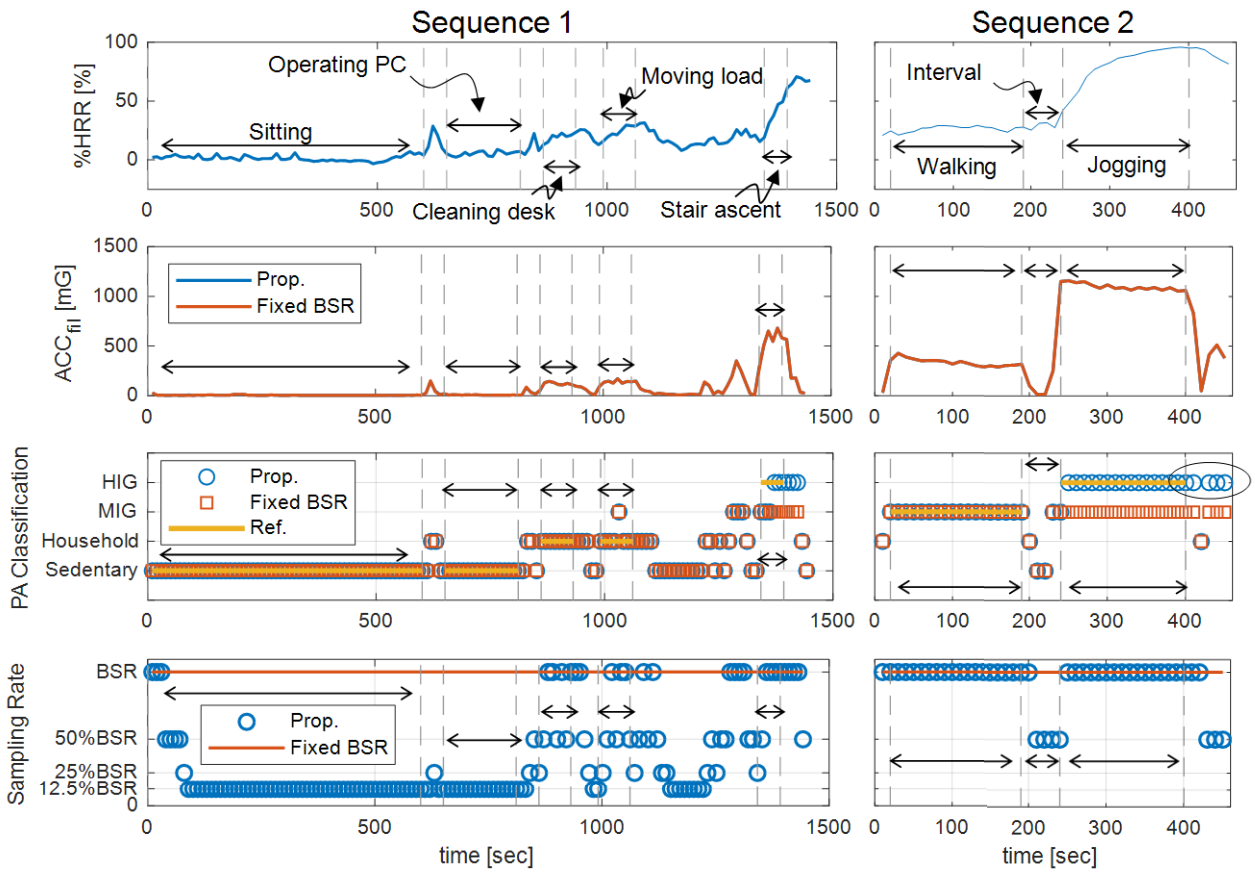


Fig. 5 Measured and processed results using proposed algorithm during experimental tests.

Table 5 Relative Root Mean Square Error of ACCfil and estimation METs and Mean Absolute Error of estimation METs

	Root Mean Square Error of ACC_{fil} [mG]		Root Mean Square Error of estimated METs [METs]		Mean Absolute Error of estimated METs [METs]	
	Seq.1	Seq.2	Seq.1	Seq.2	Seq.1	Seq.2
Sub.01	6.32	2.46	0.07	0.02	0.04	0.00
Sub.02	3.08	3.52	0.22	0.03	0.06	0.01
Sub.03	2.78	0.81	0.05	0.01	0.03	0.00
Sub.04	11.19	7.84	0.19	0.07	0.05	0.02
Sub.05	5.95	1.05	0.17	0.02	0.06	0.00
Sub.06	3.66	9.67	0.07	0.09	0.04	0.02
Sub.07	4.17	4.28	0.18	0.04	0.06	0.01
Sub.08	1.69	9.75	0.15	0.08	0.03	0.02
Average	4.86	4.92	0.14	0.04	0.05	0.01
Standard deviations	3.00	3.68	0.06	0.03	0.01	0.01

Table 6 Results of classification accuracy

	Classification Accuracy [%]			
	Seq. 1		Seq. 2	
	Prop.	Fixed BSR.	Prop.	Fixed BSR.
Sub.01	92.0	89.0	91.4	48.6
Sub.02	88.8	85.7	94.3	48.6
Sub.03	96.0	92.9	97.1	51.4
Sub.04	85.0	81.0	80.5	41.5
Sub.05	94.9	89.8	97.1	48.6
Sub.06	90.8	90.8	82.9	51.4
Sub.07	89.0	89.0	85.7	48.6
Sub.08	90.2	85.7	91.4	48.6
Average	90.8	88.0	90.1	48.4
Standard deviations	3.5	3.7	6.4	3.1

another place. Regarding the PA classification in this interval, those results should be classified into sedentary and MIG, but they were classified into sedentary and HIG. The heart rate was high in these cases, immediately after the end of jogging. Therefore, despite walking, they are misclassified as HIG. Immediately after action corresponding to such HIG, the %HRR is often high (higher than 46 [%]). One must consider such misclassifications when developing a real-time algorithm.

The mean value of classification accuracy is greater than 90% during both sequences with our proposed algorithm. Furthermore, it is almost identical as a result of the fixed sampling rate. Furthermore, regarding ACC_{fil} and

METs, no significant differences of the root mean square error and the mean absolute error are found between the previous and proposed systems. For these reasons, this paper can propose an algorithm that combines the PA classification algorithm and an adaptive sampling algorithm to achieve lower power consumption with reduction of the active rate of the accelerometer.

5. Hardware Implementation Result

To demonstrate the performance of the proposed system, a test chip was fabricated in a 130-nm CMOS process with ferroelectric capacitor. Figure 6 and Table 7 present a chip micrograph and its specifications. Figure 7 shows the application board with the SoC, an accelerometer (KX022; Kionix Inc.), a near field communication IC, and a CR1220 battery. Furthermore, Table 8 shows the adjustment coefficient for delay values in implemented IIR filter. Those are the values to reduce the influence of the sampling rate change in this application board, which uses BSR of 32 Hz. Therefore, the adjustment coefficient is recalculated for this implementation.

In addition, effects of low power consumption achieved with dedicated hardware and the proposed algorithm are assessed. Figure 8 depicts the current consumption of the CPU block with and without hardware assist of the signal processing, as described in Sect. 3. Earlier reported method [16], which adopted a fixed sampling rate, required about 19.6 [μA] for processing by software with BSR (32 Hz). The current consumption in case of software processing with fixed 50% BSR is about 10.7 [μA]. The current consumption using the dedicated hardware for BSR fixed and 50% BSR fixed are 2.9 [μA] and 2.8 [μA], respectively. Compared with the software processing, the reduction was about 85% for the BSR fixed. Moreover, results show that even if sampling rate changes to 50%, the current consumption in hardware solution is almost identical to that of BSR because the active CPU rate can be kept low using the two kind of dedicated circuit. Furthermore, the active rate is independent of the output data rate of the accelerometer when using a SoC. It has a sufficient effect of reducing the current consumption.

The current consumption by using power gating with

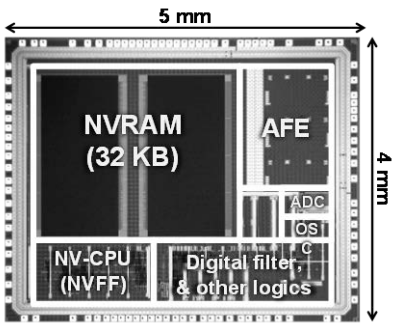


Fig. 6 Test chip micrograph.

Table 7 Test chip specifications

Technology		0.13 µm CMOS
Supply voltage		1.5 V (AFE, ADC, Logic, Mem.)
		3.3 V (32.768-kHz OSC, I/O)
Chip area		4 × 5 mm^2
Frequency		24 MHz (for processor)
		32 kHz (for other blocks)
Processor		32-bit Cortex M0 (with NVFF)
On chip memory		32-KByte 6T-4C NVRAM
AFE	Gain	54 dB
	Bandwidth	700 Hz
	CMRR	73 dB
ADC	Resolution	8 bit
	Current	0.23 µA@128 S/s, 1.0 µA@1 kS/s

Table 8 Adjustment coefficient value for implemented filter

		Next Sampling Rate			
		BSR	50%BSR	25%BSR	12.5%BSR
Sampling Rate	BSR	1	0.248	0.060	0.016
	50%BSR	4.037	1	0.241	0.063
	25%BSR	16.784	4.157	1	0.261
	12.5%BSR	64.300	15.903	3.825	1

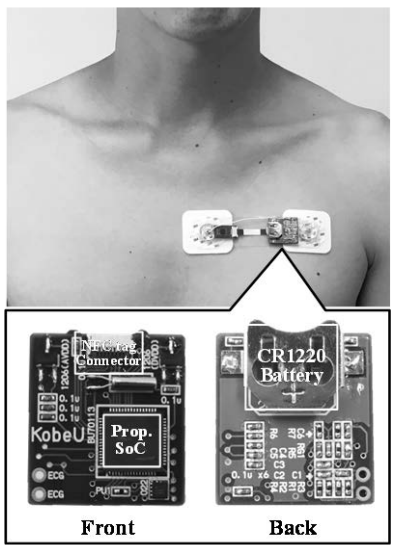


Fig. 7 Application board of the proposed sensor.

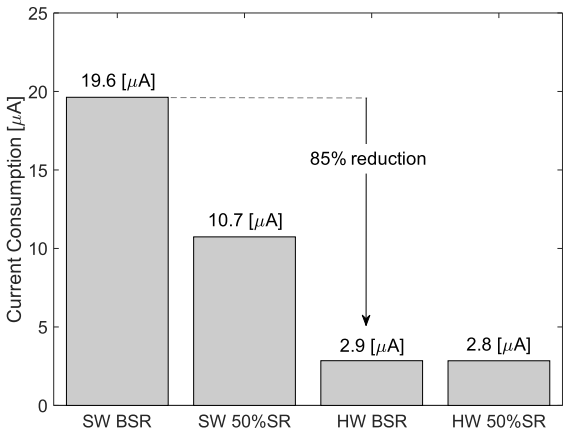


Fig. 8 Current consumption of proposed CPU.

Table 9 Results for all subjects on experimental tests

	Seq.01		Seq.02	
	Prop. [μA]	the ratio of SW w/ fixed BSR[%]	Prop. [μA]	the ratio of SW w/ fixed BSR[%]
Sub.01	13.21	31.0	25.15	59.0
Sub.02	13.70	32.1	24.60	57.7
Sub.03	14.11	33.1	24.60	57.7
Sub.04	13.46	31.6	24.02	56.3
Sub.05	12.66	29.7	24.47	57.4
Sub.06	13.73	32.2	23.76	55.7
Sub.07	13.23	31.0	24.20	56.8
Sub.08	14.20	33.3	24.65	57.8
Average	13.54	31.8	24.43	57.3

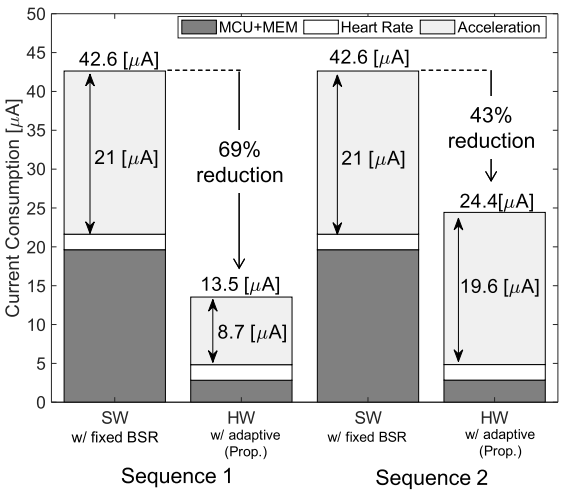


Fig. 9 Total current consumption during experimental tests.

NV-CPU and NVRAM has a potential to be higher than that without power gating, depending on its wake-up duration and active rate. According to our earlier study [14], it is shown that the current consumption with power gating can be lower than that without power gating when its wake-up duration is 200 [msec.] or more, and active rate is 1% or less. In the proposed algorithm and SoC, the wake-up duration is 10 [sec.] and the active rate is 0.1% (see Table 1), so that the significant power reduction is attained by using power gating with NV-CPU and NVRAM.

Next, this study used the test sequences shown in Table 2 with eight subjects to assess the system-level current consumption including the signal processing, heart rate sensor, and accelerometer. The signal processing test includes assessment of the CPU and dedicated hardware. Furthermore, the reduction of the current consumption was assessed by the adaptive sampling. Based on experimentally obtained results, the average current consumption in each sequence was estimated by simulation. Table 9 presents results for each subject. These results of Sequence 1 for all subjects show that about 70% reduction was achieved overall in comparison with the result of software processing with fixed BSR.

In Fig. 9, the average current consumption results of all

Table 10 Spent time of PA for simulation of daily usage

Activity	Explanation	Ratio for wake time [%]	Hours of Activity*1 [h]
Moderate-Vigorous	>3.0METs	4	0.6
Light activity	<3.0METs	39	5.85
Sedentary	Sitting etc…	57	8.55

*1 this paper defined that wake–time is 15 hours, refer to HEALY report.

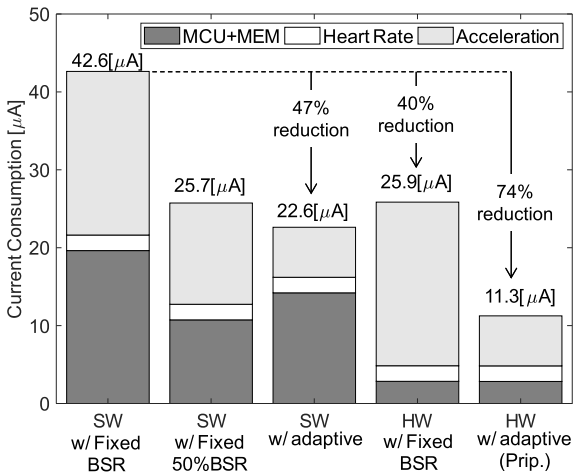


Fig. 10 Simulation result in daily usage of proposed system

subjects demonstrate that the proposed system can decrease current consumption by 69% and 43%, respectively, in Sequences 1 and 2. Here, MCU+MEM denotes the current consumption of signal processing hardware, memory, and MCU of the proposed SoC. The Heart Rate denotes the current consumption of ECG sensing block (see Fig. 2). Acceleration denotes the current consumption of the KX022 accelerometer. About 85% reduction by the CPU (according to Fig. 8) and about 59% (= (21 − 8.7)/21) reduction by the accelerometer were achieved. Sequence 1 includes time at rest, sitting, and operating a PC which greatly reduces current consumption by adopting the adaptive sampling. The estimated value of METs was confirmed as almost identical to the value estimated by fixed BSR (according to Table 5), although achieving reduction of about 70% overall.

Sequence 2 includes walking and jogging which is an operation in BSR. Results show that the hardware current consumption by the chip can be reduced by about 85%, similarly to Sequence 1. However, the current consumption of accelerometer was approximately equal to the consumption with fixed BSR: about 19.6 [μA] Therefore, 43% reduction was attained by the dedicated SoC solution.

Finally, we simulate how much power can be consumed in daily situation using the proposed algorithm and SoC. Healy *et al.* [18] reported results of measured times of exercise intensity (Sedentary, Light activity, Moderate-Vigorous) for 168 subjects. Table 10 shows the time ratio of the exercise intensity. Then, base sampling rate (BSR) = 32 Hz is set as Moderate-Vigorous. During light activity,

the processing sampling rate is set to the midpoint between 12.5% BSR and 50% BSR, that is 25% BSR (8 Hz). During sedentary, it is 12.5% BSR (4 Hz).

As shown in Fig. 10, the software implementation of the adaptive sampling consumes 22.6 [μA], which is 47% (= (22.6 − 42.6)/42.6) lower than that under the software processing with fixed BSR. This result reflects that certain power reduction can be achieved using the proposed algorithm even if hardware assist is not used. As presented in Table 5, its estimation accuracy also seems to exhibit no marked decrease. Using the dedicated hardware proposed herein without the adaptive sampling algorithm, 40% (= (25.9 − 42.6)/42.6) reduction in consumption from software processing with fixed BSR was achieved. This current consumption is achieved by implementing the dedicated circuit configurations into the proposed SoC. This improvement is regarded as a meaningful result. The dedicated SoC with the adaptive sampling algorithm realizes low power consumption of about 11.3 [μA] and reduction of 74% in comparison with software processing with fixed BSR.

Furthermore, results show that when using a CR2016, the battery capacity is 90 [mAh]. The system which is software processing with fixed BSR is able to operate continually for 88 days. The proposed system can operate continually for 333 days: about 1 year. This monitoring system for PA classification and METs estimation can operate continually for a long-term.

6. Conclusion

This study is conducted to develop algorithms and SoC with a sensor fusion approach for PA classification and METs estimation with low power consumption. As described in this paper, we propose a monitoring system that can achieve both increased number of PA classification groups and significant reduction of current consumption. In daily usage, the proposed system can achieve average current consumption of 11.3 [μA], representing a 74% reduction of the current consumption in comparison with the previous system with a fixed sampling rate and software processing.

Acknowledgments

This research was partially supported by the Ministry of Economy, Trade and Industry (METI), the New Energy an Industrial Technology Development Organization (NEDO), and a JSPS KAKENHI Grant (JP16H05868).

References

[1] K.L. Coleman, D.G. Smith, D.A. Bone, A.W. Joseph, and M.A. del Agulia, "Step activity monitor: Long term, continuous recording of ambulatory function," Journal of Rehabilitation Research and Development, vol.36, no.1, pp.8–18, Jan. 1999.

[2] D.R. Bassett, A.V. Rowlands, and S.G. Trost, "Calibration and validation of wearable monitors," Medicine and Science in Sports and Exercise, vol.44, no.1 pp.S32–S38, Jan. 2012.

[3] R.K. Albright, B.J. Goska, T.M. Hageny, M.Y. Chiz, G. Cauwenberghsx, and P.Y. Chiang, "OLAM: A Wearable, Non-Contact Sensor for Continuous Heart-Rate and Activity Monitoring," Proc. of IEEE EMBC, pp.5625–5628, Sept. 2011.

[4] J.D. Amor, J.G. Hattersley, T.M. Barber, and C.J. James, "Characterization of Wrist-wearable Activity Measurement using Whole Body Calorimetry in Semi-Free Living Conditions," Proc. of IEEE EMBC, pp.3735–3738, Aug. 2015.

[5] A.M. Khan, Y.-K. Lee, S.Y. Lee, and T.-S. Kim, "A triaxial accelerometer-based physical-activity recognition via augmented-signal features and a hierarchical recognizer," IEEE Trans. Inf. Technol. in Biomed., vol.14, no.5, pp.1166–1172, Sept. 2010.

[6] D.R. Bassett, B.E. Ainsworth, A.M. Swartz, S.J. Strath, W.L. O'Brien, and G.A. King, "Validity of four motion sensors in measuring moderate intensity physical activity," Med. Sci. Sports Exerc., vol.32, pp.S471–S480, Sept. 2000.

[7] C.E. Matthews, "Calibration of accelerometer output for adults," Med. Sci. Sports. Exerc., vol.37, pp.S512–S522, Nov. 2005.

[8] G.J. Welk, S.N. Blair, K. Wood, S. Jones, and R.W. Thompson, "A comparative evaluation of three accelerometry-based physical activity monitors," Med. Sci. Sports Exerc., vol.32, pp.S489–S497, Sept. 2000.

[9] R.D. Gonzalo, P. Celks, P. Renevey, S. Dasen, J. Solà, M. Bertschi, and M. Lemay, "Physical activity profiling: activity-specific step counting and energy expenditure models using 3D wrist acceleration," Proc. of IEEE EMBC, pp.8091–8094, Aug. 2015.

[10] M. Nakanishi, S. Izumi, S. Nagayoshi, H. Sato, H. Kawaguchi, M. Yoshimoto, T. Ando, S. Nakae, C. Usui, A. Tomoko, and S. Tanaka, "Physical activity group classification algorithm using triaxial acceleration and heart rate," Proc. of IEEE EMBC, pp.510–513, Aug. 2015.

[11] S. Izumi, K. Yamashita, M. Nakano, S. Yoshimoto, T. Nakagawa, Y. Nakai, H. Kawaguchi, H. Kimura, K, Marumoto, T. Fuchigami, Y. Fujimori, H. Nakajima, T. Shiga, and M. Yoshimoto, "Normally off ECG SoC With non-volatile MCU and noise tolerant heartbeat detector," IEEE Trans. Biomed. Circuits Syst., vol.9, no.5, pp.641–51. Oct. 2015

[12] M. Tsukahara, M. Nakanishi, S. Izumi, Y. Nakai, H. Kawaguchi, and M. Yoshimoto, "Low-power metabolic equivalents estimation algorithm using adaptive acceleration sampling," Proc. of IEEE EMBC, pp.1878–1881, Aug. 2016.

[13] Seiko Epson Corporation, "Pulse Detector, Electronic Apparatus, and Program," US Patent, US20150088013 A1, March 26, 2013.

[14] M. Tsukahara, S. Izumi, M. Nakanishi, H. Kawaguchi, M. Yoshimoto, H. Kimura, K. Marumoto, T. Fuchikami, and Y. Fujimori, "A 15-μA metabolic equivalents monitoring system using adaptive acceleration sampling and normally off computing," Proc. of IEEE ICECS, pp.61–64, 2016.

[15] Y. Oshima, K. Kawaguchi, S. Tanaka, K. Ohkawara, Y. Hikihara, K. Ishikawa-Takata, and I. Tabata, "Classifying household and locomotive activities using a triaxial accelerometer," Gait Posture, vol.31, no.3, pp.370–374, March 2010.

[16] K. Ohkawara, Y. Oshima, Y. Hikihara, K. Ishikawa-Takata, I. Tabata, and S. Tanaka, "Real-time estimation of daily physical activity intensity by a triaxial accelerometer and a gravity-removal classification algorithm," Br. J. Nutr., vol.105, no.11, pp.1681–1691, June 2011.

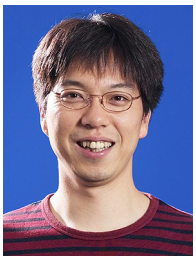
[17] A.M. Chan, N. Selevaraj, N. Ferdosi, and R. Narasimhan, "Wireless patch sensor for remote monitoring of heart rate, respiration, activity, and falls," Proc. of IEEE EMBC, pp.6115–6118, Aug. 2013.

[18] G.N. Healy, D.W. Dunstan, J. Salmon, E. Cerin, J.E. Shaw, P.Z. Zimmet, and N. Owen, "Breaks in sedentary time," Diabetes Care, vol.31, no.4, pp.661–666, April 2008.

Motofumi Nakanishi received B.S. and M.S. degrees from the Department of Robotics of Ritsumeikan University, respectively, in 2007 and 2009. In April 2009, he joined Omron Healthcare Co., Ltd., Kyoto Japan. During 2009–2014, he was engaged in designing electronic circuits for a body composite monitor and pedometer. Since October 2014, he has been working toward a Ph.D. in Engineering at Kobe University. His current research interests include biological signal processing and low-power VLSI design.

Shintaro Izumi received his B.Eng. and M.Eng. degrees in Computer Science and Systems Engineering, respectively, from Kobe University, Hyogo, Japan, in 2007 and 2008. He received his Ph.D. degree in Engineering from Kobe University in 2011. He was a JSPS Research Fellow at Kobe University during 2009–2011. Since 2011, he has been an Assistant Professor at the Organization of Advanced Science and Technology at Kobe University. His current research interests include biomedical signal processing, communication protocols, low-power VLSI design, and sensor networks. He has served as a Chair of the IEEE Kansai Section Young Professionals Affinity Group, as a Student Activity Committee Member for IEEE Kansai Section, and as a Program Committee Member for IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips). He was a recipient of the 2010 IEEE SSCS Japan Chapter Young Researchers Award.

Mio Tsukahara received B.Eng. degrees in Computer and Systems Engineering from Kobe University, Hyogo, Japan, in 2016. Currently, she is a master course student at Kobe University. Her current research is related to wearable health-care systems.



Hiroshi Kawaguchi received B.Eng. and M.Eng. degrees in electronic engineering from Chiba University, Chiba, Japan, respectively, in 1991 and 1993and earned a Ph.D. degree in Engineering from The University of Tokyo, Tokyo, Japan, in 2006. He joined Konami Corporation, Kobe, Japan, in 1993, where he developed arcade entertainment systems. He moved to The Institute of Industrial Science, The University of Tokyo, as a Technical Associate in 1996, and was appointed as a Research Associate in 2003. In 2005, he moved to Kobe University, Kobe, Japan. Since 2007, he has been an Associate Professor with The Department of Information Science at that university. He is also a Collaborative Researcher with The Institute of Industrial Science, The University of Tokyo. His current research interests include low-voltage SRAM, RF circuits, and ubiquitous sensor networks. Dr. Kawaguchi was a recipient of the IEEE ISSCC 2004 Takuo Sugano Outstanding Paper Award and the IEEE Kansai Section 2006 Gold Award. He has served as a Program Committee Member for IEEE Custom Integrated Circuits Conference (CICC) and IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips), and as a Guest Associate Editor of IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences and IPSJ Transactions on System LSI Design Methodology (TSLDM).

Hiromitsu Kimura received a B.E. degree in Electrical Engineering from Tohoku University, Sendai, Japan, in 1998 and a Master of Information Science and Doctor of Information Science degrees in Computer and Mathematical Sciences, respectively, from Tohoku University in 2000 and 2003. He is currently a Senior Engineer of Rohm Co. Ltd., Japan. His main interests and activities are in the areas of Ferroelectric random access memory (FeRAM) and non-volatile logic LSI. Dr. Kimura received the Judge's Special Award at the Ninth LSI Design of the Year from the Semiconductor Industry News of Japan in 2002 and the Grand Award at IEEE International Meeting for Future of Electron Devices, Kansai in 2006. Dr. Kimura is an IEEE member.

Kyoji Marumoto has been working at Rohm Co. Ltd., Kyoto, Japan.

Takaaki Fuchikami has been working on LSI Product Development Headquarters Core Technology Development Division, Rohm Co. Ltd., Kyoto, Japan.

Yoshikazu Fujimori received B.E. and M.E. degrees in Electronics Engineering from Kyoto University, Kyoto, Japan. In 1996, he joined Rohm Co. Ltd., Kyoto, Japan, where he has been working on device and process development of Ferroelectric Random Access Memory (FeRAM). He received a Doctor of Engineering degree from Kyoto University in 2005. His research interests include low-power and functional applications of non-volatile ferroelectric devices and piezoelectric devices.

Masahiko Yoshimoto joined the LSI Laboratory, Mitsubishi Electric Corp., Itami, Japan, in 1977. During 1978–1983 he was engaged in the design of NMOS and CMOS static RAM. From 1984, he was involved in the research and development of multimedia ULSI systems. He earned a Ph.D. degree in Electrical Engineering from Nagoya University, Nagoya, Japan in 1998. From 2000, he was a Professor of the Dept. of Electrical & Electronic System Engineering of Kanazawa University, Japan. From 2004, he was a professor of the Dept. of Computer and Systems Engineering in Kobe University, Japan. His current activities specifically emphasize research and development of ultra low power multimedia and ubiquitous media VLSI systems and dependable SRAM circuit. He holds 70 registered patents. He served on the Program Committee of the IEEE International Solid State Circuit Conference during 1991–1993. Furthermore, he served as Guest Editor for Special Issues on Low-Power System LSI, IP and Related Technologies of IEICE Transactions in 2004. He was a chair of the IEEE Solid State Circuits Society (SSCS) Kansai Chapter during 2009–2010. He is also a chair of the IEICE Electronics Society Technical Committee on Integrated Circuits and Devices from 2011–2012. He received R&D100 awards from the R&D magazine for the development of the DISP and the development of the real-time MPEG2 video encoder chipset, respectively, in 1990 and 1996. He received the 21st TELECOM System Technology Award in 2006. He is a Fellow of IEICE.