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LETTER

An 11.8 nA ultra-low power active diode using a hysteresis common gate comparator for low-power energy harvesting systems

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Abstract This paper proposes an ultra-low power active diode (ADIO) using a hysteresis common gate comparator for low-voltage and low-power energy harvesting systems. The proposed ADIO consists of a MOS switch and hysteresis common gate comparator, which eliminates unwanted ripple and noise voltages. The hysteresis comparator controls the MOS switch to turn ON or OFF, depending on the input and output voltages. The hysteresis voltages of the comparator can be controlled by the current flowing in the comparator. The measurement results demonstrated that the hysteresis comparator had −26 and 25 mV hysteresis voltages and the ADIO using the hysteresis comparator eliminated unwanted ripple voltage. The maximum current consumption of our ADIO was 11.8 nA.

Keywords: IoT, energy harvesting, active diode, hysteresis comparator, low-power, low voltage

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

In this paper, we propose an ultra-low power active diode (ADIO) circuit that is used for the reverse current protection in energy harvesting systems.

Energy harvesting has gained increasing attention to realize battery-less and maintenance-free IoT devices [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18]. To realize such devices, highly efficient power management systems are strongly required because the output voltages of the small harvesters are basically weak and are easily lost depending on their power generation environment. When the energy from the harvester is cut off during the charging phase, the charged and stored energy on the energy buffer is dissipated as a reverse current.

An ADIO can prevent the reverse current problem. However, the conventional ADIO consisting of a MOS switch and common-gate (CG) comparator suffers from ripple and noise voltages. The hysteresis comparator can cope with the ripple and noise voltages [19]. There are several hysteresis comparators that are based on the differential pair circuit. However, there are few reports on the CG comparator with hysteresis.

In light of the background, we propose an ultra-low power hysteresis CG comparator and develop an ADIO using the hysteresis CG comparator. In our proposed power management system, the hysteresis CG comparator monitors the output voltage of the energy harvester and stored voltage of the energy buffer and prevents the reverse current when the energy from the harvester is lost. This paper is organized as follows: Section II briefly summarizes our proposed power management system. Section III explains our proposed hysteresis CG comparator. Section IV discusses the simulation results. Section V concludes the paper.

2. Proposed power management system

Figure 1 shows a power management system. The system employs an ADIO as a switch between the harvester and energy buffer. Figure 2 shows the ADIO. The ADIO consists of a CG comparator and pMOS transistor. The ADIO transfers the charge to the energy buffer with a quite low voltage difference [20, 21, 22, 23, 24]. When the output voltage of the energy harvester is lost, the ADIO will detect the input voltage reduction and cut off the current path to prevent the reverse current. Figure 3 shows waveforms of input and output voltages with and without hysteresis. The ripple and noise voltages will oscillate the comparator's output when we use a comparator without hysteresis (Fig. 3(b)). To

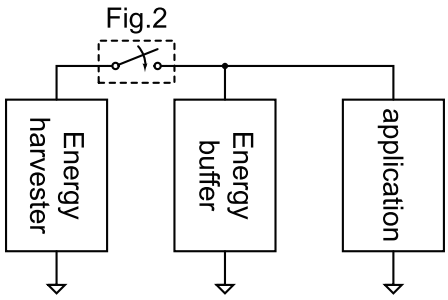

Fig. 1 Proposed power management system.

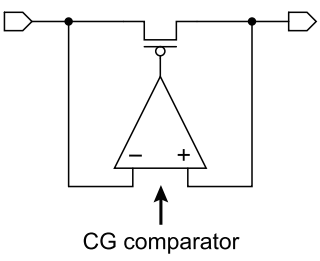

Fig. 2 ADIO using CG comparator.

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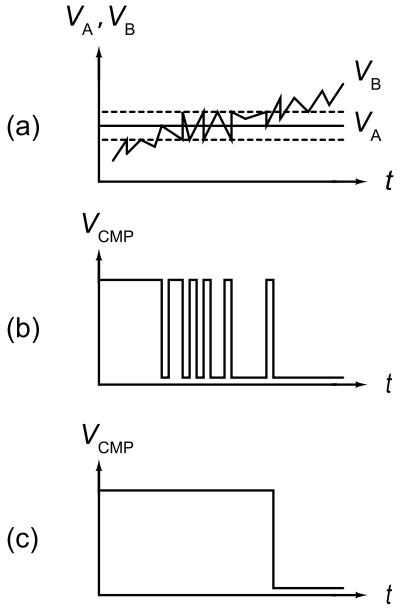

Fig. 3 Waveforms of (a) input voltages, (b) output voltage of the comparator without hysteresis, and (c) output voltage of the comparator with hysteresis.

eliminate the oscillation (Fig. 3(c)), we use hysteresis comparators. There are several hysteresis comparators that are based on the differential pair circuit. However, there are few reports on the CG comparator with hysteresis. Therefore, we develop a hysteresis CG comparator for the ADIO.

3. Hysteresis CG comparator

3.1 Conventional CG comparator

Figure 4(a) shows a simplified core circuit of the conventional CG comparator. The circuit consists of two current sources and two pMOS transistors. Input voltages V_A and V_B are connected to the source terminals of the pMOS transistors. Figure 4(b) illustrates waveforms of the output current I_X and output voltage V_X when V_A is set to a certain voltage and V_B is changed from Low to High. When V_B is lower than V_A, V_X is high because current flowing in MP_2 is larger than I_B. On the other hand, when V_B is higher than V_A, V_X is low because current flowing in MP_2 is lower than I_B. Therefore, current flowing in MP_2 will determine the voltage of V_X. This can be analyzed as follows.

When the source-drain voltage V_{SD} of a PMOS transistor is 0.1 V or more, the subthreshold drain current I can be expressed as

$$I = KI_0 \exp\left(\frac{V_{SG} - |V_{THP}|}{\eta V_T}\right), \tag{1}$$

where $K(= W/L)$ is the aspect ratio of the transistor, $I_0(= \mu C_{ox} V_T^2(\eta - 1))$ is the process dependent parameter, μ is the carrier mobility, C_{ox} is the gate-oxide capacitance, $V_T(= k_B T/q)$ is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, η is the subthreshold slope factor, V_{SG} is the source-source voltage, and $|V_{TH}|$ is the threshold voltage of a pMOS transistor. From Eq. (1), the source-gate voltage V_{SG1} of

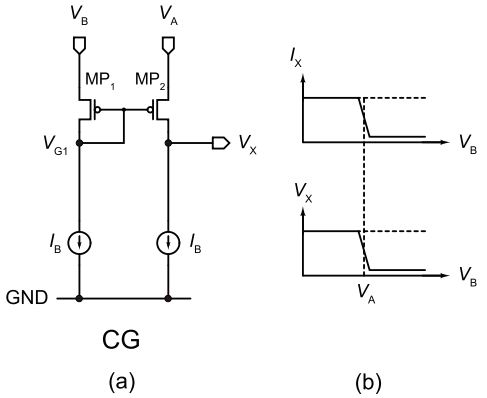

Fig. 4 (a) Schematic of the simplified CG comparator and (b) illustrations of the output current and voltage (I_X and V_X).

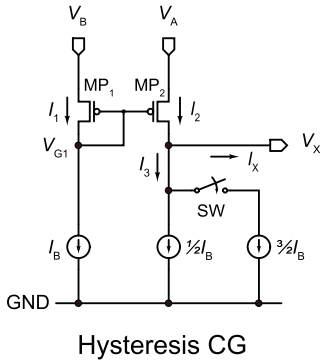

Fig. 5 Simplified schematic of our hysteresis CG comparator.

MP1 is expressed as

$$V_{SG1} = |V_{THP}| + \eta V_T \ln\left(\frac{I_B}{K_1 I_0}\right), \tag{2}$$

where I_B is the bias current and K_1 is the aspect ratio of MP1. From Eq. (2), V_{G1} can be expressed as

$$\begin{aligned} V_{G1} &= V_B - V_{SG1} \\ &= V_B - |V_{THP}| - \eta V_T \ln\left(\frac{I_B}{K_1 I_0}\right). \end{aligned} \tag{3}$$

The source-gate voltage V_{SG2} of MP2 can be expressed as

$$V_{SG2} = V_A - V_{G1}. \tag{4}$$

Therefore, from Eqs. (1) and (3), the current I_2 can be expressed as

$$I_2 = \frac{K_2}{K_1} I_B \exp\left(\frac{V_A - V_B}{\eta V_T}\right), \tag{5}$$

where K_2 is the aspect ratio of M2. When $K_1 = K_2$, Eq. (5) can be expressed as

$$I_2 = I_B \exp\left(\frac{V_A - V_B}{\eta V_T}\right). \tag{6}$$

Therefore, the current I_X flowing into V_X can be expressed as

$$\begin{aligned} I_X &= I_2 - I_B \\ &= I_B \left\{\exp\left(\frac{V_A - V_B}{\eta V_T}\right) - 1\right\}. \end{aligned} \tag{7}$$

From Eq. (7), when $V_B < V_A$, I_X becomes positive and V_X increases. On the other hand, when $V_B > V_A$, I_X becomes negative and V_X decreases. Figure 4(b) illustrates I_X and V_X as a function of V_B. When $V_B = V_A$, the output voltage V_X changes from High to Low.

3.2 Proposed hysteresis CG comparator

As discussed in the previous section, we can control the switching voltage of the CG comparator by changing the bias current I_B connected to V_X. Figure 5 shows a simplified schematic of our proposed hysteresis CG comparator. A switch (SW) is used to control the bias current.

When SW is OFF, I_3 in Fig. 5 becomes $I_B/2$. From Eq. (7), I_X can be expressed as

$$I_X = I_2 - I_3 = I_2 - \frac{1}{2}I_B = I_B\left\{\exp\left(\frac{V_A - V_B}{\eta V_T}\right) - \frac{1}{2}\right\}. \quad (8)$$

Therefore, from Eq. (8), I_X becomes positive, when

$$V_B > V_A + \eta V_T \ln 2. \quad (9)$$

The switching voltage becomes higher than V_A by $\eta V_T \ln 2$. It is 27 mV, when we set η and V_T at room temperature to 1.5 and 26 mV, respectively.

On the other hand, when SW is ON, current I_3 in Fig. 5 becomes $2I_B$. Therefore, from Eq. (7), I_X can be expressed as

$$I_X = I_2 - I_3 = I_2 - 2I_B = I_B\left\{\exp\left(\frac{V_A - V_B}{\eta V_T}\right) - 2\right\}. \quad (10)$$

Therefore, from Eq. (10), I_X becomes positive, when

$$V_B < V_A - \eta V_T \ln 2. \quad (11)$$

The switching voltage becomes lower than V_A by $\eta V_T \ln 2$. It is −27 mV, when we set η and V_T at room temperature to 1.5 and 26 mV, respectively.

Therefore, when the input voltage V_B changes from Low to High, a positive hysteresis voltage can be obtained by turning SW OFF. On the other hand, when the input voltage V_B changes from High to Low, a negative hysteresis voltage can be obtained by turning SW ON. Figure 6 shows a complete schematic of our proposed hysteresis CG comparator.

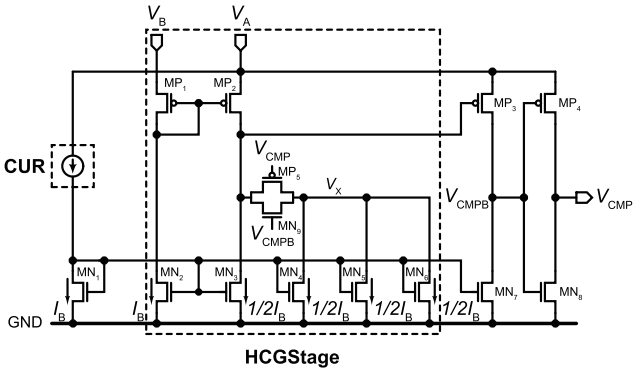

Fig. 6 Schematic of our proposed hysteresis CG comparator.

A common source amplifier (MN_7-MP_3) and inverter (MN_8-MP_4) are added to enhance the total voltage gain. A nano-ampere current source is used to achieve ultra-low power dissipation [25, 26, 27, 28, 29, 30]. The transistor sizes of MN_1:MN_2:MN_{3-6} are set to 4:2:1. A transmission gate (MP_5 and MN_9) is used as the switch to control the bias current. The outputs of the comparator V_{CMP} and common source amplifier V_{CMPB} are used to control the transmission gate.

4. Results

4.1 Simulation results

We evaluated the performance of our hysteresis CG comparator using SPICE with a set of 65-nm standard CMOS process parameters. Table I lists the transistor sizes ($M\times(W/L)$, M: multiplier, W: channel width, and L: channel length) of the comparator. Figure 7 shows the simulated hysteresis CG comparator circuit.

Figures 8 and 9 show the simulated transient waveforms of the comparator. The V_A and I_B were set to 2.4 V and 2 nA, respectively. The V_B increased from 2.3 to 2.5 V (Fig. 8), and then decreased from 2.5 to 2.3 V (Fig. 9), with a ripple voltage. The frequency and amplitude of the ripple voltage were set to 100 Hz and 50 mV, respectively. The output voltage of the comparator without hysteresis oscillated as shown on the bottom in Figs. 8 and 9. We confirmed that our proposed comparator operated correctly.

4.2 Experimental results

A prototype chip was fabricated with a 65-nm, CMOS process with deep n-well option. The circuit was designed with the same parameters as those in the simulation. Figure 10 shows a chip micrograph of our comparator. The area occupied 0.024 mm^2.

Figure 11 shows the measurement V_A, V_B, V_{CMP}, I_{OUTA},

Table I Transistor sizes

Transistor	Size
MP_1, MP_2	4×(4 μm/10 μm)
MP_3	4×(2 μm/10 μm)
MP_4	5×(1 μm/5 μm)
MP_5	5×(1 μm/1 μm)
MP_6	40×(1 μm/1 μm)
MN_1	8×(2 μm/10 μm)
MN_2, MN_7	4×(2 μm/10 μm)
MN_3, MN_4, MN_5, MN_6	2×(2 μm/10 μm)
MN_8	1×(1 μm/25 μm)
MN_9	5×(1 μm/1 μm)

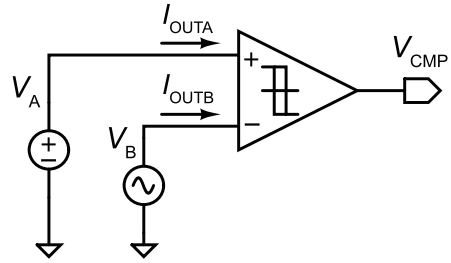

Fig. 7 Block diagram of hysteresis CG comparator.

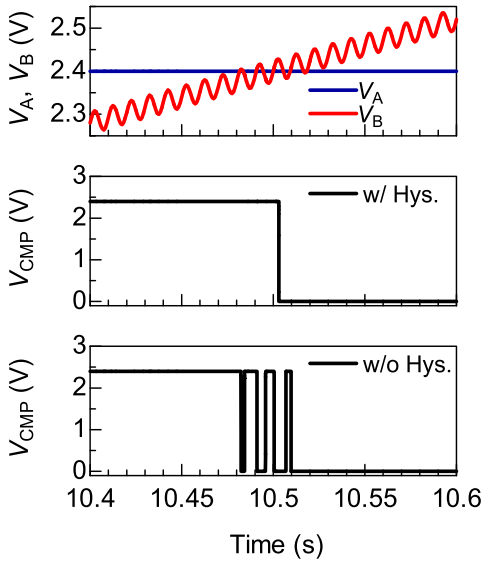

Fig. 8 Simulated transient waveforms.

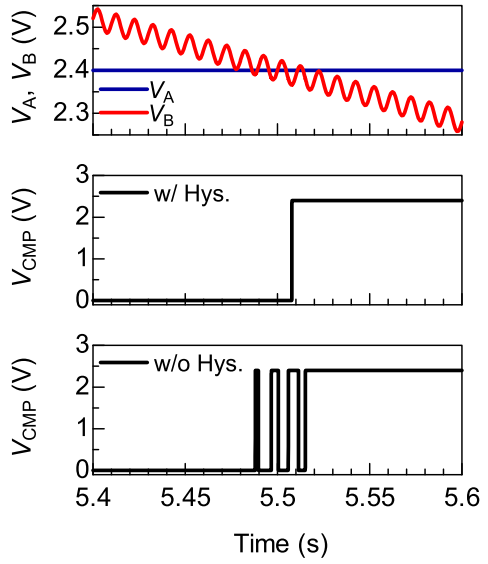

Fig. 9 Simulated transient waveforms.

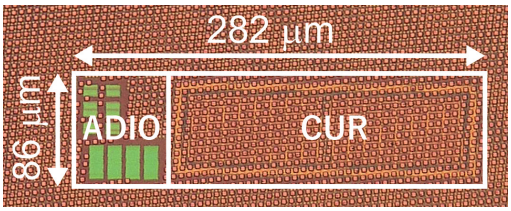

Fig. 10 Chip micrograph.

and I_{OUTB}, as a function of V_B. As shown in Fig. 11, we confirmed that V_{CMP} changed with hysteresis voltages. The positive and negative hysteresis voltages were 25 and −26 mV, respectively, which were almost the same as the calculated results. The maximum current consumption I_{OUTA}, and I_{OUTB} were 9.82 and 1.97 nA, respectively.

Figure 12 shows the measured transient waveforms V_A, V_B and V_{CMP}. The V_A and I_B were set to 2.4 V and 2 nA, respectively. The frequency and peak-to-peak voltage of V_B were set to 1 Hz and 3 V, respectively. The V_{CMP} was high

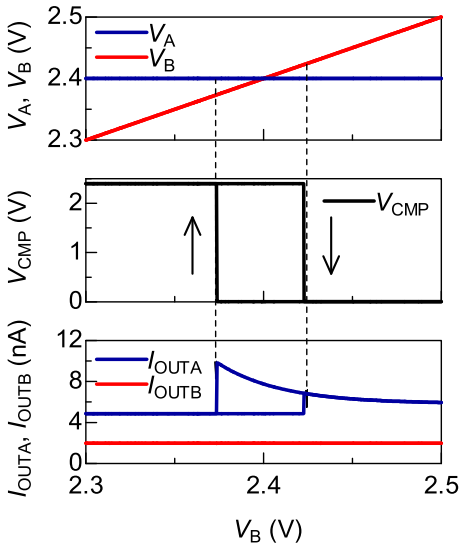

Fig. 11 Measured transfer function.

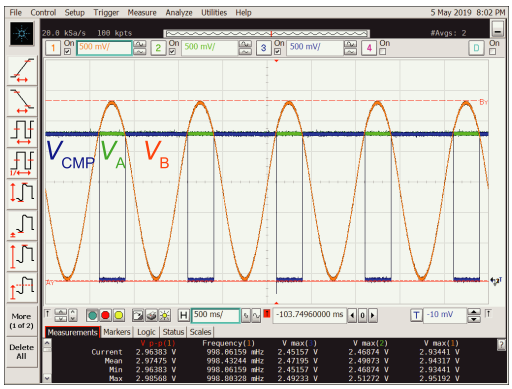

Fig. 12 Measured transient waveforms.

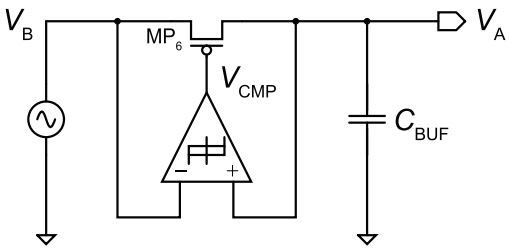

Fig. 13 Block diagram of ADIO.

when V_B was lower than V_A, while the V_{CMP} was low when V_B was higher than V_A. We confirmed that our proposed comparator operated correctly.

Figure 13 shows a test bench circuit of our proposed ADIO using our proposed hysteresis CG comparator. The C_{BUF} and I_B were set to 100 uF and 2 nA, respectively. The frequency and peak-to-peak voltage of V_B were set to 50 Hz and 2.4 V, respectively. Figure 14 shows the measured waveforms of the ADIO. The output voltage of the CG comparator V_{CMP} changed correctly according to the voltage difference between V_A and V_B. The measured V_A increased gradually as expected because the ADIO cut off the reverse current successfully.

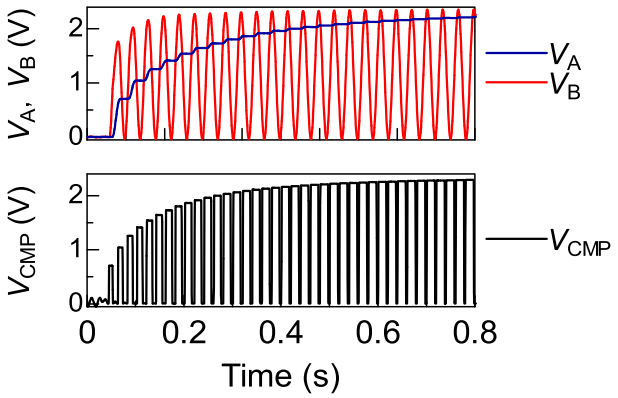

Fig. 14 Measured transient waveforms with ADIO.

5. Conclusion

This paper presented a hysteresis CG comparator and active diode (ADIO) using the CG comparator for low-voltage and low-power energy harvesting systems. The proposed ADIO consists of a MOS switch and CG comparator, which eliminates unwanted ripple and noise voltages. The hysteresis CG comparator controls the MOS switch to turn ON or OFF, depending on the input and output voltages. The hysteresis voltage of the comparator can be controlled by the current flowing in the CG comparator. The measurement results demonstrated that the hysteresis CG comparator had −26 and 25 mV hysteresis voltages and the active diode using the hysteresis CG comparator eliminated unwanted ripple voltage. The maximum current consumption of our ADIO was 11.8 nA.

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