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Evaluation of organic metal-oxide-semiconductor capacitors based on a distributed constant circuit

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The capacitance characteristics of pentacene metal-oxide-semiconductor (MOS) capacitors with a large uncovered pentacene area have been investigated. The capacitance measured was examined by assuming that the uncovered area is represented by a distributed constant circuit. The frequency dependence of the capacitance was reproduced by an equation derived based on the assumption. The sheet resistance for the uncovered area of a MOS capacitor was calculated as a function of the gate voltage from the capacitance measured. The mobility of a MOS capacitor with an uncovered area was estimated by fitting a curve to the gate-voltage dependence of the sheet resistance, and was in the range of 0.48 to 0.64 cm^2 V^{-1} s^{-1}. In addition, the mobilities were compared with those calculated from the current-voltage characteristics of pentacene transistors fabricated on the same substrate.

1. Introduction

Organic semiconductor devices, including thin film transistors (TFTs),[1,2] light-emitting diodes,[3,4] photovoltaics,[5,6] and chemical sensors,[7,8] have attracted attention because of their potential application to flexible, large-area, light-weight, and low-cost electronic devices. In addition to these features, the field-effect mobilities in organic TFTs significantly improving with finding of novel materials [9] have reached over 10 $cm^2 V^{-1} s^{-1}$.[10] With the improvement of organic device performance, the carrier transport in organic devices is required to be investigated in more detail.[11,12]

For organic TFTs, the field-effect mobility and threshold voltage calculated from the current-voltage characteristics are used as standard evaluation for them.[13] The contact resistance between the contact electrode and the organic semiconductor in organic TFTs is often calculated based on a transfer line method.[14-16] In this method, the contact resistance is also calculated from the current-voltage characteristics obtained by DC measurement. On the other hand, impedance spectroscopy based on AC measurement is an evaluation methods for organic TFTs when focusing on the metal-oxide-semiconductor (MOS) or metal-insulator-semiconductor (MIS) structure.[17,18] Actually, the capacitance-voltage characteristics measured at a certain frequency have been used for investigation of the interface states,[19,20] the flat-band voltage,[21-23] the injection barrier,[24] and the stability.[25] The investigation is based on theory for Si-based MOS capacitors.[26] However, an organic MOS capacitor often has an area uncovered with the contact electrode to the organic semiconductor. In order to eliminate the influence, it is necessary to remove the organic layer uncovered with the contact electrode.[18]

Some groups have examined organic TFTs[27,28] and organic MOS capacitors[29-33] considering organic semiconductor areas uncovered with the contact electrode. Hamadani *et al*. and Girolamo *et al*. investigated the characteristics of organic TFTs using equivalent circuits consisting of distributed elements for the uncovered area.[27,28] On the other hand, Jung *et al*. and Hayashi *et al*. reproduced the characteristics of organic MOS capacitors with uncovered organic areas using a distributed constant circuit[29] and a diffusion equation,[30] respectively. In order to reproduce the measured results, it is necessary to consider both the effect of the uncovered area and that of the MOS capacitors covered by the electrode. The lengths of the uncovered areas were up to about 95 μm for Ref. 29) and 235 μm for Ref. 30).

On the other hand, Ucurum and Goebel investigated the capacitance-voltage characteristics of pentacene MOS capacitors having uncovered areas up to 4 mm in length.[31] They analyzed the characteristics separating into three components for metal/insulator/metal, covered MIS, and uncovered MIS structures. Although the method of the analysis is effective, it is seems that the hysteresis in the capacitance-voltage characteristics caused difficulty in quantitative analysis. If a MOS capacitor having an uncovered area sufficiently larger than a covered area is examined, it is possible to eliminate the influence of the covered MOS area and intensively analyze the carrier transport in organic layers uncovered with an electrode. Actually, we have reported the voltage and frequency dependence of capacitance in pentacene MOS capacitors with a large uncovered area without detail analysis.[34]

In this paper, we report the capacitance characteristics of pentacene MOS capacitors with a large uncovered area in detail. The measured capacitance is systematically examined by assuming that the uncovered area is represented by a distributed constant circuit. The sheet resistance derived from the measured capacitance is used for calculation of the carrier mobility in the pentacene layer. The carrier mobilities are compared with those calculated from the current-voltage characteristics of pentacene TFTs fabricated on the same substrates.

2. Analytical method

2.1 Characteristics of MOS capacitors

Figure 1(a) shows illustration of a pentacene MOS capacitor examined in this study. The pentacene layer has an area uncovered with the top Au electrode. For measurement of the capacitance, an AC voltage of frequency f superimposed on a gate voltage V_G was applied to the Cr gate electrode as seen in Fig. 1(a). The length and the width of the uncovered area are denoted by L_{dis} and W_{dis}, respectively. The total capacitance of the MOS capacitor C can be represented as

$$C = C_0 + C_{MOS} + C_{dis}, \quad (1)$$

where C_0, C_{MOS}, and C_{dis} are the capacitances of Au/SiO_2/Cr, Au/pentacene/SiO_2/Cr, and pentacene/SiO_2/Cr structures shown in Fig. 1(b), respectively. When the capacitance per unit area of SiO_2 is denoted as C_{OX}, $C_0 = C_{OX} S_0$ where S_0 is the area of the Au/SiO_2/Cr structure. The capacitance of the Au/pentacene/SiO_2/Cr structure C_{MOS} is given by

$$C_{\mathrm{MOS}} = \begin{cases} C_{\mathrm{SiO2}} & \text{when carriers are accumulated in the pentacene} \\ 1/(1/C_{\mathrm{SiO2}} + 1/C_{\mathrm{semi}}) & \text{when no carrier presents in the pentacene} \end{cases}, \quad (2)$$

where $C_{\mathrm{SiO2}} = C_{\mathrm{OX}} S_{\mathrm{MOS}}$, $C_{\mathrm{semi}} = \varepsilon_{\mathrm{pen}} S_{\mathrm{MOS}}/d_{\mathrm{pen}}$, S_{MOS} is the area of the Au/pentacene/SiO_2/Cr structure, $\varepsilon_{\mathrm{pen}}$ is the dielectric constant, and d_{pen} is the thickness of the pentacene. Assuming that the pentacene/SiO_2/Cr structure is represented by a distributed constant circuit, the capacitance component C_{dis} in the admittance Y ($Y = G + jB = G + j2\pi f C_{\mathrm{dis}}$), which is composed of conductance G and susceptance B, is given by

$$C_{\mathrm{dis}} = C_{\mathrm{OX}} W_{\mathrm{dis}} L_{\mathrm{dis}} \frac{1}{\alpha} \frac{\sinh\alpha + \sin\alpha}{\cosh\alpha + \cos\alpha}, \quad (3)$$

where

$$\alpha = \sqrt{4\pi f C_{\mathrm{OX}} R_{\mathrm{sh}} L_{\mathrm{dis}}{}^2} \quad (4)$$

is a dimensionless quantity, R_{sh} is the sheet resistance in the pentacene layer, and f is the frequency for capacitance measurement.[32,33] Equation (3) can be derived by assuming that the line inductance and parallel resistance in a distributed constant circuit with open termination are equal to zero. When a function $g(\alpha)$ is defined as

$$g(\alpha) = \frac{1}{\alpha} \frac{\sinh\alpha + \sin\alpha}{\cosh\alpha + \cos\alpha}, \quad (5)$$

the function has the following properties:

$$\lim_{\alpha \to +0} g(\alpha) = 1, \quad (6a)$$

$$\lim_{\alpha \to +\infty} g(\alpha) = 0. \quad (6b)$$

Therefore, the dependence of C_{dis} on R_{sh} exhibits that

$$C_{\mathrm{dis}} \approx C_{\mathrm{OX}} W_{\mathrm{dis}} L_{\mathrm{dis}} \quad \text{for} \quad R_{\mathrm{sh}} << (1/fC_{\mathrm{OX}} L_{\mathrm{dis}}{}^2), \quad (7a)$$

$$C_{\mathrm{dis}} \approx 0 \quad \text{for} \quad R_{\mathrm{sh}} >> (1/fC_{\mathrm{OX}} L_{\mathrm{dis}}{}^2). \quad (7b)$$

Since pentacene is a *p*-channel material, the decreases in V_{G} leads to the accumulation of holes in a pentacene layer, the decrease in R_{sh}, and the asymptotic to ($C_0 + C_{\mathrm{SiO2}} + C_{\mathrm{OX}} W_{\mathrm{dis}} L_{\mathrm{dis}}$) of C. On the other hand, the increase in V_{G} leads to the depletion of holes, the increase in R_{sh}, and the asymptotic to $\{C_0 + 1/(1/C_{\mathrm{SiO2}}+1/C_{\mathrm{semi}})\}$ of C. Since R_{sh} is only an unknown

value in the equation for C, a value of R_{sh} can be estimated from an experimental C value.

For the Au/pentacene/SiO_2/Cr structure in Fig. 1(b), the bulk resistance for the pentacene and the contact resistance at the interface of Au and pentacene are not considered in this study. This is because we focus on the characteristics of C_{dis} for the pentacene/SiO_2/Cr structure. Although C defined in Eq. (1) does not contain effect of the resistances mentioned above, capacitances measured in this study are actually reproduced by the C defined in Eq. (1) as seen in Sect. 4.

2.2 Mobility and threshold voltage in uncovered pentacene layers

When V_G is applied to the Cr gate electrode, the sheet resistance R_{sh} induced by hole carriers accumulated in the pentacene layer can be expressed as

$$R_{sh} = \frac{1}{\mu C_{OX} |V_G - V_0|} \tag{8}$$

on the basis of the assumption that

$$R_{sh} = \frac{1}{\sigma \delta}, \tag{9a}$$

$$\sigma = en\mu = e\frac{n_S}{\delta}\mu = \frac{Q_S}{\delta}\mu, \tag{9b}$$

$$Q_S = C_{OX} |V_G - V_0|. \tag{9c}$$

Here, μ is the carrier mobility for the hole, σ is the conductivity, n is the density of the hole, δ is the thickness of the accumulation layer, n_S is the area density of the charge, Q_S is the surface charge density, and V_0 is the maximum value in voltages at which holes accumulate. V_0 corresponds to threshold voltage of the MOS transistor. The notation for the voltage V_0 is used to distinguish it from the threshold voltage estimated from experimental results of transistors. The R_{sh} value estimated from an experimental C depends on V_G. The μ and V_0 values can be calculated by fitting a curve to the relation between R_{sh} and V_G.

2.3 Characteristics of TFTs

In the gradual channel approximation, the drain current I_D flowing from the drain to the source for p-channel organic TFT is given by

$$I_{\mathrm{D}} = -\frac{1}{2}\mu_{\mathrm{FE}} C_{\mathrm{OX}} \frac{W}{L}(V_{\mathrm{G}} - V_{\mathrm{TH}})^2, \qquad \text{for } |V_{\mathrm{D}}| \geq |V_{\mathrm{G}} - V_{\mathrm{TH}}|, \tag{10a}$$

$$I_{\mathrm{D}} = -\mu_{\mathrm{FE}} C_{\mathrm{OX}} \frac{W}{L}\left[(V_{\mathrm{G}} - V_{\mathrm{TH}})V_{\mathrm{D}} - \frac{1}{2}{V_{\mathrm{D}}}^2\right], \qquad \text{for } |V_{\mathrm{D}}| \leq |V_{\mathrm{G}} - V_{\mathrm{TH}}| \tag{10b}$$

where μ_{FE} is the field-effect mobility, W and L are the channel width and length, V_{TH} is the threshold voltage, V_{G} and V_{D} are the source-gate and the source-drain voltages. In this study, the field-effect mobility (μ_{sat}) and V_{TH} values experimentally estimated in the saturation regime were calculated by fitting a line to a measured $|I_{\mathrm{D}}|^{1/2}$-V_{G} curve with Eq. (10a). The experimental field-effect mobility (μ_{lin}) in the linear regime was calculated from a measured $|I_{\mathrm{D}}|$-V_{G} curve using Eq. (10b).

When $|V_{\mathrm{D}}| << |V_{\mathrm{G}} - V_{\mathrm{TH}}|$, the drain current is approximated as

$$I_{\mathrm{D}} \cong -\mu_{\mathrm{FE}} C_{\mathrm{OX}} \frac{W}{L}(V_{\mathrm{G}} - V_{\mathrm{TH}})V_{\mathrm{D}}. \tag{11}$$

Equation (11) relates to Eq. (8). Actually, Eq. (8) is derived from Eq. (11) by dividing V_{D} by I_{D}. Since the structure in Fig. 1(a) corresponds to a transistor having no drain electrode, the measurement for the structure satisfies the condition that $|V_{\mathrm{D}}|$ is small.

2.4 Contact resistance and sheet resistance for TFTs

The on-resistance R_{on}, the channel resistance R_{ch}, and the contact resistance R_{C} for a TFT were calculated to compare R_{sh} estimated from C with the sheet resistance R_{TFT} calculated from the characteristics for the TFT. In the transfer line method,[15,16] the on-resistance, which is defined as $|\partial V_{\mathrm{D}}/\partial I_{\mathrm{D}}|$, is assumed to be

$$R_{\mathrm{on}} = R_{\mathrm{ch}} + R_{\mathrm{C}} = \frac{L}{\mu_{\mathrm{I}} W C_{\mathrm{OX}} |V_{\mathrm{G}} - V_{\mathrm{TH}}|} + R_{\mathrm{C}} \tag{12}$$

where μ_{I} is the mobility in the intrinsic transistor without contact resistance. R_{TFT} is given by

$$R_{\mathrm{TFT}} = R_{\mathrm{ch}} \frac{W}{L} = \frac{1}{\mu_{\mathrm{I}} C_{\mathrm{OX}} |V_{\mathrm{G}} - V_{\mathrm{TH}}|}. \tag{13}$$

As a result, Eq. (13) has the same form as Eq. (8).

3. Experimental method

Pentacene MOS capacitors and pentacene TFTs were fabricated on glass substrates, Corning (R) EAGLE XG. The cross sections are shown in Figs. 1(a) and 2(a), respectively. Each layer for the capacitor and the TFT was prepared by use of a metal mask common to the capacitor and the TFT. After cleaning the glass substrate, a 20-nm-thick Cr layer for the gate electrode was deposited on the glass substrate by thermal evaporation. Then, a 120-nm-thick SiO_2 gate dielectric was deposited by rf sputtering under a condition that a flat surface is obtained.[35] The SiO_2 dielectric had a capacitance per unit area (C_{OX}) of 26.5 nF/cm^2, which was determined by measurement of the capacitance at 1 kHz. The SiO_2 surface was treated with UV/ozone for 15 min, and was immediately exposed to hexamethyldisilazane (HMDS) vapor at 120 °C for about 30 min. A 45-nm-thick pentacene was deposited on the SiO_2 surface at room temperature. The deposition rate was 0.02 nm/s. Finally, a 45-nm-thick Au layer was deposited as the drain/source electrodes for TFTs and as the top electrode for MOS capacitors. For MOS capacitors, the width (W_{dis}) and length (L_{dis}) of an uncovered pentacene layer are 200 μm and in the range of 500 to 2500 μm, respectively. For TFTs, the channel width (W) and length (L) were 400 μm and in the range of 55 to 215 μm, respectively.

All the measurements were performed in a dry-nitrogen filled glovebox at room temperature. The capacitance characteristics of MOS capacitors were measured with a source/measurement unit, Keysight Technologies, B2912A. An AC voltage of 100 mVrms superimposed on a DC voltage was applied to the Cr gate electrode. The current characteristics of TFTs were measured with a semiconductor parameter analyzer, Agilent Technologies, B1500A.

4. Results and discussion

4.1 Transistor characteristics

Pentacene TFTs were fabricated on the same substrate for MOS capacitors in order to compare the characteristics of TFTs with those of MOS capacitors. The schematic illustration of the TFT is shown in Fig. 2(a). Figure 2(b) shows the transfer characteristics of a pentacene TFT with L = 115 μm measured at V_D = –20 V. The transfer curve showed characteristics of a typical p-channel organic TFT, and exhibited no large hysteresis in the forward and reverse sweep. For the TFT in Fig. 2(b), the μ_{sat} and V_{TH} values in the

saturation regime were estimated to 0.86 $cm^2\ V^{-1}\ s^{-1}$ and –4.51 V, respectively. The transfer characteristics in the saturation and linear regime of pentacene TFTs with different channel lengths are respectively shown in Figs. S1 and S2 in the online supplementary data. The μ_{lin}, μ_{sat} and V_{TH} values calculated from transfer characteristics are summarized in Table I. The μ_{lin} and μ_{sat} values did not largely depend on L. Although μ_{lin} was slight lower than μ_{sat}, the difference between μ_{lin} and μ_{sat} was not large. The averages of μ_{lin}, μ_{sat} and V_{TH} for TFTs with L = 55 to 215 μm were 0.79 $cm^2\ V^{-1}\ s^{-1}$, 0.84 $cm^2\ V^{-1}\ s^{-1}$ and –4.3 V, respectively. The mobilities are in the range of typical values for pentacene TFTs with top contact structure.[13,36)]

Figure 2(c) shows width-normalized R_{on} versus L calculated for the TFT of Fig. 2(b). The plots for each V_G is almost on a line. From Eqs. (12) and (13), the slope and the intercept of the line fitting to data of $R_{on}W$ versus L are equal to R_{TFT} and (R_C W), respectively. The R_C W values decreased with an increase of $|V_G - V_{TH}|$, and 3.24 kΩ cm for $V_G - V_{TH}$ = –4 V and 214 Ω cm for $V_G - V_{TH}$ = –20 V. The R_{on} W values of the TFT with L = 55 μm are equal to 52.06 kΩ cm for $V_G - V_{TH}$ = –4 V and 13.12 Ω cm for $V_G - V_{TH}$ = –20 V. The R_C W value is less than 10% of the R_{on} W value even if $V_G - V_{TH}$ = –4 V. The low contact resistance supports no large channel-length dependence of μ_{lin} and μ_{sat}. The output characteristics of pentacene TFTs with different channel lengths are shown in Fig. S3. It seems that the contact resistance did not largely influence on the output characteristics.

Figure 2(d) shows R_{TFT} obtained as a function of (V_G–V_{TH}). A curve fitting to the plots is obtained as

$$R_{TFT} = \frac{1}{(0.63\ \mathrm{cm^2\ V^{-1}\ s^{-1}}) \times C_{OX} \left| V_G - (V_{TH} + 0.10\ \mathrm{V}) \right|}. \quad (14)$$

The threshold voltage requires a small calibration of 0.10 V. On the other hand, the mobility μ_I is estimated to be 0.63 $cm^2\ V^{-1}\ s^{-1}$. Although R_{TFT} does not include the influence of contact resistance, the mobility estimated from Fig. 2(d) is lower than μ_{lin} and μ_{sat} calculated from transfer curves. The slope of the $|I_D|^{1/2}$-V_G curve in the saturation regime slightly increases with a decrease of V_G as seen in Fig. S1. Also, the $|I_D|$-V_G curve in the linear regime slightly differs from the linearly increase as seen in Fig. S2. The nonlinearity may lead to over-estimation in the mobility estimated from the transfer curve. Thus, it is possible that the mobility estimated from R_{TFT} is close to the intrinsic mobility in the

pentacene layer.

4.2 Characteristics of MOS capacitors

Figure 3(a) shows the capacitance-voltage (C-V) characteristics measured for a pentacene MOS capacitor of L_{dis} = 500 μm. The C-V characteristics had no large hysteresis in the forward and reverse sweep. For f = 1 and 10 Hz, the capacitance approaches 44.1 pF with a decrease of V_G. The value is close to (C_0 + C_{SiO2} + C_{OX} W_{dis} L_{dis}) = 42.4 pF. Thus, the approach is consistent with Eqs. (1), (2) and (7a). The capacitance of 44.1 pF indicates the accumulation of holes to the whole pentacene area of the pentacene/SiO_2/Cr structure. On the other hand, the capacitance at V_G > 5 V is about 15.7 pF for f = 1 to 1k Hz. The value is close to {C_0 + 1/(1/C_{SiO2} +1/C_{semi})} = 15.1 pF. Thus, the capacitance at V_G > 5 V is consistent with Eqs. (1), (2), and (7b). Note that it is difficult to know the accumulation of holes in the pentacene of the Au/pentacene/SiO_2/Cr structure from the C-V characteristics. This is because the difference between 1/(1/C_{SiO2} +1/C_{semi}) = 4.5 pF and C_{SiO2} = 5.3 pF is small. For f = 1 Hz, the C value dramatically decreases between V_G = −2 and 0 V. The gate voltage around −1 V corresponds to the threshold voltage V_0 in Eq. (9c) for a MOS capacitor.

Figure 3(b) shows the capacitance characteristics measured for pentacene MOS capacitors of L_{dis} = 500 to 2500 μm at f = 1 Hz. Since the MOS capacitors have different V_0, the horizontal axis is represented by (V_G−V_0). Here, the V_0 value roughly estimated from the C-V characteristics was used for Fig. 3(b). For all L_{dis}, the capacitance decreases down to 15.7 pF with an increase of (V_G−V_0). Since the MOS capacitors have the same S_0 and S_{MOS} values, the approach to 15.7 pF is reasonable. On the other hand, the capacitance at (V_G−V_0) = −5V depends on L_{dis}. The value of (C−15.7 pF) is almost proportional to L_{dis}. This indicates that holes accumulate to the whole pentacene area at (V_G−V_0) = −5V even for a long L_{dis} of 2500 μm.

Figure 4 shows the frequency dependence of C_{dis} at (V_G−V_0) of about −10V for L_{dis} = 500 to 2500 μm. For each L_{dis}, the C_{dis} value at f = 1 Hz almost equals (C−15.7 pF) for the C value at (V_G−V_0) = −5V shown in Fig. 3(b). The C_{dis} value gradually decreases with an increase of f. The dotted lines in Fig. 4 were obtained by fitting to the plots of C_{dis} with Eq. (3). For each L_{dis}, the plots are almost on the dotted line. This indicates that the frequency dependence of

C_{dis} is reproduced by Eq. (3), which is derived from the equivalent circuit shown in Fig. 1(c). In other words, C_{dis} at a certain V_G is determined by R_{sh} independent of f. Thus, R_{sh} at a certain V_G can be calculated from the C_{dis} at the V_G of the C-V characteristics using the inverse function of $g(\alpha)$ defined in Eq. (5). Note that the calculation of R_{sh} does not require the measurement of the frequency dependence of C_{dis}. In addition, the plots of C_{dis} measured are almost on the line fitting to them by use of Eq. (3) without the influence of the contact resistance. This suggests that the influence of the contact resistance on C_{dis} is negligible in the range of 1 Hz to 1 kHz. The low contact resistance described in Sect 4.1 also supports the suggestion. On the other hand, if a MOS capacitor with low channel resistance and/or large contact resistance is evaluated, the influence of the contact resistance should be considered.[27] In addition, the method is limited to a frequency range in which the presence of trap sites does not affect the admittance of evaluated MOS capacitor. If a MOS capacitor is evaluated at a frequency that trap sites affect the admittance, it is necessary to incorporate the component for the trap site into the admittance.[37]

4.3. Sheet resistance and mobility

The sheet resistance of pentacene MOS capacitors were calculated on the basis of method described in Sect. 4.2. Figure 5(a) shows the V_G dependence of R_{sh} for L_{dis} = 500 μm. Since the C-V characteristic at f = 100 Hz exhibits gradual change to V_G as seen in Fig. 3(a), the characteristic was used for the calculation of R_{sh}. The μ and V_0 values were estimated by fitting a curve to the plots of R_{sh} with Eq. (8). The plots are approximately on the dotted line obtained by the fitting. The agreement supports the validity of derivation process for Eq. (8) explained in Sect. 2.2.

Figure 5(b) shows mobilities μ_{sat}, μ_{lin} and μ_I for pentacene TFTs, and μ for pentacene MOS capacitors. The μ values were calculated from the V_G dependence of R_{sh}, and were in the range of 0.48 to 0.64 $cm^2\ V^{-1}\ s^{-1}$. The average of μ was 0.55 $cm^2\ V^{-1}\ s^{-1}$. As shown in Sect. 4.1, the values of μ_{sat} and the value of μ_I were 0.84 and 0.63 $cm^2\ V^{-1}\ s^{-1}$, respectively. On the other hand, the average of V_{TH} for Eq. (10a), the value of V_{TH} for Eq. (13), and the average of V_0 for Eq. (8) were −4.3, −4.2, and −3.7 V, respectively. The ascending order for V_{TH} and V_0 corresponds to the order of μ_{sat}, μ_I, and μ. The difference among V_{TH} and V_0 may relate to difference among μ_{sat}, μ_I, and μ. Another possibility of the reason is the difference in lateral

DC voltage in the channel layer. Drain current for calculation of the mobility in a TFT is measured under a condition that a DC voltage is applied to the drain electrode. On the other hand, capacitance for calculation of the mobility in a MOS capacitor is measured under a condition that no lateral DC voltage is applied to the channel layer. Thus, μ represents the intrinsic carrier mobility in the channel material under no static electric field.

5. Conclusions

We investigated the capacitance characteristics of pentacene MOS capacitors with pentacene area uncovered with the top electrode. The frequency dependence of the capacitance was reproduced using an equation including a capacitance component based on a distributed constant circuit for the uncovered pentacene area. The sheet resistance for the uncovered pentacene area was calculated as a function of gate voltage from the measured capacitance. The mobility of a MOS capacitor with a different length of an uncovered pentacene area was estimated by fitting a curve to the gate-voltage dependence of the sheer resistance. The mobility, which was in the range of 0.48 to 0.64 $cm^2\ V^{-1}\ s^{-1}$, has no large dependence on the length. The mobility is considered as an intrinsic mobility evaluated under a condition of no static lateral electric field.

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References

1) J. S. Chang, A. F. Facchetti, and R. Reuss, IEEE Trans. Emerg. Sel. Topics Circuits Syst. **7**, 7 (2017).
2) D. M. Taylor, Jpn. J. Appl. Phys. **55**, 02BA01 (2016).
3) N. T. Kalyani and S. J. Dhoble, Renew. Sust. Energ. Rev. **16**, 2696 (2012).
4) D. Volz, J. Photon. Energy **6**, 020901 (2016).
5) R. Ganesamoorthy, G. Sathiyan, and P. Sakthivel, Sol. Energy Mater. Sol. Cells **161**, 102 (2017).
6) A. Wadsworth, M. Moser, A. Marks, M. S. Little, N. Gasparini, C. J. Brabec, D. Baran, and I. McCulloch, Chem. Soc. Rev. **48**, 1596 (2019).
7) L. Torsi, M. Magliulo, K. Manoli, and G. Palazzo, Chem. Soc. Rev. **42**, 8612 (2013).
8) J. Liao, H. Si, X. Zhang, and S. Lin, Sensors **19**, 218 (2019).
9) K. Takimiya, I. Osaka, T. Mori, and M. Nakano, Acc. Chem. Res. **47**, 1493 (2014).
10) A. F. Paterson, S. Singh, K. J. Fallon, T. Hodsden, Y. Han, B. C. Schroeder, H. Bronstein, M. Heeney, I. McCulloch, and T. D. Anthopoulos, Adv. Mater. **30**, 1801079 (2018).
11) C. Groves, Rep. Prog. Phys. **80**, 026502 (2017).
12) N. Lu, L. Li, D. Geng, and M. Liu, Org. Electron. **61**, 223 (2018).
13) M. Kitamura and Y. Arakawa, J. Phys.: Condens. Matter **20**, 184011 (2008).
14) E. J. Meijer, G. H. Gelinck, E. van Veenendaal, B.-H. Huisman, D. M. de Leeuw, and T. M. Klapwijk, Appl. Phys. Lett. **82**, 4576 (2003).
15) D. J. Gundlach, L. Zhou, J. A. Nichols, T. N. Jackson, P. V. Necliudov, and M. S. Shur, J. Appl. Phys. **100**, 024509 (2006).
16) M. Kitamura, S. Aomori, J. H. Na, and Y. Arakawa, Appl. Phys. Lett. **93**, 033313 (2008).
17) I. Torres, D. M. Taylor, and E. Itoh, Appl. Phys. Lett. **85**, 314 (2004).
18) H. Hatta, Y. Miyagawa, T. Nagase, T. Kobayashi, T. Hamada, S. Murakami, K. Matsukawa, and H. Naito, Appl. Sci. **8**, 1493 (2018).
19) M. Yun, S. Gangopadhyay, M. Bai, H. Taub, M. Arif, and S. Guha, Org. Electron. **8**, 591 (2007).
20) K. Gooden, A. Laudari, G. Knotts, and S. Guha, Flex. Print. Electron. **1**, 015004 (2016).
21) W. T. Wondmagegn, N. T. Satyala, I. Mejia-Silva, D. Mao, S. Gowrisanker, H. N. Alshareef, H. J. Stiegler, M. A. Quevedo-Lopez, R. J. Pieper, and B. E. Gnade, Thin Solid Films **519**,

4313 (2011).

22) M. Estrada, F. Ulloa, M. Ávila, J. Sánchez, A. Cerdeira, A. Castro-Carranza, B. Iñíguez, L. F. Marsal, and J. Pallarés, IEEE Trans. Electron Devices **60**, 2057 (2013).
23) Y. Shao, Y. Zhang, W. He, C. Liu, T. Minari, S. Wu, M. Zeng, Z. Zhang, X. Gao, X. Lu, and J-M Liu, Semicond. Sci. Technol. **30**, 035005 (2015).
24) A. Nigam, P. R. Nair, M. Premaratne, and V. R. Rao, IEEE Electron Device Lett. **35**, 581(2014).
25) Md. Akhtaruzzaman, S. Ohmi, J. Nishida, Y. Yamashita, and H. Ishiwara, Jpn. J. Appl. Phys. **48**, 04C178 (2009).
26) B. L. Anderson and R. Anderson, *Fundamentals of Semiconductor Devices* (McGraw-Hill Education, NY, USA 2018) 2nd ed. Chap. 7.
27) B. H. Hamadani, C. A. Richter, J. S. Suehle, and D. J. Gundlach, Appl. Phys. Lett. **92**, 203303 (2008).
28) F. V. Di Girolamo, M. Barra, V. Capello, M. Oronzio, C. Romano, and A. Cassinese, J. Appl. Phys. **107**, 114508 (2010).
29) K.-D. Jung, C. A. Lee, D.-W. Park, B.-G. Park, H. Shin, and J. D. Lee, IEEE Electron Device Lett. **28**, 204 (2007).
30) T. Hayashi, N. Take, H. Tamura, T. Sekitani, and T. Someya, J. Appl. Phys. **115**, 093702 (2014).
31) C. Ucurum and H. Goebel, Microelectron. J. **44**, 606 (2013).
32) D. M. Taylor and N. Alves, J. Appl. Phys. **103**, 054509 (2008).
33) M. Ullah, D. M. Taylor, R. Schwödiauer, H. Sitter, S. Bauer, N. S. Sariciftci, and Th. B. Singh, J. Appl. Phys. **106**, 114505 (2009).
34) Y. Kimura, Y. Hattori, and M. Kitamura, Compound Semiconductor Week, 2019, [DOI: 10.1109/ICIPRM.2019.8819249].
35) H. Takahashi, M. Kitamura, Y. Hattori, and Y. Kimura, Jpn. J. Appl. Phys. **58**, SBBJ04 (2019).
36) Y. Kimura, M. Kitamura, A. Kitani, and Y. Arakawa, Jpn. J. Appl. Phys. **55**, 02BB14 (2016).
37) I. Torres and D. M. Taylor, J. Appl. Phys. **98**, 073710 (2005).

Figure Captions

Fig. 1. (a) Cross section of a pentacene MOS capacitor with an uncovered area examined in this study. (b) Structures separated into three parts of Au/SiO_2/Cr, Au/pentacene/SiO_2/Cr, and pentacene/SiO_2/Cr. (c) Distributed constant circuit adopted as an equivalent circuit for the pentacene/SiO_2/Cr structure uncovered with a top electrode. (d) Microphotograph of a fabricated pentacene MOS capacitor.

Fig. 2. (a) Cross section of a pentacene TFT. (b) Transfer characteristics measured at V_D = −20 V for a pentacene TFT with L = 115 μm. (c) Width-normalized on-resistance R_{on} W calculated for pentacene TFTs with L = 55, 75, …, 215 μm. (d) Sheet resistance R_{TFT} for pentacene TFTs calculated from the width-normalized on-resistance shown in (c); the dashed line is a line fitting to measured R_{TFT} represented by filled diamonds using Eq. (13).

Fig. 3. (a) C-V characteristics of a pentacene MOS capacitor with L_{dis} = 500 μm measured at f = 1, 10, 100, and 1k Hz. (b) C versus (V_G−V_0) characteristics of pentacene MOS capacitors with different L_{dis} measured at 1 Hz.

Fig. 4. C_{dis} versus f characteristics of pentacene MOS capacitors with different L_{dis} measured at (V_G−V_0) of about −10 V. The dasehed lines are lines fitting to measured C_{dis} data represnted by filled plots using Eq. (3).

Fig. 5. (a) Sheet resistance R_{sh} for pentacene MOS capacitors calculated from C-V characteristics; the dashed line is a line fitting to measured R_{sh} data (filled circule) using Eq. (8). (b) Mobility in the saturation regime (μ_{sat} ; filled diamond) and in the linear regime (μ_{lin} ; filled triangle) for individual pentacene TFTs; intrinsic mobility μ_I for pentacene TFTs (dashed line); carrier mobility μ for pentacene MOS capacitors (filled circle).

Table I. Electrical properties of pentacene TFTs with different channel lengths: mobility in the linear regime μ_{lin}, mobility in the saturation regime μ_{sat}, and threshold voltage V_{TH}.

L (μm)	μ_{lin} (cm V^{-1} s^{-1})	μ_{sat} (cm V^{-1} s^{-1})	V_{TH} (V)
55	0.81	0.86	−4.2
75	0.76	0.80	−4.3
95	0.77	0.82	−4.5
115	0.79	0.84	−4.7
215	0.80	0.83	−3.5

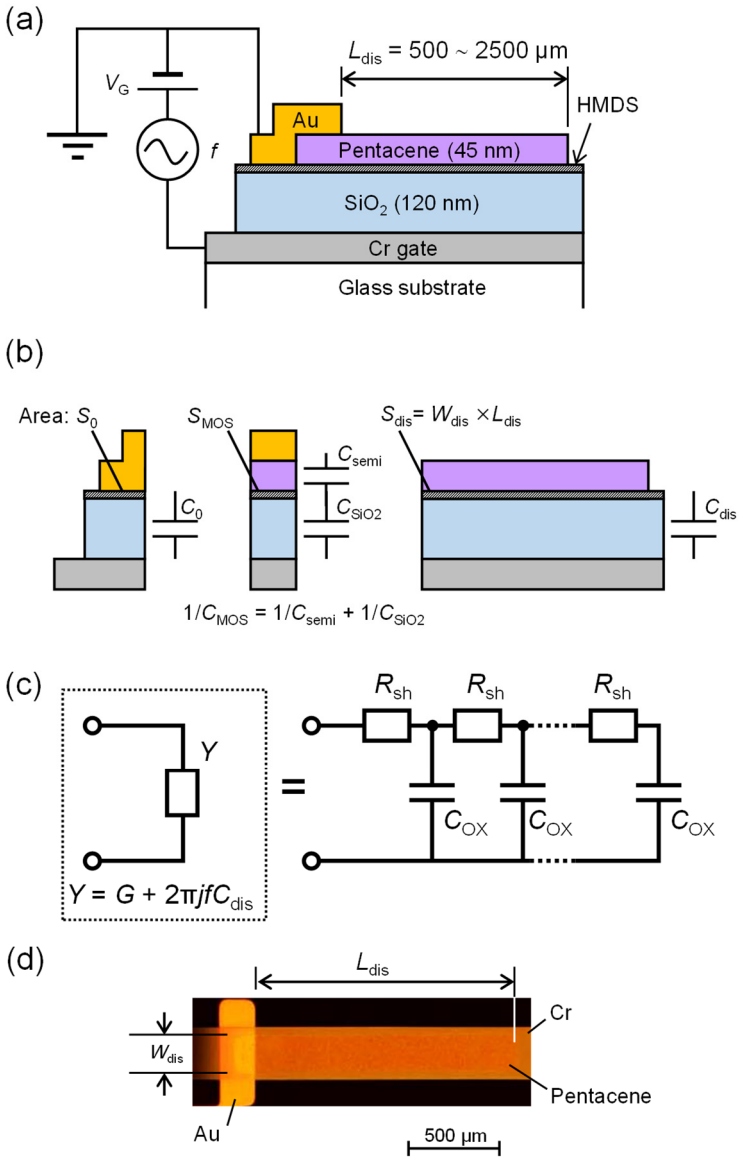
(a)
L_{dis} = 500 ~ 2500 μm
V_G
f
Au
HMDS
Pentacene (45 nm)
SiO_2 (120 nm)
Cr gate
Glass substrate
(b)
Area: S_0
S_{MOS}
S_{dis}= W_{dis} ×L_{dis}
C_{semi}
C_{SiO2}
C_0
C_{dis}
$1/C_{MOS} = 1/C_{semi} + 1/C_{SiO2}$
(c)
Y
$Y = G + 2\pi jfC_{dis}$
=
R_{sh}
R_{sh}
R_{sh}
C_{OX}
C_{OX}
C_{OX}
(d)
L_{dis}
W_{dis}
Cr
Pentacene
Au
500 μm

Fig.1.

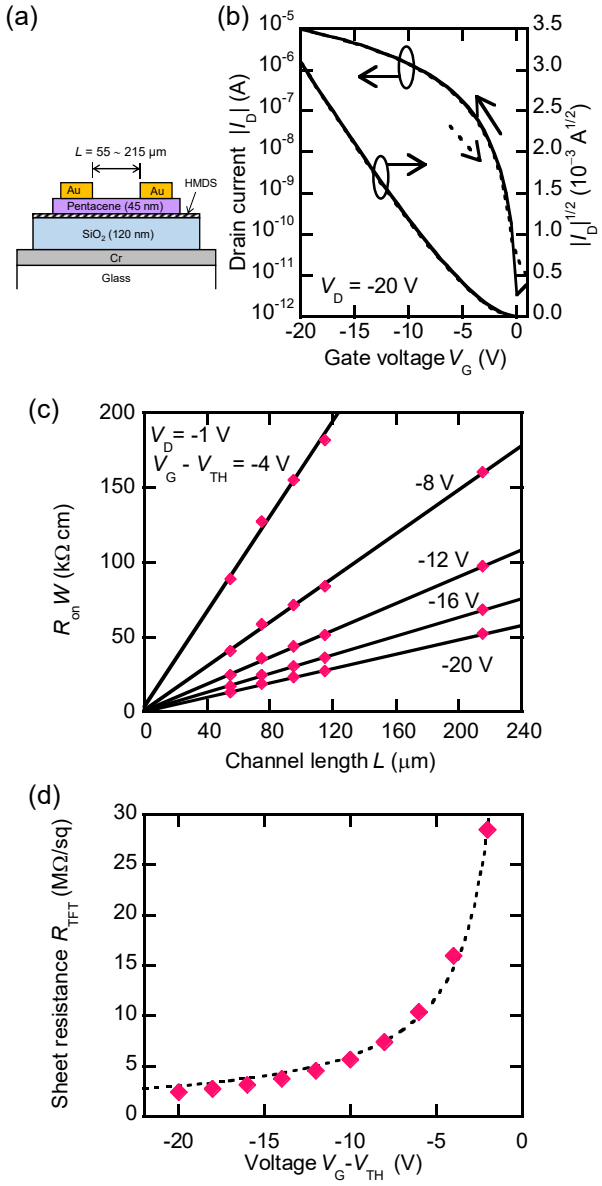
(a)
L = 55 ~ 215 μm
Au
Au
HMDS
Pentacene (45 nm)
SiO2 (120 nm)
Cr
Glass
(b)
Drain current |I_D| (A)
|I_D|^1/2 (10^-3 A^1/2)
V_D = -20 V
Gate voltage V_G (V)
(c)
V_D = -1 V
V_G - V_TH = -4 V
-8 V
-12 V
-16 V
-20 V
R_on W (kΩ cm)
Channel length L (μm)
(d)
Sheet resistance R_TFT (MΩ/sq)
Voltage V_G-V_TH (V)

Fig. 2.

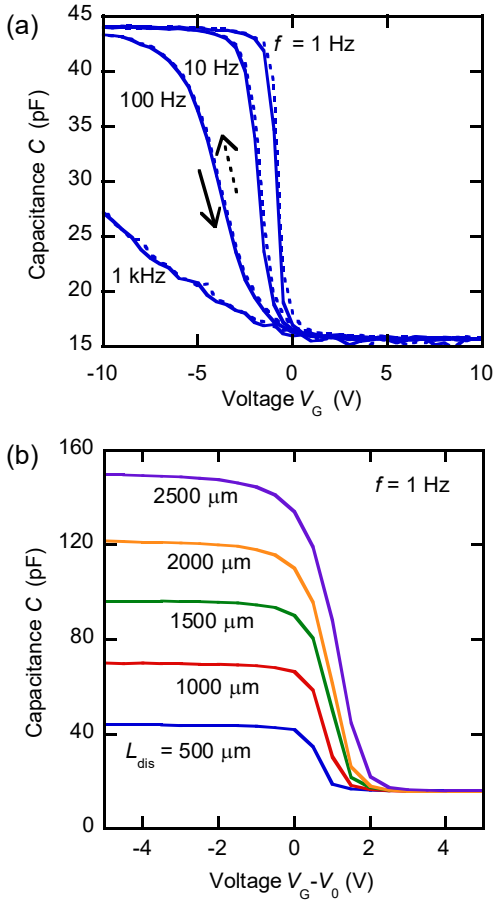
(a)
f = 1 Hz
10 Hz
100 Hz
1 kHz
Capacitance C (pF)
Voltage V_G (V)
(b)
f = 1 Hz
2500 μm
2000 μm
1500 μm
1000 μm
L_{dis} = 500 μm
Capacitance C (pF)
Voltage V_G-V_0 (V)

Fig. 3.

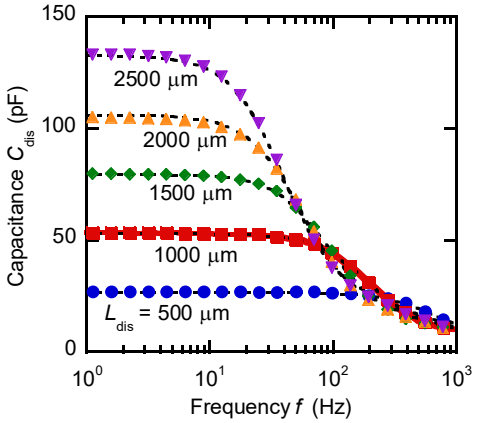
150
100
50
0
Capacitance C_{dis} (pF)
2500 μm
2000 μm
1500 μm
1000 μm
L_{dis} = 500 μm
10^0
10^1
10^2
10^3
Frequency f (Hz)

Fig. 4.

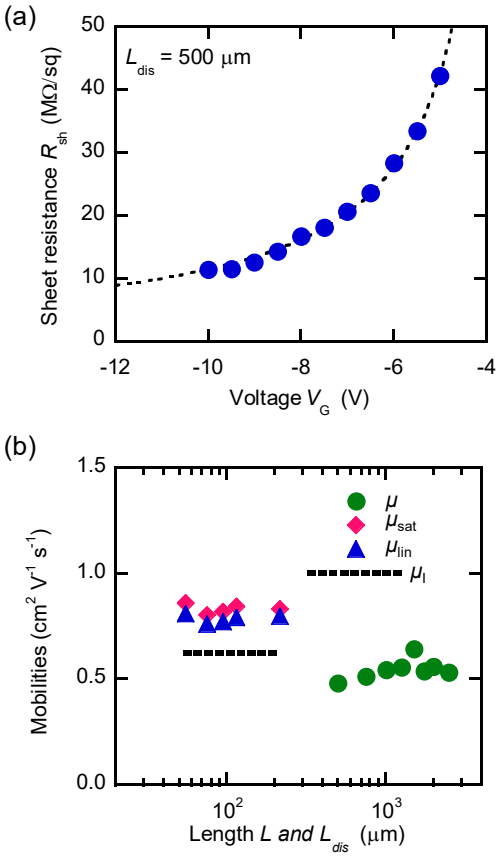
(a)
L_{dis} = 500 μm
Sheet resistance R_{sh} (MΩ/sq)
Voltage V_G (V)
(b)
μ
μ_{sat}
μ_{lin}
μ_I
Mobilities (cm^2 V^{-1} s^{-1})
Length L and L_{dis} (μm)

Fig. 5.

Evaluation of organic metal-oxide-semiconductor capacitors based on a distributed constant circuit

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Supplementary data

1. Transfer characteristics in the saturation regime of pentacene TFTs

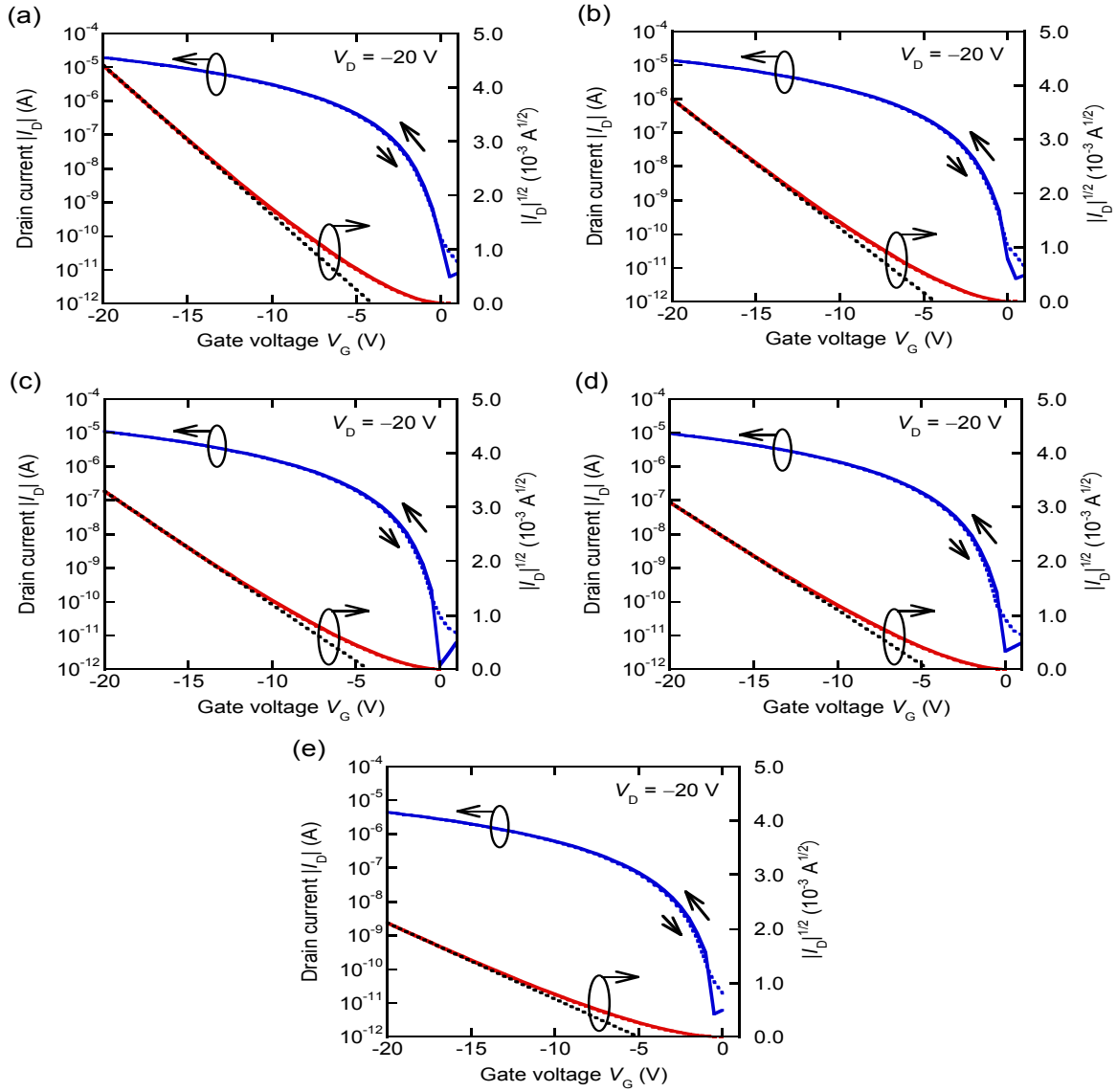

Fig. S1. The transfer characteristics in the saturation regime at a drain voltage of −20 V of pentacene TFTs. The channel lengths are (a) 55 μm, (b) 75 μm, (c) 95 μm, (d) 115 μm, and (e) 215 μm. The solid and dotted, colored lines are data taken from positive-to-negative (forward) and negative-to-positive (reverse) gate-voltage sweeps, respectively. The black dotted line is a line fitting to the $|I_D|^{1/2}$-V_G curve, being for estimation of μ_{sat} and V_{TH}.

2. Transfer characteristics in the linear regime of pentacene TFTs

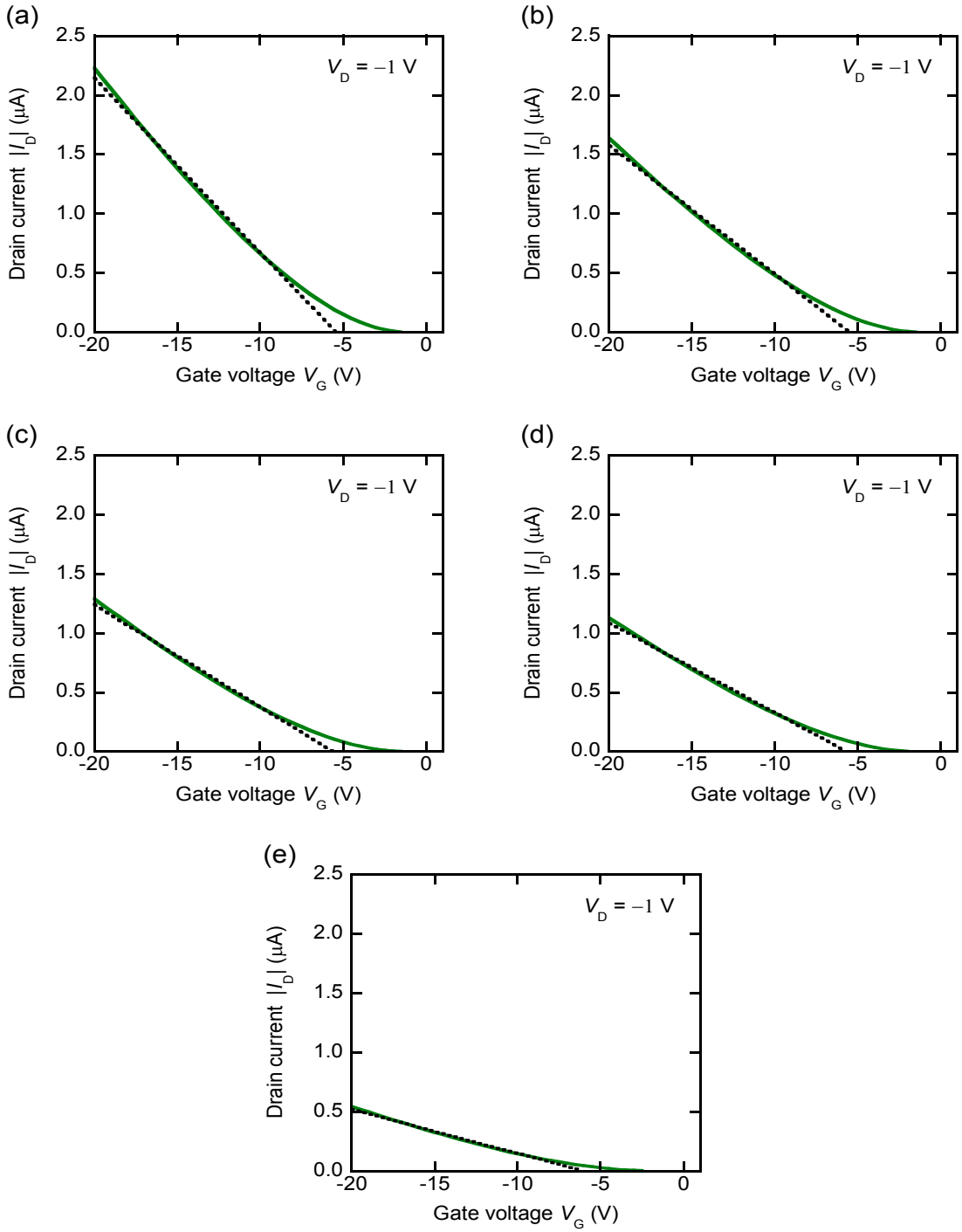

Fig. S2. The transfer characteristics in the linear regime at a drain voltage of −1 V of pentacene TFTs. The channel lengths are (a) 55 μm, (b) 75 μm, (c) 95 μm, (d) 115 μm, and (e) 215 μm. The solid and dotted, colored lines are data taken from positive-to-negative (forward) and negative-to-positive (reverse) gate-voltage sweeps, respectively. The black dotted line is a line fitting to the $|I_D|$-V_G curve, being for estimation of μ_{lin}.

3. Output characteristics of pentacene TFTs

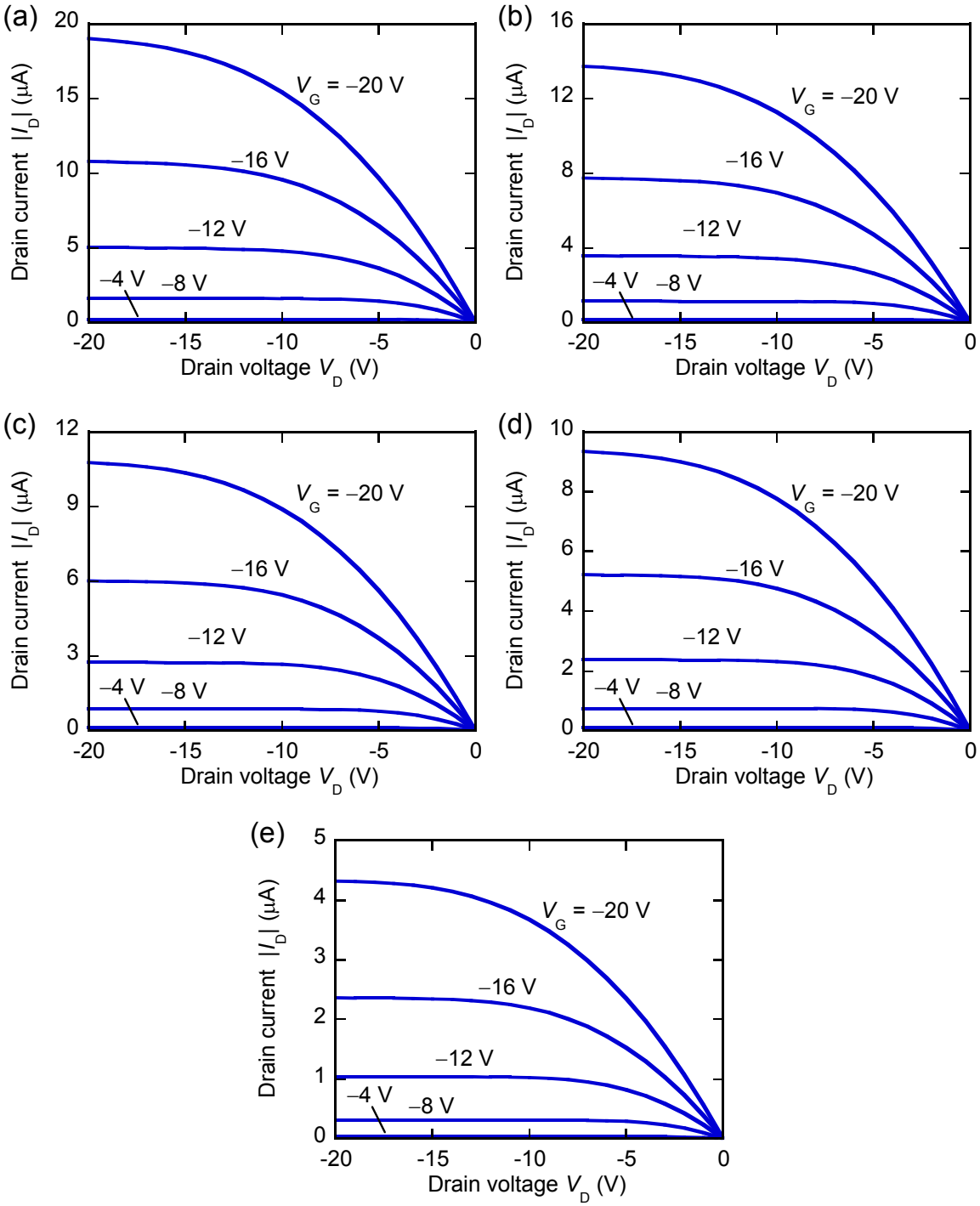

Fig. S3. The output characteristics at gate voltages of −4, −8, and −20 V of pentacene TFTs with channel lengths of (a) 55 μm, (b) 75 μm, (c) 95 μm, (d) 115 μm, and (e) 215 μm.