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Energy distribution of interface states generated by oxygen plasma treatment for control of threshold voltage in pentacene thin-film transistors

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Abstract

Pentacene metal-oxide-semiconductor (MOS) capacitors with a SiO_2 dielectric treated by oxygen plasma have been studied by capacitance-voltage (*C-V*) measurement to investigate the energy distribution of the interface states. Oxygen plasma treatment, which is used for control of the threshold voltage in pentacene thin-film transistors, shifted the *C-V* curves of pentacene MOS capacitors to positive gate voltage as well as the transfer curves of pentacene TFTs. The shift is explained by electrons captured at interface states generated by oxygen plasma treatment. The interface states capturing the electrons are expected to locate at low energy levels. The energy distribution of the interface states locating at middle or high energy levels was extracted by a method equivalent to Terman method. By use of the method in two steps, the interface state densities distributed at middle and high energy levels (D_M and D_H) were separately obtained. The D_M and D_H were of the order of 10^{10} – 10^{12} cm^{-2} eV^{-1}, and increased with an increase in plasma treatment time.

Keywords: interface states, MOS capacitors, C-V measurement, pentacene, oxygen plasma

1. Introduction

Organic thin-film transistors (TFTs) have attracted considerable attention because of their potential applications to large area, mechanically flexible, lightweight, and cost-effective devices [1-4]. In addition to the advantage, field-effect mobilities in organic TFTs have reached to about 10 cm^2 V^{-1} s^{-1} [5-9], which is close to those of oxide TFTs practically used in flat panel displays. For practical application, threshold voltage control in organic TFTs is an important issue as well as improvement of the performance. Some groups have been attempting threshold voltage control in organic TFTs using various methods such as using self-assembled monolayers (SAM) on a gate dielectric [10-13], utilizing new polymer gate dielectrics [14-16], doping into organic layers [17-19], choosing gate metals [20-22], adjusting parasitic resistance [23,24], and using multi gate structures [25,26].

Another approach of threshold voltage control adopted oxygen plasma treatment to the surface of gate dielectrics [27-30]. Oxygen plasma treatment has been used to obtain a hydrophilic surface for formation of a SAM on a gate dielectric [31,32]. Thus, the threshold voltage control by oxygen plasma treatment does not require an additional process if the organic TFT requires a SAM layer. In addition,

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the threshold voltage gradually changes with plasma treatment time. The continuous change is suitable for application to integrated circuits of organic TFTs. In actual, we applied pentacene TFTs with the controlled threshold voltage to logic circuits [33,34]. Since the threshold voltage shifts to positive gate voltage with plasma treatment time, the threshold voltage change is probably attributed to electrons captured at interface states generated by oxygen plasma treatment. Although a concern is that the change is temporary, we reported that gate bias stress does not negate the threshold voltage change provided by oxygen plasma treatment [29]. This implies that the interface states work as deep traps at low energy levels for electrons. On the other hand, the presence of electron traps at middle or high energy levels has been unclear.

For Si metal-oxide-semiconductor (MOS) field-effect transistors (FET), electron states at the interface between semiconductors and gate dielectric have been examined using some methods including electron spin resonance spectroscopy [35], current-voltage measurements [36], and capacitance-voltage (*C-V*) measurements [37,38]. Among the methods, *C-V* measurement has an advantage that the measurement is performed without light irradiation and elevated temperature. Since organic TFTs are generally sensitive to light and temperature change, *C-V* measurement is suitable for evaluation of organic TFTs and MOS capacitors. In actual, interface traps in organic MOS capacitors have been investigated by *C-V* measurement [39-42]. Also, we have reported *C-V* characteristics of pentacene MOS capacitors with a large uncovered pentacene area [43]. Thus, *C-V* measurement will be used for evaluation of organic MOS capacitors with a SiO_2 dielectric treated by oxygen plasma.

In this paper, we report *C-V* characteristics of pentacene MOS capacitors with a SiO_2 gate dielectric treated by oxygen plasma to examine the energy distribution of interface states generated by the treatment. First, we show current-voltage characteristics of pentacene TFTs to compare the characteristics with those of the MOS capacitors. Then, *C-V* characteristics of the MOS capacitors are shown. The energy distribution of the interface states is calculated from the *C-V* characteristics using a method equivalent to Terman method. [44-47]. The purpose of this study is to clarify the distribution, in particular, at middle or high energy levels. In addition, the originality of this study is that the *C-V* characteristics of a MOS capacitor without oxygen plasma treatment is used for a reference of the method. Actually, the *C-V* characteristics shifted by the threshold voltage change is adopted as the reference, and the influence of interface states at low energy levels, which relate to the threshold voltage change, is eliminated.

2. Analytical method

2.1 Threshold voltage of TFTs

Organic TFTs generally operate in the accumulation mode. The threshold voltage (V_{TH}) for an accumulation mode of MOS FETs equals a flat band voltage and is given by

$$V_{TH} = \frac{\Phi_M - \Phi_S}{q} - \frac{Q}{C_{OX}} \quad (1)$$

where q is the electron elementary charge, Φ_M and Φ_S are the work functions of the gate electrode and the organic semiconductor, respectively, C_{OX} is the gate capacitance per unit area, and Q is the charge density [48]. Q is written as

$$Q = Q_S + \int_0^d \frac{x}{d} \rho_{OX}(x) dx \quad (2)$$

where Q_S is the surface charge density at the interface between the gate dielectric and the semiconductor, and $\rho_{OX}(x)$ is the charge density per unit volume in the gate dielectric. The interfaces of the gate dielectric for the gate metal and the semiconductor are defined as $x = 0$ and d, respectively.

In this study, Q_S is assumed to be mainly induced by oxygen plasma treatment. Previous our work supports the assumption [29,30]. In addition, the work shows that Q_S is expressed as

$$Q_S = q_P t_P \quad (3)$$

where q_P is the surface charge density per unit time induced by oxygen plasma treatment, and t_P is the plasma treatment time. Sbstituting Eqs. (2) and (3) into Eq. (1), the V_{TH} is written as

$$V_{TH} = \frac{\Phi_M - \Phi_S}{q} - \frac{1}{C_{OX}}\left(q_P t_P + Q_0\right) \quad (4)$$

where

$$Q_0 = \int_0^d \frac{x}{d} \rho_{OX}(x) dx \, . \quad (5)$$

Under this assumption, the V_{TH} linearly changes as a function of t_P. Equation (4) is used for estimation of q_P and Q_0 in Sect. 4.

2.2 Characteristics of MOS capacitors

Figure 1 shows schematic band diagram of a SiO_2/pentacene MOS capacitor examined in this study. We attempt to estimate the interface state density by *C-V* measurement. The total capacitance per unit area of the MOS capacitor (C_G) is expressed as

$$1/C_G = 1/C_{OX} + 1/C_S. \quad (6)$$

where C_S is the capacitance per unit area of the pentacene layer. The capacitances C_G and C_S are functions of the gate voltage (V_G) and are represented as $C_G(V_G)$ and $C_S(V_G)$. The interface state density is experimentally classified into three groups denoted as D_L, D_M, and D_H. The D_L, D_M, and D_H are expected to be roughly distributed in ascending order shown in Fig. 1. Because the fixed charge in the gate dielectric is expect to be positive, it is represented by a plus sign.

Flat band voltage (V_{FB}) of a MOS capacitor without inversion mode is equal to V_{TH} as described above, and is written as

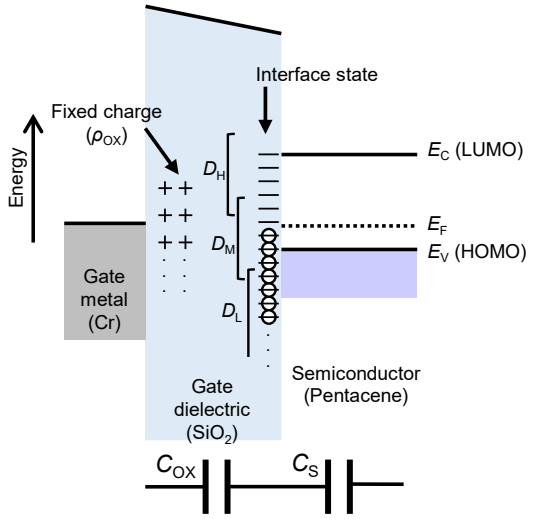

Figure 1. Schematic band diagram of a SiO_2/pentacene MOS structure.

$$V_{FB} = \frac{\Phi_M - \Phi_S}{q} - \frac{Q}{C_{OX}}. \quad (7)$$

When a V_{FB} value is experimentally obtained, Q is calculated from Eq. (7) as well as Q in Eq. (1). Also, Q_S, Q_0, and q_P can be calculated from V_{TH} for TFTs or V_{FB} for MOS capacitors. Thus, these values calculated from V_{TH} and V_{FB} are denoted such as $Q_{S,\,TFT}$ and $Q_{S,\,MOS}$, respectively, when distinguish them. Also, the V_{FB} value is used in an equation for surface potential shown below. An issue is how to determine V_{FB} experimentally. In this study, the V_{FB} value is experimentally determined as

$$C_S(V_{FB}) = 20 \min[C_S(V_G)]. \quad (8)$$

Although this definition is not standard, Eq. (8) for a MOS capacitor provides a V_{FB} value close to a V_{TH} value obtained from the current characteristics of a TFT prepared under the same condition as that of the MOS capacitor. Experimental results shown in Sect. 4 justify the definition of Eq. (8). Physically, Eq. (8) means that one twentieth thickness of a pentacene layer acts as insulator. In this study, the average thickness of a pentacene is about 22.5 nm as explained later. Thus, the one twentieth thickness is about 1.1 nm.

The interface state density (D_{it}) in an evaluated MOS capacitor is generally obtained as a function of the surface potential at the interface between the semiconductor and the gate dielectric. The surface potential Ψ_S is expressed as [44,49]

$$\Psi_S(V_G) = V_G - V_{FB} - \int_{V_{FB}}^{V_G} \left(\frac{C_G(V)}{C_{OX}} \right) dV \quad (9)$$

as a function of V_G and is constructed by using V_{FB} and $C_G(V_G)$. The calculation of D_{it} requires the C-V characteristic of a MOS capacitor, which ideally has no interface state, as a reference. Here, the surface potential and the total capacitance of the reference MOS capacitor are denoted as $\Psi_{ref}(V_G)$ and $C_{ref}(V_G)$, respectively. Using these notations, D_{it} can be given by

$$D_{it}(\Psi_S(V_G)) = \lim_{\Delta V_G \to 0} \frac{1}{q^2} \frac{\Delta Q_G - \Delta Q_{ref}}{\Psi_S(V_G + \Delta V_G) - \Psi_S(V_G)} \quad (10)$$

where

$$\Delta Q_G = \int_{V_G}^{V_G + \Delta V_G} C_G(V) dV \quad (11a)$$

$$\Delta Q_{ref} = \int_{V_G'}^{V_G' + \Delta V_G'} C_{ref}(V) dV \quad (11b)$$

The V_G' and $\Delta V_G'$ are defined as the following equations:

$$\Psi_{ref}(V_G') = \Psi_S(V_G), \quad (12a)$$

$$\Psi_{ref}(V_G' + \Delta V_G') = \Psi_S(V_G + \Delta V_G). \quad (12b)$$

The ΔQ_G and ΔQ_{ref} are charges stored in the evaluated and reference MOS capacitors, respectively, when the surface potential changes from $\Psi_S(V_G)$ to Ψ_S ($V_G + \Delta V_G$). V_G' and $\Delta V_G'$ are calculated from Eq. (12a) when values of V_G and ΔV_G are decided.

Equation (10) is mathematically equivalent to

$$D_{it}(\Psi_S) = \frac{C_{OX}}{q^2} \frac{d(V_G - V_G')}{d\Psi_S} \quad (13)$$

known as Terman method [44-47]. Derivation of Eq. (13) from Eq. (10) is written in the supplemental data. A calculated D_{it} value generally contains numerical errors. Thus, a value calculated from Eq. (10) may be slightly different from that calculated from Eq. (13). In actual, the difference was less than 1 % for calculation of D_M and less than 5 % for calculation of D_H. In this paper, $\Delta V_G = 0.5$ V and D_{it} calculated from Eq. (10) is shown. We show Eq. (10) for intuitive understanding that D_{it} directly relates to the difference between the stored charges. Also, we can see the increases in accumulated charges ΔQ_G and ΔQ_{ref} in the calculation process. Since V_G is discrete as ΔV_G = 0.5 V, it is necessary to approximately perform Eqs. (9)-(13). The calculation was performed by linear interpolation.

In general, other methods have been also used for determination of interface states [49]. One of them is conductance method that requires measurement of continuous frequency dependence of the admittance. On the other hand, Terman method does not require measurement of frequency dependence of capacitance. In addition, Terman method does not directly contain conductance element. Therefore, we used the method equivalent to Terman method. The method may be suitable for evaluation of a MOS capacitor having a low-mobility channel material such as an organic semiconductor. This is because the low conductivity in the material possibly causes unintentional error in conductance method.

3. Experimental method

Figure 2(a) and 2(b) shows cross sections of a pentacene TFT and a MOS capacitor, respectively. The fabrication process is almost the same as that of our previous study except for oxygen plasma treatment [43]. TFTs and MOS capacitors were fabricated on glass substrates, Corning (R) EAGLE XG.

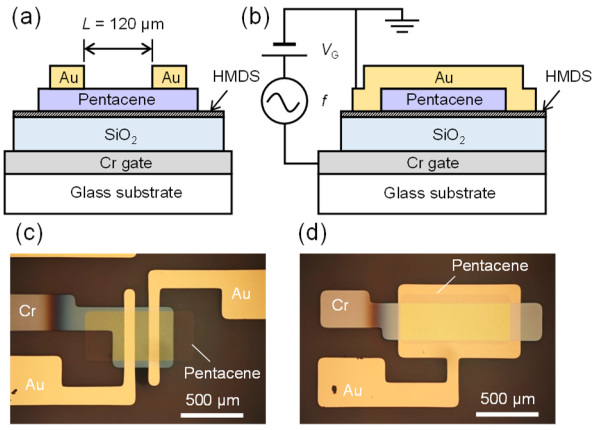

Figure 2. Cross sections of (a) a pentacene TFT and (b) a pentacene MOS capacitor. Microphotographs of (c) a fabricated pentacene TFT and (d) a fabricated pentacene MOS capacitor.

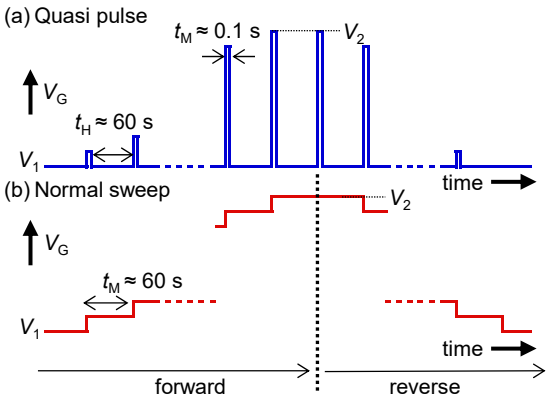

Figure 3. Waveforms of V_G applied for C-V measurement in (a) a quasi-pulse wave and (b) a normal sweep. A 100-mVrms AC voltage of a frequency of 200 Hz is superimposed on the V_G voltage for C-V measurement.

Each layer for the TFT and capacitor was deposited through a metal mask. First, a 20-nm-thick Cr layer was deposited as a gate electrode. Then, a SiO_2 layer was deposited as a gate dielectric by rf sputtering. The SiO_2 layer has a thickness of about 120 nm and a capacitance per unit area (C_{OX}) of about 27 nF cm^{-2}. Measured C_{OX} values are determined as the average value near to the maximum of C_G in accumulation regime from C-V measurement, and are shown in Table 2. The substrates were cleaned with acetone, isopropanol, and UV/ozone. Then, the SiO_2 surfaces were exposed to oxygen plasma for a time (t_P) of 10 to 30 s under a condition of an O_2 flow rate of 100 mL min^{-1} and an AC power for plasma generation of 9.2 W. After oxygen plasm treatment, or UV/ozone treatment as a reference without oxygen plasma treatment, the substrate was immediately exposed to hexamethyldisilazane (HMDS) vapor for 30 min at 120˚C. The TFT without oxygen plasma treatment is represented as t_P = 0 afterhere. A 45-nm-thick pentacene layer was deposited at a rate of 0.2 Å/s on the substrate of room temperature. Finally, a 45-nm-thick Au layer was thermally deposited as the top electrode of MOS capacitors and as the drain/source electrode of TFTs. For TFTs, the channel width (W) is 400 μm and the channel length (L) is 60, 80, 100, or 120 μm. For MOS capacitors, the MOS capacitor area of Au/pentacene/SiO_2/Cr structure is 2.7 × 10^{-3} cm^2. The MOS capacitor has an area of Au/SiO_2/Cr structure, which is 0.3 × 10^{-3} cm^2. Capacitance values excluding the capacitance of the Au/SiO_2/Cr area are shown as the capacitance of a MOS capacitor. Pentacene MOS capacitors and TFTs for a certain t_P value were fabricated at the same glass substrate.

All characteristics were examined in a dry-nitrogen filled glovebox at room temperature. The current-voltage characteristics of TFTs were measured by using a semiconductor parameter analyzer, Agilent Technologies, B1500A. The capacitance characteristics of MOS capacitors were measured by using a source/measurement unit, Keysight Technologies, B2912A. A 100-mVrms AC voltage of a frequency of 200 Hz superimposed on a DC voltage (V_G) was applied to the Cr electrode with respect to the Au electrode as seen in Fig. 2(b). The source/measurement unit exhibits good accuracy at frequencies of the order of 10 to 100 Hz rather than high frequencies. Thus, we measured C-V characteristics at a frequency of 200 Hz. The source/measurement unit can output a DC voltage more than 30 V for C-V measurement without an external power supply.

For MOS capacitors, the C-V measurement was performed in the range of $V_G = V_1$ to V_2 where V_1 = –10 V, V_2 = 10, 15, 18, and 23 V for t_P = 0, 10, 20, and 30 s, respectively. To change the number of charges trapped in the interface states at a certain V_G, we adopted two time-profiles of applied V_G shown in Figs. 3(a) and 3(b). One is a quasi-pulse wave and the other is a normal sweep. The holding voltage in the quasi-pulse wave, which was set at –10 V, contributes to suppression of unintended charge transfer under a certain V_G. C_G measured by a quasi-pulse wave and a normal sweep is denoted as $C_{G,\,pulse}$ and $C_{G,\,sweep}$ when distinguish them. In this study, the characteristics of capacitance is probably dominated by pulse width, t_M, shown in fig. 3(a) rather than frequency. This is because the characteristics of capacitance measured at a normal sweep is different from that measured at quasi pulses as shown in Fig. 7. Particularly, C-V characteristics did not largely depend on frequency as seen in Fig. S6 of supplemental data. In addition, capacitance measured at a certain V_G did not largely depends on frequency as seen in Fig. S7 of supplemental data.

4. Results and discussion

4.1 Transistor characteristics

Figure 4(a) shows the drain current (I_D) versus gate voltage (V_G) characteristics of pentacene TFTs with L = 120 μm in the saturation regime at a drain voltage (V_D) of –20 V. The I_D-V_G

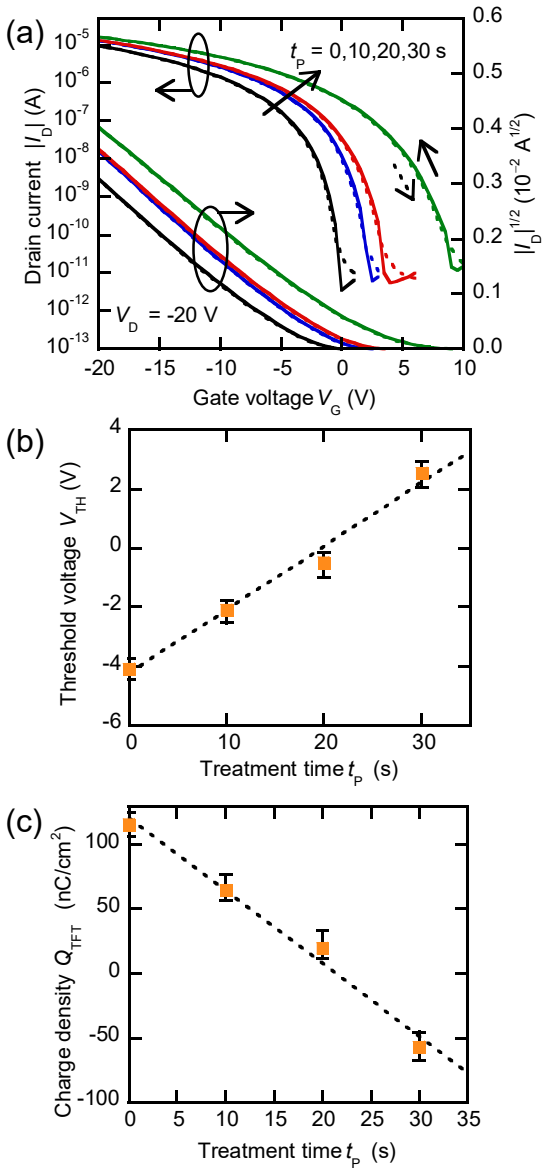

Figure 4. (a) Drain current versus gate voltage characteristics measured V_D = –20 V for pentacene TFTs having SiO_2 gate dielectrics treated by oxygen plasma for t_P = 0, 10, 20, and 30 s. (b) Threshold voltages estimated from the transfer characteristics of pentacene TFTs. (c) Charge density Q_{TFT} calculated from the threshold voltages in (b). The top and bottom of the error bar indicate the maximum and minimum values measured, respectively.

characteristics were obtained by a normal sweep from a positive V_G to –20 V, and the reverse sweep from –20 V to the positive V_G. The plasma treatment time t_P is 0, 10, 20, and 30 s. The I_D-V_G curves shift to positive gate voltages with increase in t_P. For $|I_D| > 10^{-10}$ A, the I_D-V_G curves do not exhibit large hysteresis in the forward and reverse sweeps. For $|I_D| < 10^{-10}$ A, a small hysteresis appears in the sweep. The hysteresis may relate to shallow traps shown as D_M and/or D_H in Fig. 1. The output characteristics are shown in Fig. S1 of supplemental data.

Table 1 Properties of pentacene TFTs estimated from the transfer characteristics: field-effect mobilities in the saturation regime μ_{SAT}, threshold voltage V_{TH}, sub-threshold swing S, charge densities $Q_{S,\,TFT}$. The value after ± indicates the standard deviation.

t_P (s)	μ_{SAT} (cm^2 V^{-1} s^{-1})	V_{TH} (V)	S (V/decade)	$Q_{S,TFT}$ (nF/cm^2)
0	0.84±0.05	–4.08±0.21	0.56±0.14	-
10	0.82±0.04	–2.09±0.27	0.65±0.04	–53.0±7.9
20	0.88±0.06	–0.47±0.24	0.72±0.33	–100.7±6.2
30	0.76±0.06	2.53±0.38	1.00±0.14	–177.6±9.6

The filed-effect mobilities in the saturation regime (μ_{SAT}), V_{TH}, and sub-threshold swing (S) are summarized in Table 1. These are the average measured for six to nine TFTs fabricated at the same substrate for each t_P. The μ_{SAT} and V_{TH} values are calculated by fitting a line to $|I_D|^{1/2}$-V_G plots as shown in Fig. S3 of supplemental data. The average μ_{SAT} values, calculated using C_{OX} value shown in Table 2, are in the range of 0.76 to 0.88 cm^2 V^{-1} s^{-1}, and does not largely depend on t_P. On the other hand, V_{TH} increases with an increase in t_P. In Fig. 4(b), V_{TH} is plotted with respect to t_P. By assuming values of Φ_M and Φ_S, Q in Eq. (2) can be calculated as a function of t_P. We used Φ_M = 4.8 eV and Φ_S = 4.5 eV for the calculation. Although Cr was used for the gate metal, the surface of Cr is easily oxidized in general. Thus, we adopted work function of 4.8 eV reported for Cr_2O_3 [50] as Φ_M. The Φ_S value corresponds to the Fermi energy of pentacene. Some groups have reported the Fermi energy of pentacene deposited on a underlayer as following: –4.35 eV on Au (5.2 eV) [51], –4.20 eV on Au (4.65 eV) [52], –4.53 eV on Au (4.8 eV) [53], and –4.57 eV on MoO_3 (6.95 eV) [54]. The value in the parentheses is the work function of the underlayer. Since the work function of 4.8 eV for Au reported in [53] equals 4.8 eV for C_2O_3, we used 4.5 eV as Φ_S.

Figure 4(c) shows Q_{TFT} calculated from Eq. (1). The Q_S (= q_P t_P) values are appended in Table 1. From the fitting curve, Q_0 and q_P are estimated to be 120 .5 nC/cm^2 and –5.64 nC cm^{-2} s^{-1}. By assuming that positive charges are uniformly distributed in SiO_2, ρ_0 is calculated as 2.0×10^{-2} C/cm^3 which corresponds to positive charges of 1.2×10^{17} cm^{-3}. The negative q_P value suggests that oxygen plasma treatment generates interface states serving as electron traps. Q_0 and q_P values have also been reported in our papers [29,33,34]. Note that Q_0 value depends on (Φ_M - Φ_S) values and contains error caused by the estimation errors of Φ_M and Φ_S values used. On the other hand, Q_S and q_P are not affected by the estimation error.

4.2 MOS capacitor characteristics

Figures 5(a)-5(d) shows the $C_{G,\,pulse}$ versus V_G characteristics of pentacene MOS capacitors for t_P = 0, 10, 20, and 30 s. Properties extracted from the $C_{G,\,pulse}$ characteristics are summarized in Table 2. For t_P = 10, 20, and 30 s, the C-V

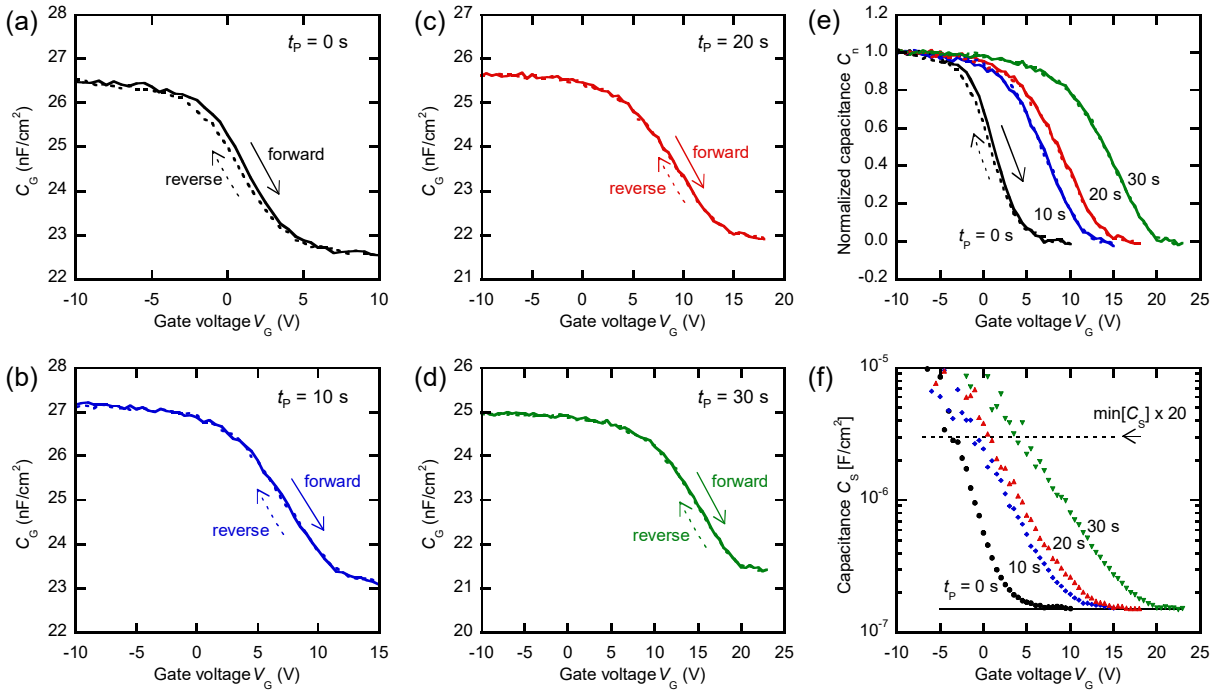

Figure 5. (a) *C-V* characteristics obtained by applying quasi-pulse waves of forward (solid line) and reverse (dotted line) for t_P = (a) 0 s, (b) 10 s, (c) 20

Table 2 Properties of pentacene MOS capacitors

t_P (s)	C_{OX} (nF/cm^2)	min[C_S] (nF/cm^2)	V_{FB} (V)	$Q_{S,MOS}$ (nF/cm^2)	$\|Q_{S,MOS}/q\|$ (cm^{-2})
0	26.5	155	–3.57	-	-
10	27.2	158	–0.77	–69.6	4.4×10^{11}
20	25.6	153	0.64	–107	6.7×10^{11}
30	25.0	153	3.61	–181	1.1×10^{12}

characteristics do not exhibit hysteresis in the forward and reverse measurement. This suggests that electrons trapped at the interface states by applying $V_G > -10$ V leave from the states when applying $V_G = -10$ V for a holding time of about 60 s. On the other hand, the *C-V* characteristic for $t_P = 0$ s exhibits a small hysteresis. The $C_{G,\ pulse}$ in the reverse measurement is slightly lower than that in the forward measurement. This may be due to the presence of hole traps at the interface without oxygen plasma treatment. The reason has been under investigation. The $C_{G,\ sweep}$ is shown with $C_{G,\ pulse}$ in Fig. S3 of supplemental data. All $C_{G,\ sweep}$-V_G curves exhibit large hysteresis in the forward and reverse sweeps. The hysteresis was observed in the $C_{G,\ sweep}$-V_G curve for $t_P = 0$ s as well as those for t_P = 10, 20, and 30 s. Thus, oxygen plasma treatment probably does not cause the hysteresis. We adopted quasi-pulse measurement to exclude the influence of the hysteresis.

The maximum and minimum values of C_G depend on the SiO_2 thickness. Although the SiO_2 layers were deposited under the same condition, unintentional difference in conditions leads to the difference in the SiO_2 thickness. For comparison of the *C-V* characteristics, we calculated a normalized capacitance C_n defined as

$$C_n(V_G) = \frac{C_G(V_G) - \min[C_G(V_G)]}{\max[C_G(V_G)] - \min[C_G(V_G)]}. \qquad (14)$$

In the calculation, average values near to the maximum and minimum of $C_G(V_G)$ are adopted as values of functions $\max[C_G(V_G)]$ and $\min[C_G(V_G)]$. As described in Sect. 3, $\max[C_{G,\ pulse}(V_G)]$ was adopted as C_{OX}. Figure 5(e) shows $C_{n,\ pulse}$ versus V_G of pentacene MOS capacitors for t_P = 0, 10, 20, and 30 s. The *C-V* curves shift to positive gate voltage with an increase in t_P.

The V_{FB} values were calculated based on Eq. (8). Figure 5(f) shows the C_S values calculated by substituting C_G values into Eq. (6). When V_G decrease to –20 V, accumulation of holes in the pentacene layer proceeds. Thus, C_S increases to infinity with a decrease in V_G. The increase in C_S shown in Fig. 5(f) is consistent with the explanation. On the other hand, the C_S decreases with an increase in V_G, and approaches 1.55, 1.58, 1.53, and 1.53×10^{-7} F/cm^2 for t_P = 0, 10, 20, and 30 s, respectively. From Eq. (8), the V_{FB} value, which equals V_G that satisfies C_S = 3.06-3.16 $\times 10^{-6}$ F/cm^2, are estimated to be –3.57, –0.77, 0.64, 3.61 V for t_P = 0, 10, 20, and 30 s, respectively. The V_{FB} values are summarized in Table 2 and Fig. S4(a). For each t_P, this value is close to the V_{TH} value shown in Table 1. The V_{FB} as well as V_{TH} can be used for estimation of Q, Q_0, and q_P. The calculated Q (Q_{MOS}) is shown in Fig. S4(b). Q_0 and q_P are estimated to be 98.7 nC/cm^2 and –5.92 nC cm^{-2} s^{-1}, which are not far from those estimated from

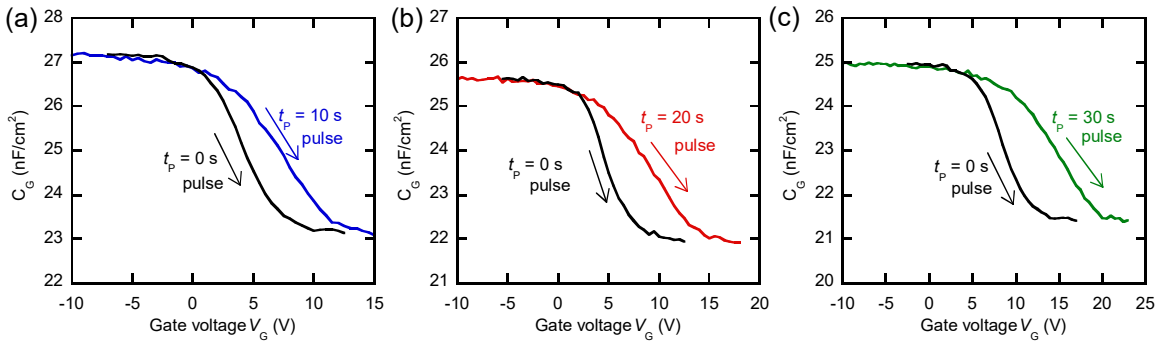

Figure 6. $C_{G,\,pulse}$ versus V_G characteristics for calculation of D_M for t_P = (a) 10 s, (b) 20 s, and (c) 30 s. $C_{G,\,pulse}$ for t_P = 0 s is shifted so that its V_{FB} equals V_{FB} of $C_{G,\,pulse}$ for t_P = 10 s, 20 s, or 30 s and is adjusted as its maximum and minimum fit to those of $C_{G,\,pulse}$ for t_P = 10 s, 20 s, or 30 s. The $C_{G,\,pulse}$ for t_P = 0 s was used as C_{ref}.

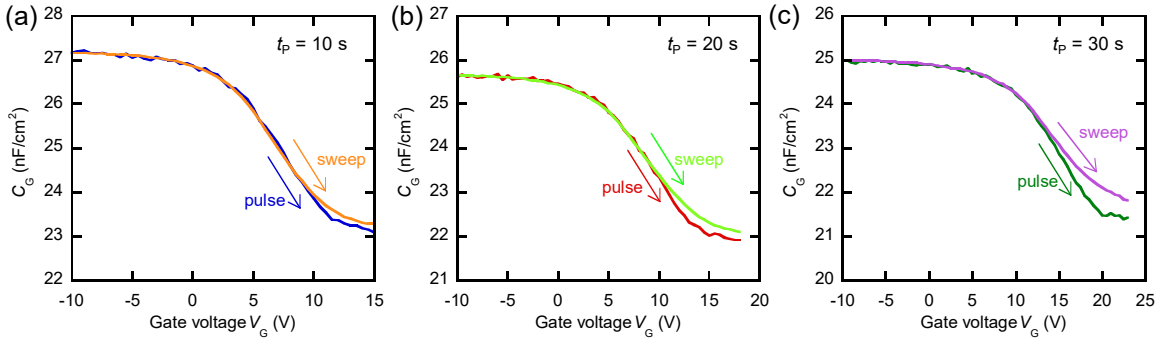

Figure 7. $C_{G,\,sweep}$ versus V_G and $C_{G,\,pulse}$ versus V_G characteristics for calculation of D_H for t_P = (a) 10 s, (b) 20 s, and (c) 30 s. The $C_{G,\,pulse}$ was used as C_{ref}.

V_{TH} because of small difference between V_{FB} and V_{TH}. Electrons that cause Q_S (= q_P t_P) probably capture at interface states. We classify the interface state density into D_L. This is because Q_S does not cause hysteresis in the transfer characteristics of pentacene TFTs. This indicate that D_L work as deep traps. Thus, D_L corresponds to low energy levels as shown in Fig. 1. Q_S is expressed as

$$Q_S = q\int D_L d\Psi \ . \qquad (15)$$

as integral of D_L with respective to potential Ψ. The area density $|Q_{S,\,MOS}/q|$ for D_L is shown in Table 2.

An increase in V_G leads to depletion of holes in the pentacene layer. Consequently, the minimum C_S corresponds to the capacitance of pentacene serving as insulator. By assuming the thickness of pentacene, the relative dielectric constant of the pentacene layer can be calculated from the minimum C_S. The thickness of 45 nm described in Sect. 3 is the thickness at the top of the pentacene. A pentacene generally has a dendritic structure. Thus, the average thickness is roughly assumed to be a half of 45 nm. Under this assumption, the relative dielectric constant is estimated to be 3.9. This value is almost the same as that reported by a group [55].

4.3 Interface state density

For calculation of $D_{it}(\Psi_S)$, $C_{G,\,pulse}$ and $C_{G,\,sweep}$ measured in the forward shown in Fig. 3 were used. The calculation of $D_{it}(\Psi_S)$ from Eq. (10) requires $C_{ref}(V_G)$ and $\Psi_{ref}(V_G)$. First, $D_{it}(\Psi_S)$ calculated from $C_{G,\,pulse}(V_G)$ for t_P = 10, 20, and 30 s are examined. For the calculation, $C_{G,\,pulse}(V_G)$ for t_P = 0 s are used as $C_{ref}(V_G)$. The $D_{it}(\Psi_S)$ is assigned as D_M. Next, $D_{it}(\Psi_S)$ calculated from $C_{G,\,sweep}$ (V_G) for t_P = 10, 20, and 30 s are examined. $C_{G,\,pulse}(V_G)$ for t_P = 10, 20, and 30 s are used as $C_{ref}(V_G)$ for the calculation from $C_{G,\,sweep}$ (V_G) for t_P = 10, 20, and 30 s, respectively. The $D_{it}(\Psi_S)$ is assigned as D_H. The justification of the assignment for D_M and D_H is discussed below. The $\Psi_S(V_G)$ calculated from $C_{G,\,pulse}$ and $C_{G,\,sweep}$ measured in the forward is shown in Fig. S5 of supplemental data.

Since a MOS capacitor of t_P = 0 s has no interface state generated by oxygen plasma treatment, we chose $C_{G,\,pulse}(V_G)$ of t_P = 0 as $C_{ref}(V_G)$. However, $C_{G,\,pulse}(V_G)$ of t_P = 10, 20, and 30 s involves the change in V_{FB} induced by the influence of D_L. To eliminate the influence, we shifted $C_{G,\,pulse}(V_G)$ of t_P = 0 by the difference in V_{FB} and used it as $C_{ref}(V_G)$. In addition, the maximum and minimum of $C_{ref}(V_G)$ were adjusted to the maximum and minimum of $C_G(V_G)$ of t_P = 10, 20, or 30 s, respectively. Figures 6(a)-6(c) shows $C_G(V_G)$ and $C_{ref}(V_G)$ curves for t_P = 10, 20, and 30 s. The $C_G(V_G)$ of $t_P > 0$ is larger than $C_G(V_G)$ of t_P = 0. The difference in $C_G(V_G)$ corresponds to electrons trapped at interface states for D_M.

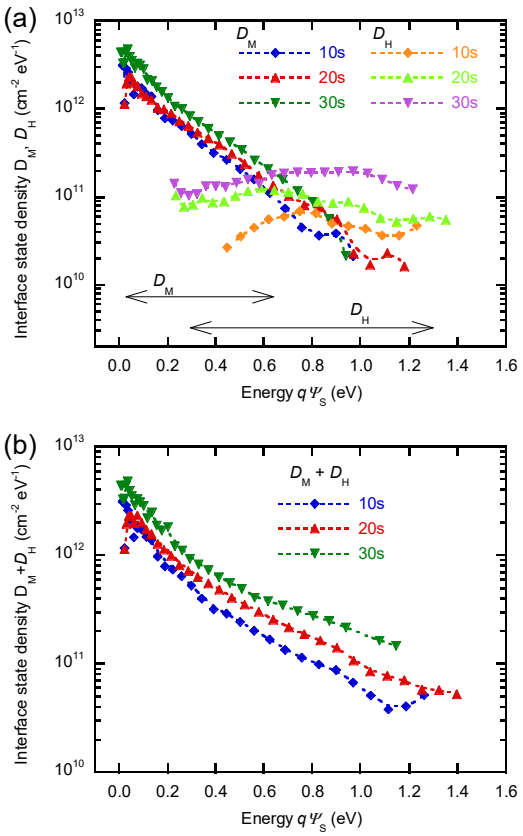

Figure 8. Interface state densities D_M and D_H for t_P = 10 s, 20 s, and 30 s. (b) Interface state densities calculated as ($D_M + D_H$).

For quasi-static voltage of the normal sweep, the bias stress at each V_G for about 60 s leads to electrons trapped at interface states locating at high energy levels. Figure 7 shows $C_{G,\,pulse}(V_G)$ and $C_{G,\,sweep}$ (V_G) versus V_G. For t_P = 10, 20, and 30, the difference in $C_{G,\,pulse}(V_G)$ and $C_{G,\,sweep}$ (V_G) increase at V_G > 10. The difference in $C_G(V_G)$ corresponds to electrons trapped at interface states for D_H. The $C_{G,\,pulse}(V_G)$ adopted as $C_{ref}(V_G)$ involves the influence of D_M. It is expected that D_H is distributed at high energy levels.

Figure 8(a) shows D_M and D_H calculated form $C_G(V_G)$ and $C_{ref}(V_G)$ explained above. Indeed, D_M locates near $q\Psi_S = 0$ as shown in Fig. 1 and gradually decreases with an increase in Ψ_S. The D_M are distributed in the range of $q\Psi_S$ = 0.0 – 0.6 eV. For example, the D_M values at $q\Psi_S$ = 0.2 eV are 7.6 × 10^{11}, 9.3 × 10^{11}, and 1.3 × 10^{12} cm^{-2} eV^{-1} for t_P = 10, 20, and 30 s, respectively. These values increase with plasma treatment time. For $q\Psi_S$ > 0.8 eV, D_M is less than D_H. On the other hand, D_H obtained by a normal sweep is distributed at high energy as compared with D_M obtained by a quasi-pulse wave. The result is also expected from Fig. 7. The D_H is broadly distributed in the range of $q\Psi_S$ = 0.4 – 1.3 eV, and is in the range of 4 × 10^{10} to 2 × 10^{11} cm^{-2} eV^{-1}. For $q\Psi_S$ = 0.6 – 1.0 eV, the D_H is about 5.6 × 10^{10}, 9.7 × 10^{10}, and 1.8 × 10^{11}cm^{-2} eV^{-1} on average for t_P = 10, 20, and 30, respectively. In the method of this study, D_M and D_H can be interpreted as density of states which trap electrons at each Ψ_S for t_M. Since t_M = 0.1 s for D_M and t_M = 60 s for D_H, D_H represents states that take a long time to trap as compared to D_M. Thus, Fig. 8(a) suggests that the trapping at $q\Psi_S$ > 0.7 eV takes longer time than that at $q\Psi_S$ < 0.7 eV.

Figure 8(b) shows interface state densities calculated as ($D_M + D_H$). The total distribution of the interface state can be seen from Fig. 8(b). The ($D_M + D_H$) monotonically decreases on average with an increase in $q\Psi_S$. The values of ($D_M + D_H$) are comparable to those of MOS capacitors having crystal Si [35], amorphous Si [36], SiC [56], GaN [57], and polymers [58,59] as a semiconductor. When integrating ($D_M + D_H$) with respect to $q\Psi_S$, the area densities are obtained as 4.9, 6.2, and 9.7 × 10^{11} cm^{-2} for t_P = 10, 20, and 30 s, respectively. The area density is close to $Q_{S,MOS}/q$ relating to D_L shown in Table 2. The increase of ($D_M + D_H$) with t_P is similar to the increases in $Q_{S,MOS}/q$. We predict that the origin of the trap is excess oxygen atoms, such as ≡Si–O–O–Si≡, ≡Si–O–O·, and ≡Si–O·, generated by oxygen plasm treatment [24,60]. Here, "≡" and "–" denote three and one network between O and Si, respectively, and "·" represents an unpaired electron. The increase in t_P leads to the increase of the excess oxygen atoms in SiO_2. The explanation is consistent with the increases of ($D_M + D_H$) and $Q_{S,MOS}/q$. The energy levels of point defects for ≡Si–O–O–Si≡, ≡Si–O–O·, and ≡Si–O· are placed between the valence band edge of perfect SiO_2 and the energy level of the highest occupied molecular orbital of pentacene [24]. Probably, total distribution of (D_L + D_M + D_H) exhibits the maximum at an energy level close to those of the point defect. Generally, the energy level of point defects in amorphous material has distribution. Thus, the decrease in Fig. 8 may exhibit tail of the distribution of (D_L + D_M + D_H).

Probably, the interface states for D_M and D_H do not largely influence on the characteristics of TFTs when TFTs operates at V_G < 0. Conversely, positive V_G may temporarily lead to threshold voltage shift by electrons trapped at the interface states for D_M and D_H. The finding in this study is useful for operational stability in organic TFTs. The interface states at high energy level such as D_M and D_H may be used for applications that intentionally require temporary characteristic changes.

5. Conclusion

We measured *C-V* characteristics of pentacene MOS capacitors with a SiO_2 dielectric treated by oxygen plasma to extract the energy distribution of the interface states. For the pentacene MOS capacitors, the V_{FB} determined by the definition in this study were close to those of threshold voltages estimated from transfer curves of pentacene TFTs. The V_{FB} values increased with an increase in plasma treatment time. First, the *C-V* characteristics of MOS capacitors without oxygen plasma treatment was used as a reference for extraction of energy distribution. The interface states

extracted from the *C-V* characteristics measured by applying a quasi-pulse wave voltage were distributed in the range of Ψ_S = 0.0 – 0.6 eV. The interface state density has the maximum of about 4×10^{12} cm^{-2} eV^{-1} and gradually decreases with an increase in Ψ_S. Next, the *C-V* characteristics for a quasi-pulse wave voltage was used as a reference. The interface states extracted from the *C-V* characteristics measured by applying a normal sweep voltage were broadly distributed in the range of Ψ_S = 0.4 – 1.3 eV. The interface density is in the range of 4×10^{10} to 2×10^{11} cm^{-2} eV^{-1}. The information of the energy distribution contributes to development of inorganic FET with oxide gate dielectric as well organic TFTs.

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Energy distribution of interface states generated by oxygen plasma treatment for control of threshold voltage in pentacene thin-film transistors

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Supplementary data

1. Derivation of the equation for Terman method

In this section, Eq. (13) used for Terman method is derived from Eq. (10):

$$D_{\mathrm{it}}\left(\Psi_{\mathrm{S}}(V_{\mathrm{G}})\right)=\lim_{\Delta V_G\to 0}\frac{1}{q^2}\frac{\Delta Q_{\mathrm{G}}-\Delta Q_{\mathrm{ref}}}{\Psi_{\mathrm{S}}(V_{\mathrm{G}}+\Delta V_{\mathrm{G}})-\Psi_{\mathrm{S}}(V_{\mathrm{G}})}. \tag{10}$$

By substituting Eq. (9) into Eq. (11a), we obtain

$$\begin{aligned}\Delta Q_{\mathrm{G}} &= \int_{V_{\mathrm{G}}}^{V_{\mathrm{G}}+\Delta V_{\mathrm{G}}} C_{\mathrm{G}}(V)dV \\ &= \left[-C_{\mathrm{OX}}\Psi_{\mathrm{S}}(V_{\mathrm{G}}+\Delta V_{\mathrm{G}})+C_{\mathrm{OX}}\left(V_{\mathrm{G}}+\Delta V_{\mathrm{G}}-V_{\mathrm{FB}}\right)\right]-\left[-C_{\mathrm{OX}}\Psi_{\mathrm{S}}(V_{\mathrm{G}})+C_{\mathrm{OX}}\left(V_{\mathrm{G}}-V_{\mathrm{FB}}\right)\right] \\ &= -C_{\mathrm{OX}}\left[\Psi_{\mathrm{S}}(V_{\mathrm{G}}+\Delta V_{\mathrm{G}})-\Psi_{\mathrm{S}}(V_{\mathrm{G}})\right]+C_{\mathrm{OX}}\Delta V_{\mathrm{G}}\end{aligned}. \tag{S1}$$

Surface potential $\Psi_{\mathrm{ref}}(V_{\mathrm{G}})$ is expressed as

$$\Psi_{\mathrm{ref}}(V_{\mathrm{G}})=V_{\mathrm{G}}-V_{\mathrm{FB}}'-\int_{V_{\mathrm{FB}}'}^{V_{\mathrm{G}}}\left(\frac{C_{\mathrm{ref}}(V)}{C_{\mathrm{OX}}}\right)dV \tag{S2}$$

where V_{FB}' is flat band voltage determined from $C_{\mathrm{ref}}(V_{\mathrm{G}})$. By substituting Eq. (S2) into Eq. (11b), we have

$$\begin{aligned}\Delta Q_{\mathrm{ref}} &= \int_{V_{\mathrm{G}}'}^{V_{\mathrm{G}}'+\Delta V_{\mathrm{G}}'} C_{\mathrm{ref}}(V)dV \\ &= \left[-C_{\mathrm{OX}}\Psi_{\mathrm{ref}}(V_{\mathrm{G}}'+\Delta V_{\mathrm{G}}')+C_{\mathrm{OX}}\left(V_{\mathrm{G}}'+\Delta V_{\mathrm{G}}'-V_{\mathrm{FB}}'\right)\right]-\left[-C_{\mathrm{OX}}\Psi_{\mathrm{ref}}(V_{\mathrm{G}}')+C_{\mathrm{OX}}\left(V_{\mathrm{G}}'-V_{\mathrm{FB}}'\right)\right] \\ &= -C_{\mathrm{OX}}\left[\Psi_{\mathrm{ref}}(V_{\mathrm{G}}'+\Delta V_{\mathrm{G}}')-\Psi_{\mathrm{S}}(V_{\mathrm{G}}')\right]+C_{\mathrm{OX}}\Delta V_{\mathrm{G}}'\end{aligned} \tag{S3}$$

as well as Eq. (S1). Using (S1) and (S3), we get

$$\begin{aligned}\Delta Q_{\mathrm{G}}-\Delta Q_{\mathrm{ref}} &= \left\{-C_{\mathrm{OX}}\left[\Psi_{\mathrm{S}}(V_{\mathrm{G}}+\Delta V_{\mathrm{G}})-\Psi_{\mathrm{S}}(V_{\mathrm{G}})\right]+C_{\mathrm{OX}}\Delta V_{\mathrm{G}}\right\} \\ &\quad -\left\{-C_{\mathrm{OX}}\left[\Psi_{\mathrm{ref}}(V_{\mathrm{G}}'+\Delta V_{\mathrm{G}}')-\Psi_{\mathrm{S}}(V_{\mathrm{G}}')\right]+C_{\mathrm{OX}}\Delta V_{\mathrm{G}}'\right\} \\ &= C_{\mathrm{OX}}\left(\Delta V_{\mathrm{G}}-\Delta V_{\mathrm{G}}'\right)\end{aligned}. \tag{S4}$$

Here, we use Eqs. (12a) and (12b). By substituting (S4) into Eq. (10), Eq. (13) is obtained as following:

$$\begin{aligned}D_{\mathrm{it}}\left(\Psi_{\mathrm{S}}(V_{\mathrm{G}})\right) &= \lim_{\Delta V_G\to 0}\frac{1}{q^2}\frac{\Delta Q_{\mathrm{G}}-\Delta Q_{\mathrm{ref}}}{\Psi_{\mathrm{S}}(V_{\mathrm{G}}+\Delta V_{\mathrm{G}})-\Psi_{\mathrm{S}}(V_{\mathrm{G}})} \\ &= \lim_{\Delta V_G\to 0}\frac{1}{q^2}\frac{C_{\mathrm{OX}}\left(\Delta V_{\mathrm{G}}-\Delta V_{\mathrm{G}}'\right)}{\Psi_{\mathrm{S}}(V_{\mathrm{G}}+\Delta V_{\mathrm{G}})-\Psi_{\mathrm{S}}(V_{\mathrm{G}})} \\ &= \frac{C_{\mathrm{OX}}}{q^2}\frac{d\left(V_{\mathrm{G}}-V_{\mathrm{G}}'\right)}{d\Psi_{\mathrm{S}}}\end{aligned}. \tag{S5}$$

Thus, V_{G} and V_{G}' satisfy the relationship Eq. (12a). In other word, V_{G}' is calculated from Eq. (12a) when a value of V_{G} is decided.

2. Pentacene TFT characteristics

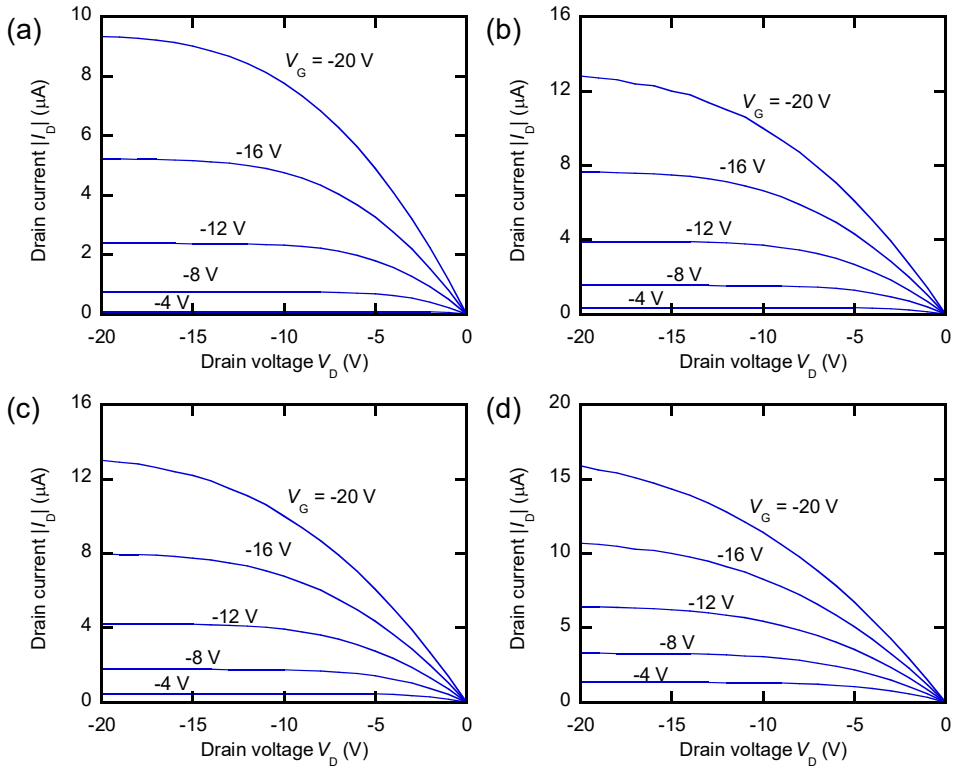

Figure S1. Output characteristics of typical pentacene TFTs with L = 120 μm for t_P = (a) 0 s, (b) 10 s, (c) 20 s, and (d) 30 s.

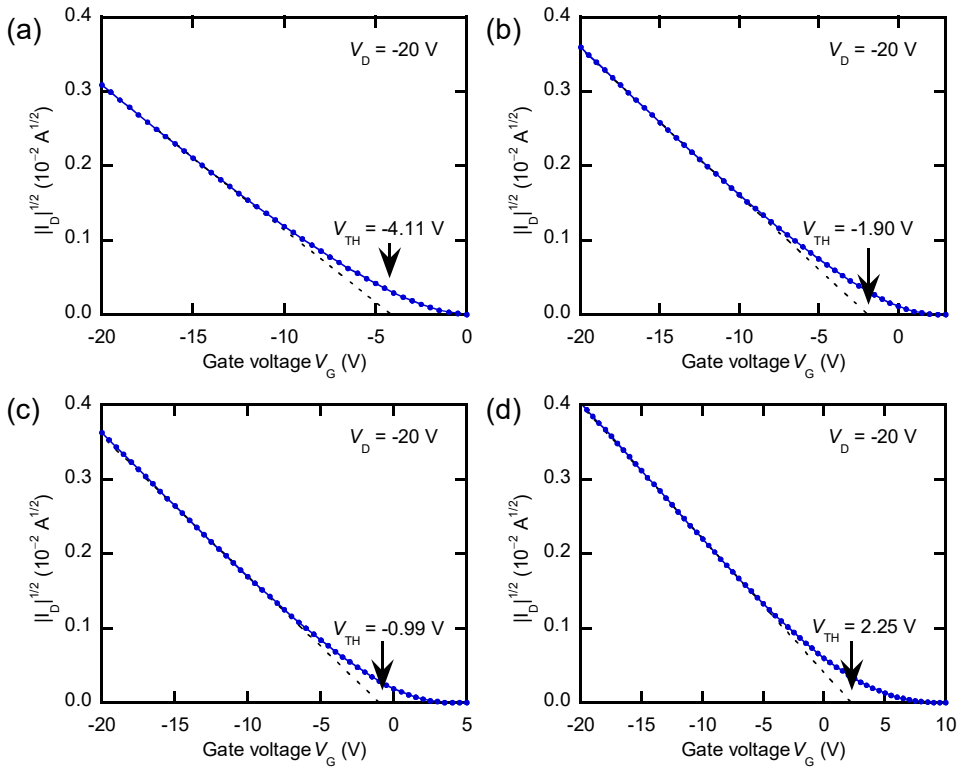

Figure S2. Transfer characteristics in the saturation regime at V_D = −20 V of typical pentacene TFTs with L = 120 μm for t_P = (a) 0 s, (b) 10 s, (c) 20 s, and (d) 30 s. The fitting lines for estimation of field-effect mobilities and threshold voltage are shown in these figures with estimated V_{TH} values.

3. Pentacene MOS capacitor characteristics

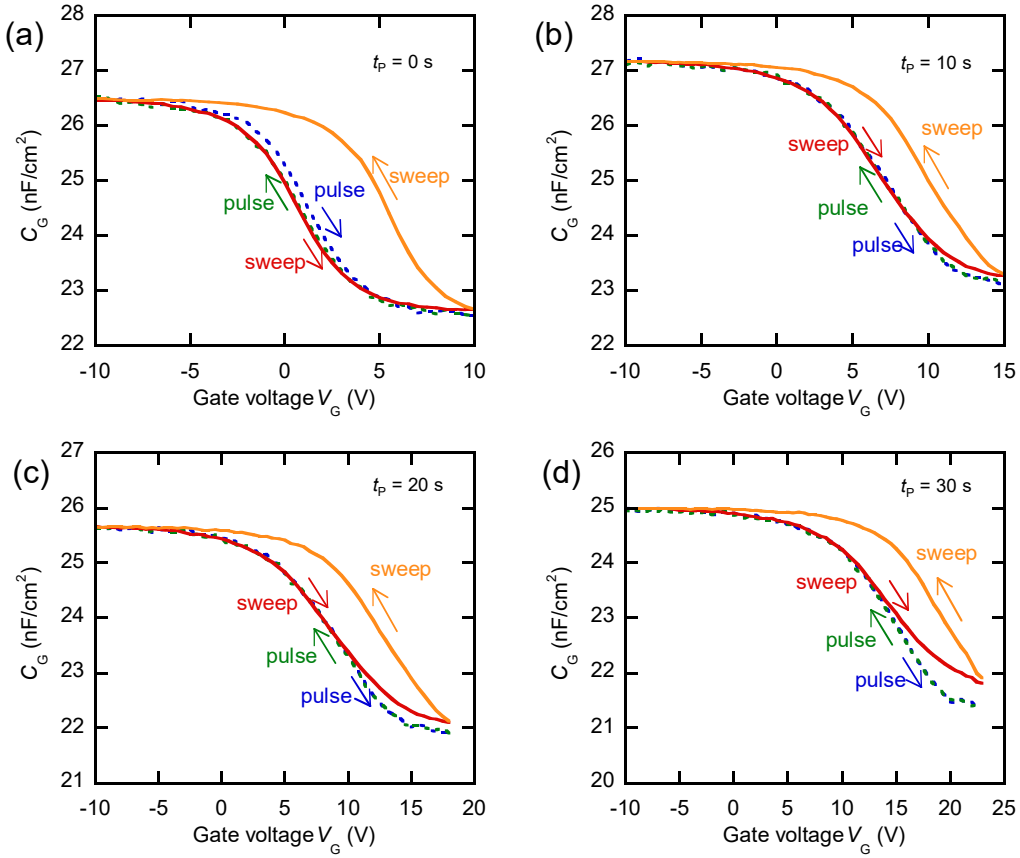

Figure S3. $C_{G,\,pulse}$ versus V_G and $C_{G,\,sweep}$ versus V_G characteristics for pentacene MOS capacitors for t_P = (a) 0 s, (b) 10 s, (c) 20 s, and (d) 30 s.

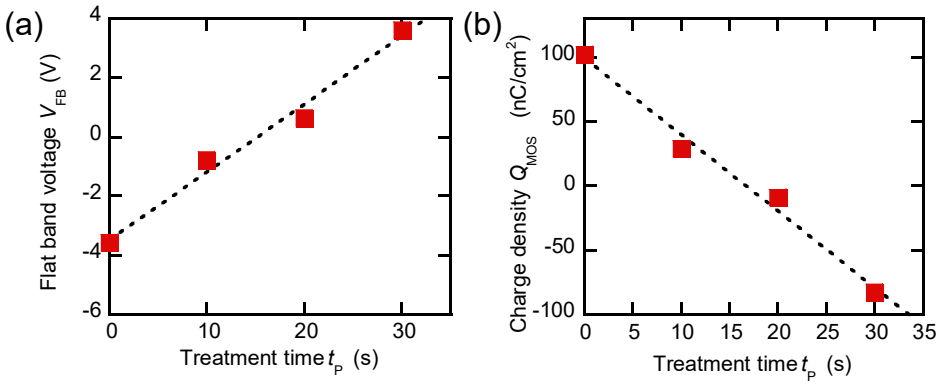

Figure S4. (a) V_{FB} versus t_P determined from C_S shown in Fig. 5(f). (b) Q_{MOS} versus t_P calculated from Eq. (7) and V_{FB} values shown in (a).

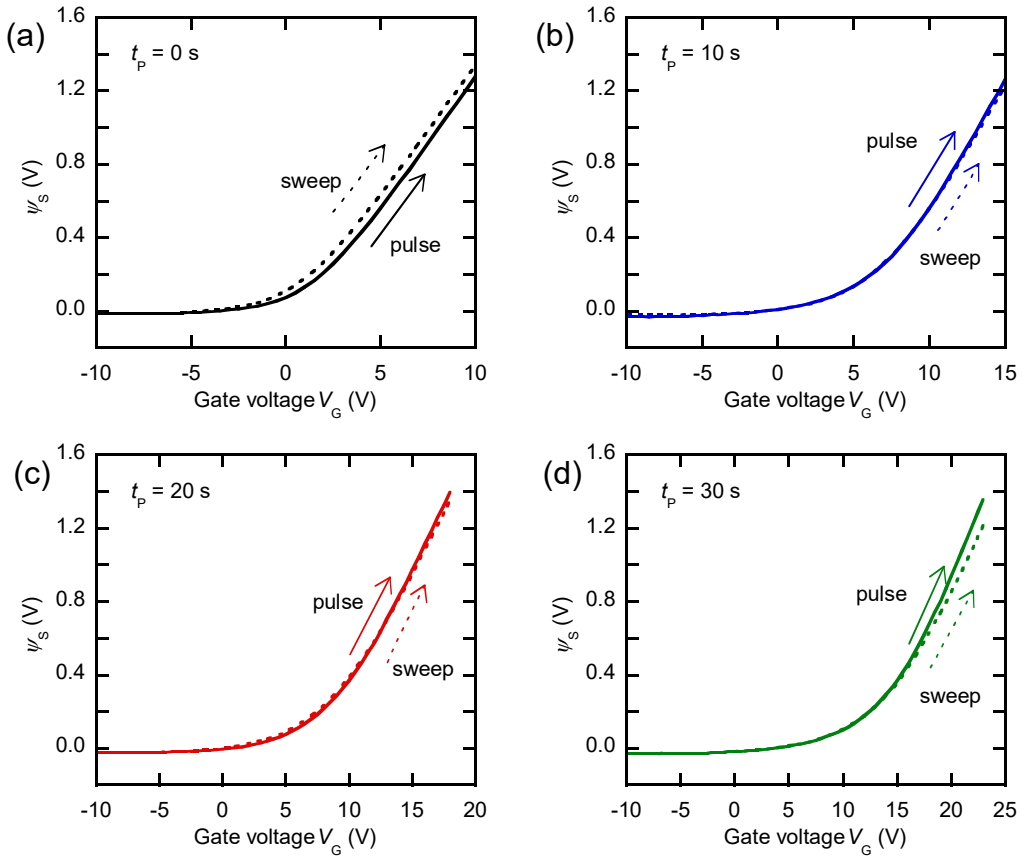

Figure S5. Surface potential Ψ_S calculated from Eq. (9), $C_{G,\,pulse}$, and $C_{G,\,sweep}$ shown in Fig. 7 for t_P = (a) 0 s, (b) 10 s, (c) 20 s, and (d) 30 s.

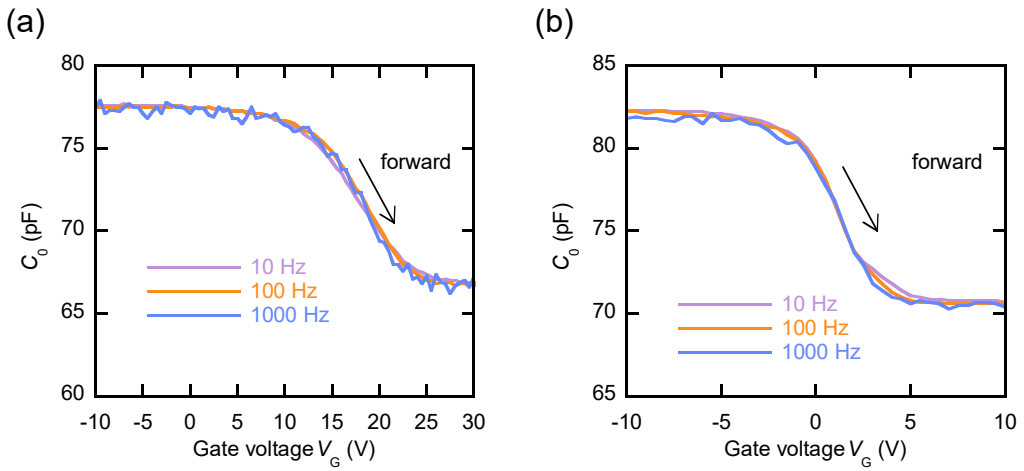

Figure S6. C-V_G characteristics for capacitance (C_0) including the Au/SiO_2/Cr area for t_P = (a) 0 s and (b) 30 s, which were measured at normal sweep that f = 10, 100, and 1000 Hz and t_M =0.8, 0.2, and 0.1 s, respectively.

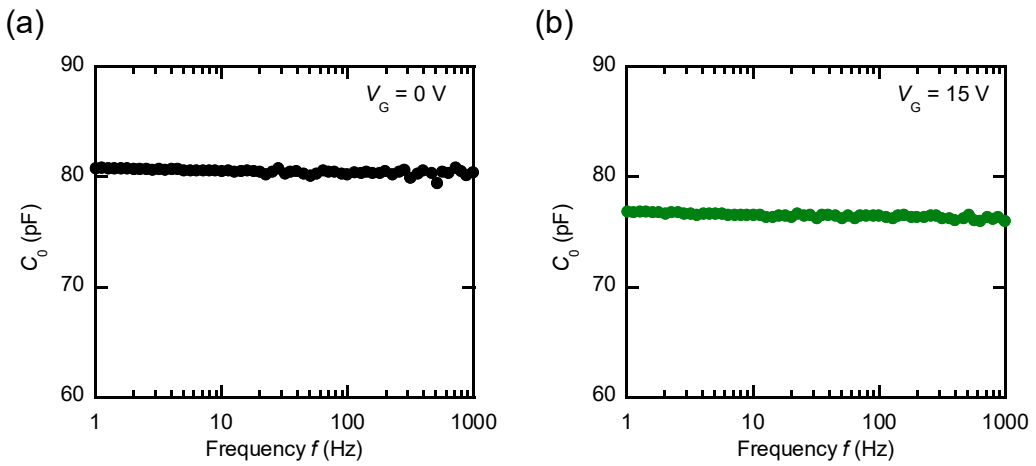

Figure S7. *C-f* characteristics for capacitance (C_0) including the Au/SiO_2/Cr area for t_P = (a) 0 s and (b) 30 s, which were measured at V_G = 0 and 15 V, respectively.