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# A Single-Stage High Frequency-Link Modular Three-Phase $LLC$ AC-DC Converter

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***Abstract*—A new single-stage high frequency-link three-phase $LLC$ ac-dc converter is proposed in this paper. The proposed converter is featured by a boost full-bridge (BFB) topology-based phase module with power factor correction (PFC) for the three-phase utility frequency ac (UFAC) to single-phase high-frequency ac (HFAC) conversion without a smoothed dc link, which brings the simplicity, cost-effectiveness, excellent modularity and high efficiency into the power supply. The soft switching commutation can achieve over the wide range of load power with the assist of magnetizing current of a high frequency transformer in the $LLC$ topology. The load power and voltage can be regulated by pulse frequency modulation (PFM) and phase-shift pulse-width-modulation (PS-PWM) depending on the load conditions. The effectiveness of the proposed converter is investigated by simulation and experiment of a $2\,\mathrm{kW}$-$50\,\mathrm{kHz}$ preliminary prototype, thereby the single-stage frequency conversion, power factor correction (PFC) and zero voltage soft-switching (ZVS) are revealed from a practical point of view.**

***Index Terms*—boost full bridge (BFB), EV battery chargers, high frequency-link, $LLC$ resonant converter, phase modular, pulse frequency modulation (PFM), phase shift pulse-width-modulation (PS-PWM), single-stage frequency conversion, zero voltage soft switching (ZVS), zero current soft switching (ZCS).**

## I. Introduction

THE three-phase ac-dc converter with a high frequency (HF)-link plays a key role in the wide varieties of power supplies; microgrids[1], electric vehicle (EV) rapid battery charger[2][3], solid state transformer (SST) in transportation systems, and telecommunications (Telecom) facilities[4].

The conventional passive rectifier and one switch-boost PFC converter, or a voltage-source pulse-width-modulation (PWM) rectifier are a mature technology with advanced control strategies, however some technical issues still exist; two or multi-stage power conversion processing, bulky reactive components, low modularity and a limited soft switching range of semiconductor power devices, all of which are obstacles to high power density and cost-effectiveness of power supplies[4]-[7].

Anther option is a single-stage / matrix converter rectifier and isolated dc-dc converter, and several types of circuit topology have been proposed for an inductive power transfer, battery charger, and telecom applications[8]-[12]. The three-phase UFAC to single-phase HFAC is directly converted in the front-end power stage with multiple sets of bidirectional switches or reversely blocking /conducting active switches. However, the switching frequency is limited under the several kilo-hertz paying for a complex calculation and modulation strategy of the switching signals. A unique active front-end rectifier-based single-stage three-phase ac-dc converter is proposed in [13] with nine unidirectional switches. This kind of topology may have limitation of modularity for the sake of integration topology of boost three-phase PWM converters and $LLC$ resonant converters.

The alternative solution is a phase modular three-phase ac-dc converter, which consists of three sets of single-phase converters[14]–[24]. The individual control can be applied in each phase module while it may be advantage or disadvantage for the three-phase to single-phase ac-ac power conversion stage depending on the availability of the neutral point of the three-phase voltage sources. In the telecom facilities where three-phase four-wire connection is widely used, the phase modular topology is suitable and effective for the three-phase ac-dc converter owing to the simplicity of controller and flexibility of utility power; three-phase or single-phase system.

All of the previously-developed phase modular three-phase ac-dc converters are comprised of a two- or three-stage power conversion with dc-link. Therefore, a large volume of electrolyte capacitor or dc inductor is indispensable in each phase module, consequently the size and weight of main circuit increase with a short cycle of maintenance. The single-stage isolated ćuk converter-based single-stage three-phase ac-dc converter is proposed in [14]. Although no dc link capacitor is necessary in this topology, the ćuk converter with a single switch suffers from the high voltage stress due to the non-smoothed ac source voltage, which results in the power capacity limitation. The bridge-less PFC converters and two-switch forward converter-based isolated three-phase ac-dc converter is also proposed in [24]. However, the technical concern is the high electro-magnetic noise due to the bridge-less topology where the negative dc-bus line is disconnected with one of the terminals of the high-frequency transformer (HF-X) windings. Thus, the single-switch PWM based phase module topologies still have technical issues such as the large voltage stress and soft switching performances.

Meanwhile, a bridgeless PFC and three-level inverter integrated single-stage isolated three-phase ac-dc converter is proposed in [21], which is suitable especially medium dc voltage applications. However, there is no proposal of the bridgeless PFC and high frequency full-bridge inverter-based single-stage isolated three-phase ac-dc converter suitable for the small and middle power applications by now to the best

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knowledge of the authors.

In order to overcome the drawback of the multi-stage phase modular, a single-stage phase modular three-phase ac-dc converter with HF-link has been proposed in [25]. The proposed converter can attain a single-stage UFAC-HFAC power converter with PFC and without any bulk dc-link capacitor on the basis of phase-shift pulse-width modulation (PS-PWM) with constant switching frequency. Although the circuit topology has novelty and originality, soft switching constraint is severe and its achievable range is small due to non-resonant topology with PS-PWM, which results in the efficiency deterioration especially in the middle to light load conditions.

As a solution for the technical issues of the previously proposed converter in [25], a new single-stage three-phase ac-dc converter is proposed in this paper. Taking over the topological merits of thee-phase ac-dc converter in [25], the newly proposed converter features ; a single-stage UFAC-HFAC power converter with PFC can be achieved on the basis of a $LLC$ multi-resonant boost full bridge (BFB) topology[26]. Accordingly, in addition to PS-PWM, pulse frequency modulation (PFM) can be applied for power control depending on the load voltage condition, which is effective for extending the soft switching range. The $LLC$ converter facilitates voltage boost operation as well as buck while the previous topology is adaptable only for buck operation due to PS-PWM. Accordingly, voltage control is more flexible in the newly-proposed topology than the previous one. There is no need of voltage sensing in the three-phase power sources for achieving PFC in principle, then a cost-effective subsystem can be realized as well as the main circuit. The low frequency and high frequency ripples can be eliminated effectively by the output parallel circuit configuration and $120\,^\circ$ phase shifted pulse patterns of the switching three phase modulars, which facilitates the large chemical capacitor-less topology.

The rest of this paper is organized as follows: The circuit topology and operation principle together with the design consideration of the proposed ac-dc converter are described in Section II. The cancelation and mitigation theory of low and high frequency ripples is explained by mathematical analysis, then power controller scheme is presented in Section III, whereby the high power factor and soft switching conditions are also theoretically clarified. The simulation and experimental results and evaluations are presented in Section IV for revealing the effectiveness of the proposed circuit topology, after which the essential points of the verification are summarized in Section V.

## II. Circuit Topology and Operation Principle

### A. Main Circuit and Control Principle

The main circuit of the proposed three-phase ac-dc power converter is depicted in Fig. 1, where the battery charging application is assumed. Each phase UFAC-HFAC power stage consists of a BFB circuit with a hybrid configuration of diodes $\mathrm{D}_5$, $\mathrm{D}_6$ and reversely conducting active switches $\mathrm{Q}_1$–$\mathrm{Q}_4$. In a phase module, the left-side leg of BFB are driven by $50\,\%$ duty cycle as a fixed phase while the right-side leg are phase shifted with $50\,\%$ duty cycle as a controlled phase. The diodes $\mathrm{D}_5$, $\mathrm{D}_6$ fold the line current ever half cycle of UFAC.

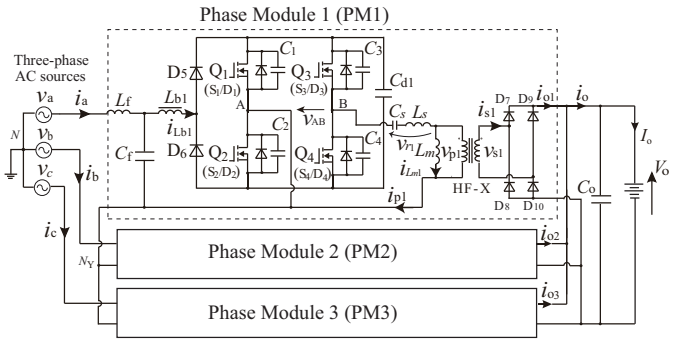


Fig. 1. Proposed high frequency-link three-phase $LLC$ ac-dc converter for battery charging applications.

The resonant capacitor $C_s$ is inserted with the high frequency transformer (HF-X) for attaining the multi resonance with its leakage inductance $L_r$ and magnetizing inductance $L_m$. The UFAC-side inductor currents operate in discontinuous conduction mode (DCM). Accordingly, there is no voltage sensing of the UFAC power sources for achieving PFC, then a cost-effective subsystem can be expected as well as the main circuit. While the peak current is relatively high as compared to continuous conduction mode (CCM), it can be reduced due to the $LLC$ resonant tank as compared to non-resonant converters.

The low side of HF-X primary windings as well as the left-side switching leg middle point $A$ is connected to the neutral point $N_\mathrm{Y}$ of of the three phase modules. Accordingly, the voltage potential of HF-X and the left-side switching leg are stable when the three-phase power source are rigidly balanced, thus electromagnetic noises are relatively small while almost all of the existing isolated three-phase ac-dc converter topologies have floating potentials in the HF inverters.

The switching pulse modulation consists of PFM for boost mode and PS-PWM for buck mode depending on the load conditions. The phase shift (PS) angle $\phi$ between the fixed and controlled phase switches is regulated in accordance with the load conditions in the case of PS-PWM while it is fixed to zero in PFM. The three sets of switching pulse patterns for BFB are shifted by $120^\circ$ each other, thereby high frequency ripples can be alleviated in the output smoothing filter at the dc side.

Key operating waveforms of a utility frequency are indicated in Fig. 2. The three-phase utility currents $i_a$, $i_b$, $i_c$ are respectively converted to the high frequency ac currents $i_{p1}$, $i_{p2}$, $i_{p3}$ through the BFB circuit. The voltages $v_{cd1}$, $v_{cd2}$, $v_{cd3}$ across the voltage-clamping film capacitors $C_{d1}$, $C_{d2}$, $C_{d3}$ comprises the dc load voltage and a double frequency component of the utility frequency. The dc-side current $i_o$ contains the ripple as six-time high as the utility frequency, but it is naturally reduced by the effect of the phase displacement in the three-phase power sources. Accordingly, no large inductive and capacitive smoothing filters are necessary at the output terminal. The three-phase line currents $i_a$, $i_b$, and $i_c$ are controlled in phase with $v_a$, $v_b$, and $v_c$ respectively, thus PFC can attain in the proposed converter. The relevant ac inductor currents $i_{Lb1}$, $i_{Lb2}$, and $i_{Lb3}$ are regulated in DCM, hence no need to detect

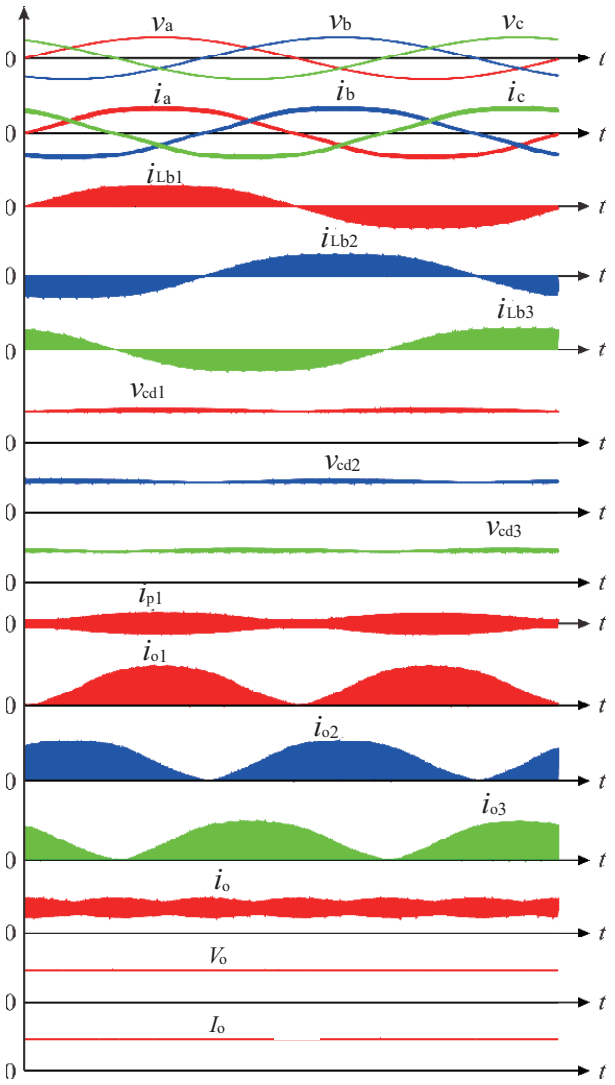


Fig. 2. Key waveforms in a utility frequency cycle.

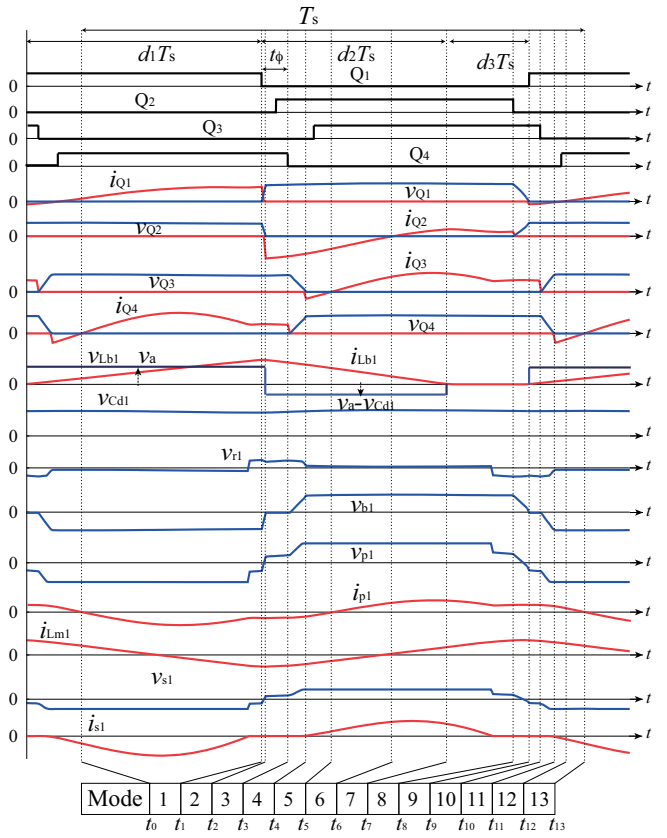


Fig. 3. Relevant voltage and current waveforms of the phase-$a$ BFB in a high frequency switching cycle with $v_a > 0$.

the source voltages; the source voltage sensor-less controller is feasible.

### B. Switching and Mode Transitions

The switching waveforms with the gate-driving signal patterns are illustrated in Fig. 3 under the condition of PS-PWM. The phase-a ac-dc converter only is explained in details for simplicity of discussion. The operations of each half cycle of the source voltages are divided into the thirteen modes, where the symbol $t_\phi$ indicates the time interval defined as $T_\phi = (\phi/360°)T_s$. It should be noted here that Mode 2-4 and Mode 9-11 are combined in the case of PFM as drawn by Mode 2'-4' and Mode 9'-11' respectively. The switch-mode transitions and equivalent circuits per phase are illustrated in Fig. 4(a) and (b) respectively under the condition of PS-PWM. Note herein that the ac line filter $L_f$ and $C_f$ is eliminated for the sake of simplification. The conditions are given as:1) all the active switches and diodes are ideal and no power dissipation exist, 2) the dc voltages of the clamping capacitors are equal as $V_{cd} = V_{cdk,k\in\{1,2,3\}}$ under the condition of the balanced three-phase source voltages and loads.

- Mode 1 [inductive energy storing mode in $L_{b1}$: $t_0 \le t < t_1$] The switches $Q_1$, $Q_4$ keep ON-state, and the input ac power is fed through the closed loop network $v_{in}$-$L_b$-$D_5$-$C_1$; the inductive energy is stored at the ac inductor $L_{b1}$. Meanwhile, the resonant current passes through $S_1$-$L_s$-$C_s$-$S_4$-$C_{d1}$ in the high frequency resonant (HF-R) inverter that is comprised of $S_1$-$L_s$-$C_s$-$S_4$-$C_{d1}$, thereby the capacitive energy is discharged from the clamping film capacitor $C_{d1}$. The secondary-side windings current $i_{s1}$ goes down to zero before the end of this interval due to the resonance in the primary-side inverter.
- Mode 2 [The fixed-phase switches edge resonance: $t_1 \le t < t_2$] The gate signal for $Q_1$ is removed at $t = t_1$; the edge resonance begins with $C_1$, $C_2$ and $L_s$, whereby the current starts commutation naturally from $S_1$ to $C_1$. The charging current of $C_{s1}$ consists of the input ac current $i_{Lb1}$ and the displacement current from $C_{d1}$. The voltage $v_{Q1}$ rises gradually from zero while the voltage $v_{Q2}$ across the low-side switch $Q_2$ decreases gradually from $V_{cd}$ across $C_d$. The primary-side resonant current $i_{p1}$ matches with the magnetizing current $i_{m1}$ at $t = t_1$, then the secondary-side current $i_{s1}$ reduces to zero.
- Mode 3 [$Q_1$ and $Q_2$ ZVS commutation: $t_2 \le t < t_3$] The voltages $v_{Q2}$ across $Q_2$ reaches to zero at $t = t_2$ due to the edge-resonance sustaining from Mode 2, consequently

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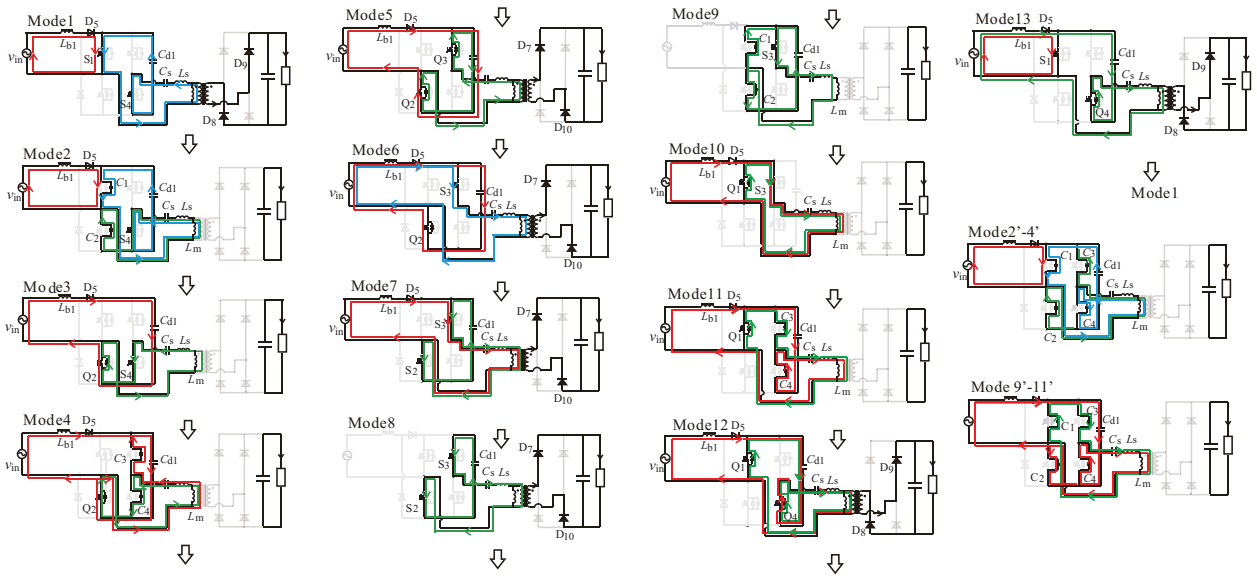



Fig. 4. Mode transitions and equivalent circuits of one phase BFB with PS-PWM in a high-frequency cycle for a positive half cycle $v_{in} > 0$; Mode 2'-4' and Mode 9'-10' for the case of PFM.

$D_2$ is forward biased. Thus, ZVS turn-off is completed in $Q_2$. During this interval, the gate terminal of $Q_2$ is triggered, thereby zero voltage and zero current soft switching (ZVZCS) turn-on is completed in $Q_2$. The primary-side current $i_p$ circulates through $S_4$ and $D_2$ as the magnetizing current $i_{Lm1}$.

- Mode 4 [the controlled-phase switches edge resonance: $t_3 \leq t < t_4$] The gate signal of $S_4$ in $Q_4$ is removed at $t = t_3$, then the edge resonance begins with $C_3$, $C_4$ and $L_s$ in the HF-R inverter while the current starts commutation naturally from $S_4$ to $C_4$. Consequently, the voltage $v_{Q4}$ rises gradually from zero while the voltage $v_{Q3}$ across the high-side switch $Q_3$ decreases gradually from $V_{cd}$. Thus, ZVS commutation is initiated by the magnetizing current $i_{Lm1}$.
- Mode 5 [$Q_4$ and $Q_3$ ZVS commutation: $t_4 \leq t < t_5$] The voltage $v_{Q4}$ across $Q_4$ reaches to $V_{cd}$ at $t = t_4$ due to the edge-resonance sustaining from Mode 4, consequently $D_3$ is forward biased. Thus, ZVS turn-off is completed in $Q_4$. During this interval, the gate terminal of $Q_3$ is triggered, thereby ZVZCS turn-on attains in $Q_3$. The primary-side current $i_{p1}$ changes its polarity during this interval, then the rectifying diodes $D_7$ and $D_{10}$ start conduction.
- Mode 6 [ac power fed to secondary side: $t_5 \leq t < t_6$] The primary-side current $i_{p1}$ changes its polarity naturally, then $i_{Lb1}$ is fed to the secondary side by passing through the network $Q_3$-$C_s$-$L_r$-HF-X and $C_{d1}$-$Q_2$ while $C_{d1}$ is charged by $i_{Lb1}$. The magnetizing current $i_{Lm1}$ is lagging to $i_{p1}$ and its polarity changes ahead of $t = t_6$. The secondary-side current $i_{s1}$ rises gradually from zero in the reverse polarity, then $D_7$ and $D_{10}$ are forward biased.
- Mode 7 [power fed from $L_{b1}$ and $C_d$: $t_6 \leq t < t_7$] The primary-side current $i_{p1}$ exceeds over the inductor current $i_{Lb1}$ at $t = t_6$, then $C_{d1}$ begins to discharge. Thus, the load power is supplied from both the released inductive energy $L_{b1}$ and the discharged capacitive energy from $C_d$.
- Mode 8 [$L_{b1}$ discontinuous conduction: $t_7 \leq t < t_8$] The ac inductor current $i_{Lb1}$ declines to zero, then the load power is supplied only from $C_d$. The secondary-side current $i_{s1}$ also declines to zero during this interval. Accordingly, the ac power source is disconnected from the BFB circuit.
- Mode 9 [the fixed-phase switches edge resonance: $t_8 \leq t < t_9$] The gate signal $S_2$ is removed at $t = t_8$, and the voltage $v_{Q2}$ increases from zero while the voltage across $v_{Q1}$ declines from the clamping voltage $V_{cd1}$. Accordingly, ZVS turn-off completes by the end of this interval. The charging and discharging currents in $C_2$ and $C_1$ are fed from the magnetizing current $i_{p1}$, a part of which is discharged from the clamping film capacitor $C_d$.
- Mode 10 [$Q_2$ and $Q_1$ ZVS commutation: $t_9 \leq t < t_{10}$] The voltage $v_{Q2}$ across $Q_2$ reaches up to $v_{cd}$ at $t = t_9$ while the voltage $v_{Q1}$ across $Q_1$ declines to zero. Thereby, ZVS turn-off attains in $Q_2$. During this interval, the ac inductor current begins to increase linearly from zero.
- Mode 11 [Fixed-phase leg edge resonance :$t_{10} \leq t < t_{11}$] The gate signal of $S_3$ in $Q_3$ is removed at $t = t_{10}$, whereby the voltage $v_{Q3}$ increases linearly from zero. At the same time, the voltage $v_{Q4}$ across $Q_4$ declines from the peak value of $v_{cd}$.
- Mode 12 [$Q_3$ and $Q_4$ ZVS commutation: $t_{11} \leq t < t_{12}$] The voltage $v_{Q3}$ reaches the clamping voltage $V_{cd}$ at $t = t_{11}$, whereby ZVS turn-off achieves in $Q_3$. The voltage $v_{Q4}$ across $Q_4$ declines to zero at $t = t_{11}$ after which the gate signal is applied to $S_4$. Accordingly, ZVZCS turn-on achieves in $Q_4$.
- Mode 13 [$i_{Q1}$ reverses polary $t_{12} \leq t < t_{13}$] The current through $Q_1$ starts commutation naturally from $D_1$ to $S_1$,

thereby the inductor current $i_{Lb1}$ is shared by $\mathrm{S}_1$ and $C_{d1}$. The magnetizing current $i_{Lm1}$ is greater than $i_{p1}$ during this interval, then the diode $\mathrm{D}_4$ in $\mathrm{Q}_4$ keeps conducting up to $t = t_{13}$. The amplitude of $i_{p1}$ exceeds over that of $i_{p1}$ at $t = t_{13}$, then the circuit operation return to Mode 1.

### C. Design Consideration

*1) AC Inductors:* The one switching cycle of $i_{Lb} = i_{Lbk,k\in\{1,2,3\}}$ is divided into the three terms where $d_1T_s$, $d_2T_s$ and $d_3T_s$ correspond with the linearly increasing, linearly decreasing and zero level respectively as portrayed in Fig. 3. The three intervals are schematically redrawn with the line current $i_a(=\sqrt{2}M_iI_s\sin\omega_u t)$, ac inductor current $i_{Lb}$ and its peak peak value $i_{Lb,pp}$ in Fig. 5. The time integral of the voltage $v_{Lb} = v_{Lbk}$ across $L_b = L_{bk}$ over the one switching cycle is ideally zero as expressed by

$$\int_0^{T_s} v_{Lb}dt = \{d_1v_a + d_2(v_a - V_{cd}) + d_3\cdot 0\} = 0. \quad (1)$$

The relationship between $d_1$ and $d_2$ can be derived from the foregoing equation as

$$d_2 = \frac{|v_a|}{V_{cd} - |v_a|}\cdot d_1 = \frac{|\sqrt{2}V_s\sin\omega_u t|d_1}{V_{cd} - |\sqrt{2}V_s\sin\omega_u t|} \quad (2)$$

where $V_s$ is the RMS of the source voltage $v_a$ and $\omega_u$ represents the angular utility frequency. Eq.(2) indicates $V_{cd}$ should be larger than the peak value of the source voltage ($\sqrt{2}V_s$) ; the boost PFC should be achievable regardless of $d_1$. In order to keep the DCM in $i_{Lb}$ under the condition $d_1 = 0.5$, $d_2$ should be less than $0.5$. Accordingly, the clamping film capacitor voltage $V_{cd}$ should satisfy the condition which is derived from (2) as $V_{cd} > 2\sqrt{2}V_s$. Fig. 6 illustrates the available range of $d_2$ versus the phase angle of $v_a$ with the parameters of $V_{cd}$. In order to keep DCM in $i_{Lb}$ through the whole UFAC cycle of $v_a$, $V_{cd}$ should be regulated over $565\,\mathrm{V}$.

The ac inductor $L_b$ is expressed by dealing with its inductive energy releasing interval $d_2T_s$ as

$$L_b = \frac{(V_{cd} - |v_a|)d_2T_s}{i_{Lb,pp}}. \quad (3)$$

The relation between $i_a$ and $i_{Lb,pp}$ can be expressed mathematically from Fig. 5 as

$$i_{Lb,pp}(t) = |\sqrt{2}M_iI_s\sin\omega_u t| \quad (4)$$

where $M_i$ represents the ac current ratio to $i_a$. As a result, the ac inductor $L_b$ can be decided from (2), (3) and (4) as

$$L_b = \frac{|\sqrt{2}V_s\sin\omega_u t|\cdot d_1}{|\sqrt{2}M_iI_s\sin\omega_u t|\cdot f_s} = \frac{V_sd_1}{M_iI_sf_s} = \frac{{V_s}^2d_1}{P_aM_if_s} \quad (5)$$

where $P_a$ denotes the power capacity (in apparatus power) per phase.

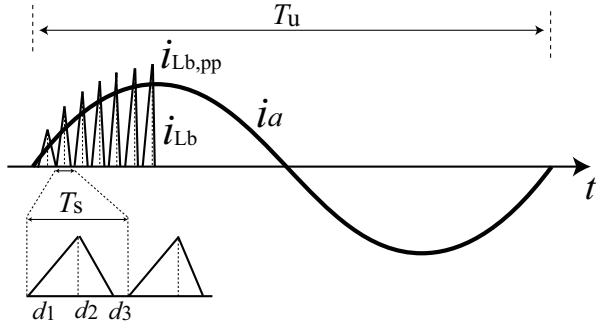



Fig. 5. Inductor current $i_{Lb}$ and the source current $i_s$ under DCM.

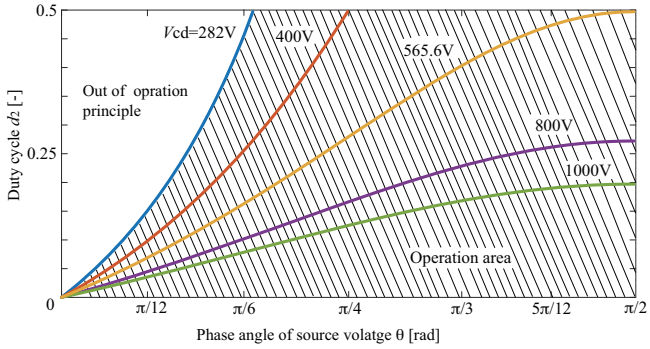



Fig. 6. Available range of the duty factor $d_2$ for DCM.

*2) Magnetizing Inductance in HF-X:* The magnetizing inductance $L_m = L_{mk,k\in\{1,2,3\}}$ of the HF-X can be designed by approximating the magnetizing current $i_{Lm}$ in linear, which can be written as

$$i_{Lm}(t) = \frac{aV_o}{L_m}\cdot t - i_{Lm,pp}, \quad t\in\left[0, T_s/2\right] \quad (6)$$

where $i_{Lm,pp}$ denotes the peak value of $i_{Lm}$ and $a = N_p/N_s$ represents the windings turns ratio of HF-X. Since $i_{Lm}(T_s/2) = i_{Lm,pp}$ is established, the magnetizing inductance $L_m$ can be determined by

$$L_m = \frac{aV_o}{4i_{Lm,pp}f_s}. \quad (7)$$

*3) Series Resonant Inductor and Capacitor:* The first resonant frequency $f_\mathrm{r}$ and the second resonant frequency $f_m$ of the $LLC$ converter are defined as

$$f_r = \frac{1}{2\pi\sqrt{L_sC_s}}, \quad f_m = \frac{1}{2\pi\sqrt{(L_s + L_m)C_s}}. \quad (8)$$

Since a frequency ration $\lambda = f_r/f_m$ is preferably set less than 5 from the practical point of view, $L_s$ can be decided from (8) as

$$L_s = \frac{L_m}{\lambda^2 - 1}. \quad (9)$$

Subsequently, the series resonant capacitor $C_s$ can be determined by (8) and (9).

*4) Voltage-Clamping Film Capacitor:* The third interval $d_3T_s$ includes Mode 8 and Mode 9 where ZVS commutation from $Q_2$ to $Q_1$ accomplishes. Accordingly, in addition to Mode 7 where the discharged current $i_{cd} = i_{cdk,k\in\{1,2.3\}}$ from $C_{dk}$ assists $i_{Lbk}$, $d_3T_s\,(= t_9 - t_7)$ should guarantee the net change of capacitive charge in $C_d = C_{dk}$ as expressed by

$$\Delta Q_{cd} = C_d \zeta V_{cd} > \int_{t_7}^{t_9} i_{cd} dt \tag{10}$$

where $\zeta = \Delta v_{cd}/V_{cd}$ represents a voltage ripple ratio in $C_d$. Since $i_{cd}$ consists of only the HFAC component as illustrated in Fig. 4, the voltage-clamping film capacitor $C_d$ can be small enough to compensate the HFAC current and satisfy (10) with the given $\zeta$.

## III. Elimination of Double Utility Frequency and High Frequency Components

### A. Input and Output Power Analysis

The instantaneous powers relevant to UFAC are defined in phase-a, -b, and -c, respectively under the conditions of unity power factor as

$$\begin{aligned} p_a(t) &= \sqrt{2}V_s \sin\omega_u t \cdot \sqrt{2} I_s \sin\omega_u t \\ &= V_s I_s (1 - \cos 2\omega t) \\ p_b(t) &= \sqrt{2}V_s \sin\big(\omega_u t - 2\pi/3\big) \cdot \sqrt{2} I_s \sin\big(\omega_u t - 2\pi/3\big) \\ &= V_s I_s \big\{1 - \cos(\omega_u t - 2\pi/3)\big\} \\ p_c(t) &= \sqrt{2}V_s \sin\big(\omega_u t - 4\pi/3\big) \cdot \sqrt{2} I_s \sin\big(\omega_u t - 4\pi/3\big) \\ &= V_s I_s \big\{1 - \cos(\omega_u t - 4\pi/3)\big\}. \end{aligned} \tag{11}$$

The BFB circuit includes the double frequency $2\omega_u$ as appears in the ac inductor currents $i_{Lb1}$, $i_{Lb2}$, $i_{Lb3}$. Accordingly, the instantaneous currents $i_{o1}$, $i_{o2}$, $i_{o3}$ of the secondary-side rectifiers are expressed

$$\begin{aligned} i_{o1}(t) &= \frac{V_s I_s}{V_o}\big(1 - \cos 2\omega_u t\big) + i_{h,a}(t) \\ i_{o2}(t) &= \frac{V_s I_s}{V_o}\big\{1 - \cos 2(\omega_u t - 2\pi/3)\big\} + i_{h.b}(t) \\ i_{o2}(t) &= \frac{V_s I_s}{V_o}\big\{1 - \cos 2(\omega_u t - 4\pi/3)\big\} + i_{h,c}(t) \end{aligned} \tag{12}$$

where the UFAC-enveloped HFAC fluctuations are defined with the angular switching frequency $\omega_s\,(= 2\pi f_s)$ as

$$\begin{aligned} i_{h,a}(t) &= f(2\omega_u t, \omega_s t) \\ i_{h,b}(t) &= f(2\omega_u t - 2\pi/3, \omega_s t - 2\pi/3) \\ i_{h,c}(t) &= f(2\omega_u t - 4\pi/3, \omega_s t - 4\pi/3). \end{aligned} \tag{13}$$

As a result, the output current $i_o$ that is the sum of $i_{o1}$, $i_{o2}$ and $i_{o3}$ is ideally expressed by referring to equation sets of (12) and (13) as

$$i_o(t) = \sum_{k=1}^{3} i_{ok} = \frac{3V_s I_s}{V_o} + i_{h,a} + i_{h,b} + i_{f,c}. \tag{14}$$

It can be known from (12)-(14) that the double utility frequency components are ideally cancelled out at the output filter $C_o$. Thus, there is no need to implement a large capacitor at the output smoothing filter. Although the mixed components of HFAC remain in $i_o$, it can be eliminated by a small capacitive filter $C_o$, thereby the smoothed dc current $I_o$ can be obtained as portrayed in Fig. 2.

The instantaneous voltage $v_{cd1}$, $v_{cd2}$, $v_{cd3}$ across the clamping film capacitors are expressed as

$$\begin{aligned} v_{cd1}(t) &= V_{cd1} + \tilde{v}_{cd1} \\ v_{cd2}(t) &= V_{cd2} + \tilde{v}_{cd2} \\ v_{cd3}(t) &= V_{cd3} + \tilde{v}_{cd3} \end{aligned} \tag{15}$$

where the ac components are written in the double frequency with the RMS value $V_p$ as

$$\begin{aligned} \tilde{v}_{cd1}(t) &= \sqrt{2}V_p \sin(2\omega_u t) \\ \tilde{v}_{cd2}(t) &= \sqrt{2}V_p \sin(2\omega_u t - 2\pi/3) \\ \tilde{v}_{cd3}(t) &= \sqrt{2}V_p \sin(2\omega_u t - 4\pi/3). \end{aligned} \tag{16}$$

The average values for one switching cycle $T_s\,(= {f_s}^{-1})$ are calculated as

$$\begin{aligned} < v_{cd1} >_{T_s} &= \frac{1}{T_s}\int_0^{T_s} (V_{cd1} + \tilde{v}_{cd1}) dt \simeq V_{cd1} \\ < v_{cd2} >_{T_s} &= \frac{1}{T_s}\int_{T_s/3}^{4T_s/3} (V_{cd2} + \tilde{v}_{cd2}) dt \simeq V_{cd2} \\ < v_{cd3} >_{T_s} &= \frac{1}{T_s}\int_{2T_s/3}^{5T_s/3} (V_{cd3} + \tilde{v}_{cd3}) dt \simeq V_{cd3} \end{aligned} \tag{17}$$

where $\omega_s$ is much higher than $\omega_u$. The three clamping capacitor voltages may not be identical when the source voltages $v_a$, $v_b$, $v_c$ or the three-phase load impedances are unbalanced. In the case, the duty cycle $d_1$ should be controlled individually in each phase BFB.

### B. Hybrid Switching Pulse Modulations

The single-phase BFB circuit is analyzed by a simplified equivalent circuit as well as the conventional $LLC$ converter. The bridge-leg voltage $v_{AB}$ in Fig. 1 appears as the two-level rectangular voltage with the amplitude of $\pm V_{cd}$ since the PS angle is zero under the condition of PFM. In the case of PS-PWM, $v_{AB}$ appears as the three-level rectangular waveform. By adopting the Fourier Series, RMS value $V_{AB,1}$ of $v_{AB}$ is ideally expressed on the basis on the pulse modulations as

$$V_{AB,1} = \begin{cases} \frac{2\sqrt{2}V_{cd}}{\pi} & \text{(in PFM)} \\ \frac{2\sqrt{2}V_{cd}}{\pi}\cos\left(\frac{\phi_s}{2}\right) & \text{(in PS-PWM)} \end{cases} \tag{18}$$

The ac equivalent circuit is expressed of the rectifier, output filter and dc load by the first-harmonics approximation (FHA) as in Fig. 7, where the ac resistance $R_{ac}$ is expressed as $R_{ac} = 8a^2R_o\,/\,\pi^2$. The HF-X primary current $i_{p1}$ deviates from the sine waveforms in accordance with the expansion of PS angle. Therefore, the voltage gain $M_v = V_{\rm o}/V_{\rm cd}$ can be denoted in the single-phase unit of $LLC$ converter as

$$M_v = \frac{V_{\rm o}}{V_{\rm cd}} = \frac{1}{a\sqrt{\left(1 + \frac{1}{S} - \frac{1}{SF^2}\right)^2 + Q^2\left(F - \frac{1}{F}\right)^2}} \tag{19}$$

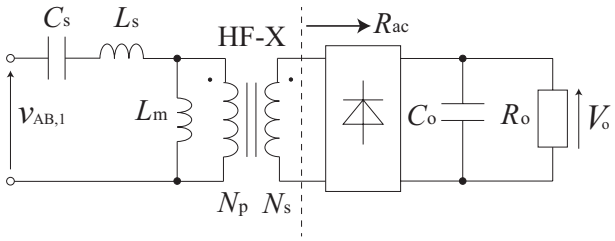



Fig. 7. Simplified equivalent circuit of one phase topology for the FHA analysis.

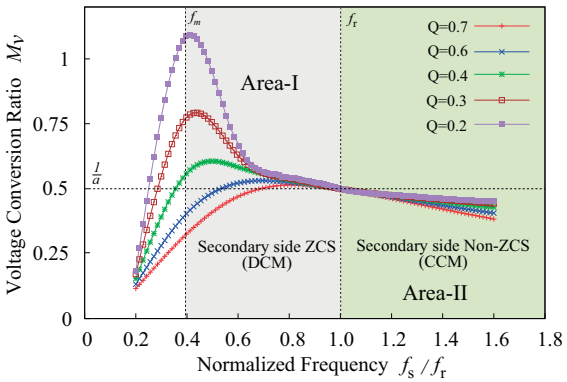



Fig. 8. Theoretical characteristics of the voltage conversion ratio versus switching frequency: $f_{\rm m} = 18\,{\rm kHz}$, $f_{\rm r} = 50\,{\rm kHz}$, $S = 200\,\mu{\rm H}\,/\,30\,\mu{\rm H} \simeq 6.7$, and $a = 2$.

where the resonant characteristics impedance $Z_{\rm r} = \sqrt{L_{\rm s}/C_{\rm s}}$, the inductors ratio $S = L_m/L_s$, the normalized frequency $F = f_s\,/\,f_r$, and the load quality factor $Q = Z_{\rm r}\,/\,R_{\rm ac}$ are defined respectively.

The theoretical curves of the voltage gain versus normalized frequency are depicted in Fig. 8 for the single-phase unit of $LLC$ converter. In the frequency area between $f_m$ and $f_r$ (named as "Area-I"), ZVS and ZCS operations can attain in the primary and secondary-side switches respectively. In the area greater than $f_r$ (named as "Area-II"), only ZVS can attain in the primary-side switches while non-ZCS occurs in the secondary-side rectifier due to CCM operation. Accordingly, the pulse modulation changes from PFM to PS-PWM before $f_s$ reaches $f_r$ in order to maintain ZVS in the primary side and ZCS in the secondary side, respectively. The hybrid power control strategy of PFM and PS-PWM works effectively in the constant current and constant voltage (CCCV) profile of a battery charging scenario as depicted in Fig. 9; PFM is applicable for CC and CV while PS-PWM for the area of a low current in CV.

The hybrid power controller is schematically illustrated in Fig. 10. The output voltage and current closed loop controllers provide the command value for the PFM and PS-PWM schemes. The gate signals are decided for the active switches in Phase-a, then are sequentially phase shifted by 120 ° for the remaining Phase-b and -c.

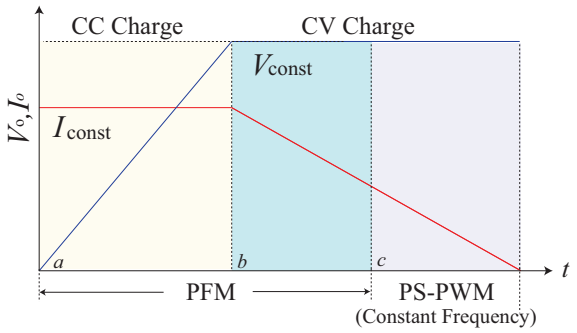



Fig. 9. Typical voltage and current profile of CCCV battery charger.

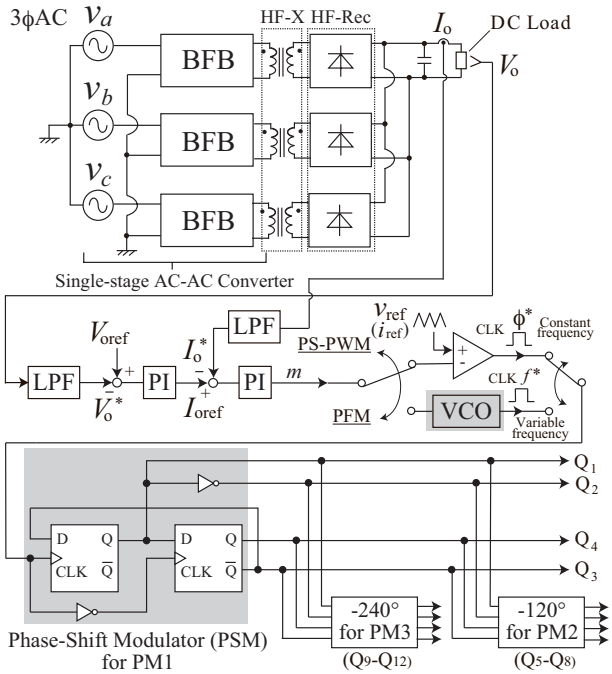



Fig. 10. Closed loop power controller in proposed ac-dc converter.

### C. Zero Voltage Soft Switching Conditions

All the active switches $Q_1$-$Q_4$ can commutate completely by ZVS with the magnetizing current $i_{Lm}$ in the case of PFM. In contrast to that, ZVS conditions should be considered individually in the case of PS-PWM due to the circulating current between the fixed and lagging-phase legs. Fig. 11 displays the simplified equivalent circuits for the turn-on and off transitions of $Q_1$-$Q_4$ in the case of PS-PWM. ZVS turn-off of $Q_1$ in the fixed-phase leg is assisted by both the HF-X primary current $i_{p1}$ and the input ac inductor current $i_{Lb1}$ as shown in Fig. 11(a). The other commutation process is carried out by $i_{p1}$ as portrayed in Fig.11 (b)-(d). Note here that the HF-X primary winding current $i_{p1}$ is identical with the magnetizing current $i_{Lm1}$ since the secondary-side current $i_{s1}$ is zero in each ZVS commutation interval.

In contrast to non-resonant power converters such as dual active bridge converters, the currents in the $LLC$ resonant

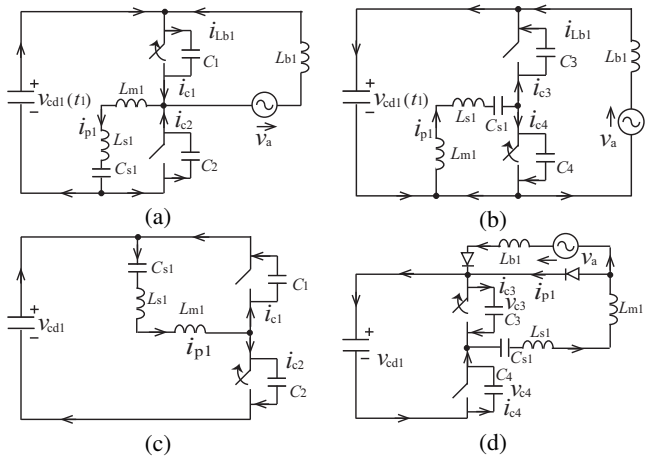



Fig. 11. Simplified equivalent circuits for the switching transitions with PS-PWM: (a) ZVS turn-off of $Q_1$ and ZVS turn-on of $Q_2$ in Mode 2, (b) ZVS turn-off of $Q_4$ and ZVS turn-on of $Q_3$ in Mode 4, (c) ZVS turn-off of $Q_2$ and ZVS turn-on of $Q_1$ in Mode 9, and (d) ZVS turn-off of $Q_3$ and ZVS turn-on of $Q_4$ in Mode 11.

converter cannot be expressed by a time domain manner. Therefore, ZVS conditions are expressed in terms of inductive and capacitive energies as discussed below.

*1) ZVS Commutation from* $Q_1$ *to* $Q_2$*:* ZVS commutation from $Q_1$ to $Q_2$ is expressed as

$$t_{zvs,Q_1\to Q_2} = \frac{C_1 V_{cd}}{\Delta i_{c1\oplus}} = \frac{C_2 V_{cd}}{\Delta i_{c2\ominus}} < t_2 - t_1 \quad (20)$$

$$i_{C1\oplus}(t) = i_{Lb1}(t) + i_{cd\ominus}(t) \quad (21)$$

$$i_{c2\ominus}(t) = i_{p1}(t) - i_{cd\ominus}(t) \quad (22)$$

where the symbols $\oplus$,$\ominus$ represent the charging and discharging actions of capacitors. The net change of charging and discharging currents in the lossless snubber capacitors are expressed as

$$\frac{\Delta i_{c1\oplus}}{\Delta i_{c2\ominus}} = \frac{C_1}{C_2}. \quad (23)$$

When the lossless snubber capacitors $C_1$, $C_2$ have the same capacitance, the charging and discharging currents are equally shared by the HF-X primary winding current $i_{p1}$ and the input ac inductor current $i_{Lb1}$. The ZVS condition can be defined inters of inductive and capacitive energy as

$$\frac{1}{2}\Big[(L_s + L_m) i_{p1}(t)^2 + L_{b1} i_{Lb1}(t)^2\Big] > \frac{(C_1 + C_2) V_{cd}^2}{2}$$

*2) ZVS Commutation from* $Q_4$ *to* $Q_3$*:* ZVS commutation from $Q_4$ to $Q_3$ is expressed as

$$t_{zvs,Q_4\to Q_3} = \frac{C_4 V_{cd}}{\Delta i_{c4\oplus}} = \frac{C_3 V_{cd}}{\Delta i_{c3\ominus}} < t_4 - t_3 \quad (24)$$

$$i_{c4\oplus}(t) = i_{p1}(t) + i_{Lb}(t) - i_{cd\oplus}(t) \quad (25)$$

$$i_{c3\ominus}(t) = i_{cd\oplus}(t) - i_{Lb1}(t). \quad (26)$$

The net change of charging and discharging currents of the lossless snubber capacitors $C_3$, $C_4$ are expressed as

$$\frac{\Delta i_{c4\oplus}}{\Delta i_{c3\ominus}} = \frac{C_4}{C_3}. \quad (27)$$

Combining (25) and (26) results in

$$i_{p1}(t) = i_{Lm1}(t) = i_{c4\oplus}(t) + i_{c3\ominus}(t). \quad (28)$$

When $C_4$ and $C_3$ are identical, $i_{c4\oplus}$ and $i_{c3\ominus}$ are equally distributed from $i_{p1}$. The ZVS condition can be defined in terms of inductive and capacitive energy as

$$\frac{1}{2}\Big[(L_s + L_m) i_{p1}(t)^2\Big] > \frac{(C_3 + C_4) V_{cd}^2}{2}. \quad (29)$$

*3) ZVS Commutation from* $Q_2$ *to* $Q_1$*:* ZVS commutation from $Q_2$ to $Q_1$ for the time interval $t \in [t_8, t_9]$ is expressed as

$$t_{zvs,Q_2\to Q_1} = \frac{C_2 V_{cd}}{\Delta i_{c2\oplus}} = \frac{C_1 V_{cd}}{\Delta i_{c1\ominus}} < t_9 - t_8 \quad (30)$$

$$i_{p1}(t) = i_{Lm1}(t) = i_{c2\oplus}(t) + i_{c1\ominus}(t). \quad (31)$$

Since $C_1$ and $C_2$ are identical, the charging and discharging currents are equally shared by the HF-X primary winding current $i_{p1}$. The ZVS condition can be defined in terms of inductive and capacitive energy as

$$\frac{1}{2}\Big[(L_s + L_m) i_{p1}(t)^2\Big] > \frac{(C_1 + C_2) V_{cd}^2}{2}. \quad (32)$$

*4) ZVS Commutation from* $Q_3$ *to* $Q_4$*:* ZVS commutation from $Q_3$ to $Q_4$ for the interval $t \in [t_{10}, t_{11}]$ is denoted as

$$t_{zvs,Q_3\to Q_4} = \frac{C_3 v_{c3}(t)}{\Delta i_{c3\oplus}} = \frac{C_4 v_{c4}(t)}{\Delta i_{c4\ominus}} < t_{11} - t_{10} \quad (33)$$

$$i_{c3\oplus}(t) = i_{p1}(t) - i_{cd\oplus}(t) \quad (34)$$

$$i_{c4\ominus}(t) = i_{cd\oplus}(t). \quad (35)$$

Combing (34) and (35) leads to

$$i_{p1}(t) = i_{c3\oplus}(t) + i_{c4\ominus}(t). \quad (36)$$

Thus, the net change of charging and discharging currents $\Delta i_{c3}$, $\Delta i_{c4}$ are equally distributed by $i_{p1}$. The ZVS condition can be defined in terms of inductive and capacitive energy as

$$\frac{1}{2}\Big[(L_s + L_m) i_{p1}(t)^2\Big] > \frac{(C_3 + C_4) V_{cd}^2}{2}. \quad (37)$$

## IV. Simulation and Experimental Verifications

### A. Simulation Results

The circuit operations are analyzed in simulations by emulating the CCCV battery charging scenario.

The simulated waveforms for the PFM-based CC and CV modes are depicted in Fig. 12. It can be confirmed hereby that ZVS commutations attain in all the switches under the principle of $LLC$ converter, which implies the low switching losses and noises can be ensured. The simulated waveforms of the PS-PWM-based CV mode are displayed in Fig. 13. The fixed and controlled phase switches perform ZVS at the small PS angle for CV mode. However, the incomplete ZVS which is identified with the residual voltage at the turn-off transitions appears in the controlled phase switches $Q_3$ and $Q_4$ with the large PS angle condition for CV mode. Meanwhile, the diodes in the rectifiers can maintain ZCS regardless of pulse modulations owing to the effect of $LLC$ resonant converter.

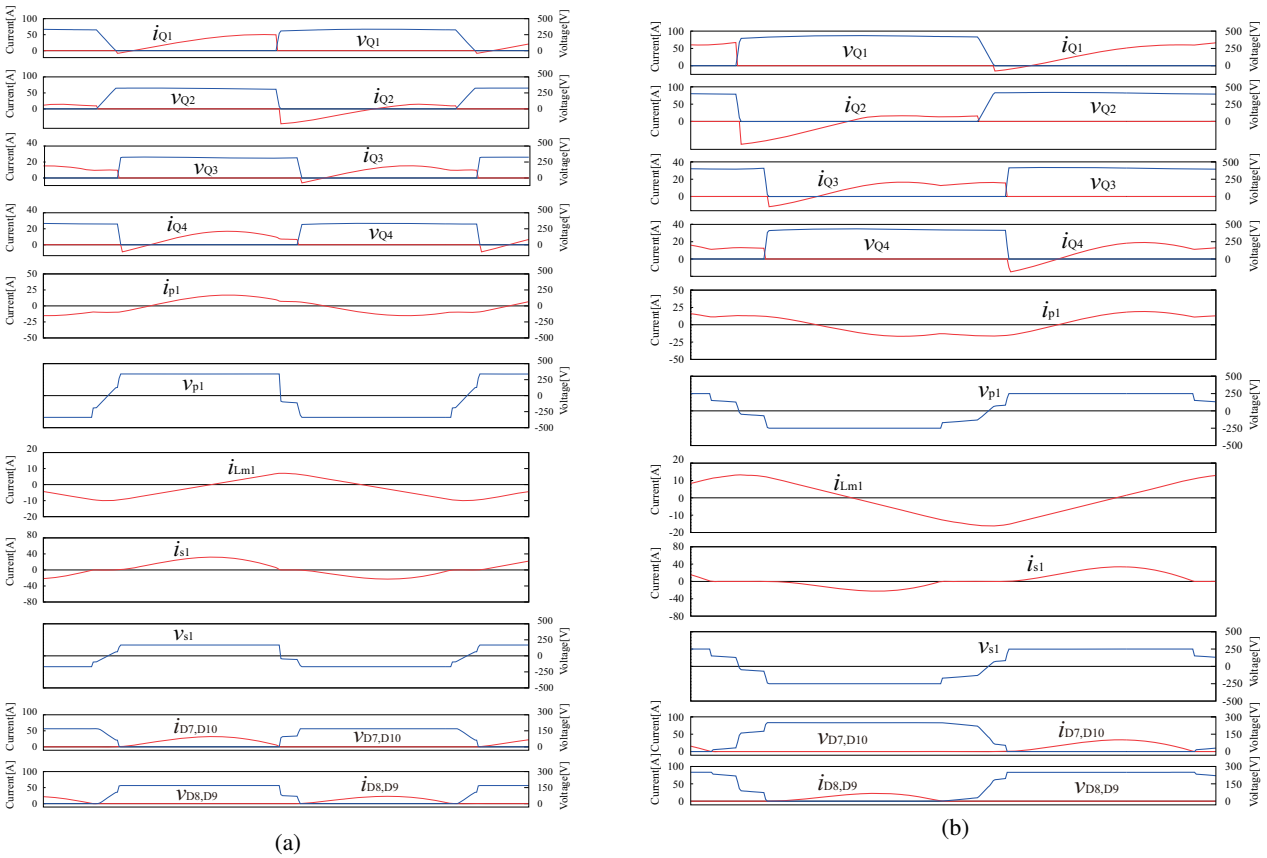



Fig. 12. Simulation waveforms of the switching performances with PFM: (a) CC mode for $I_o = 25\,\mathrm{A}$, and (b) CV mode for $V_o = 400\,\mathrm{V}$.

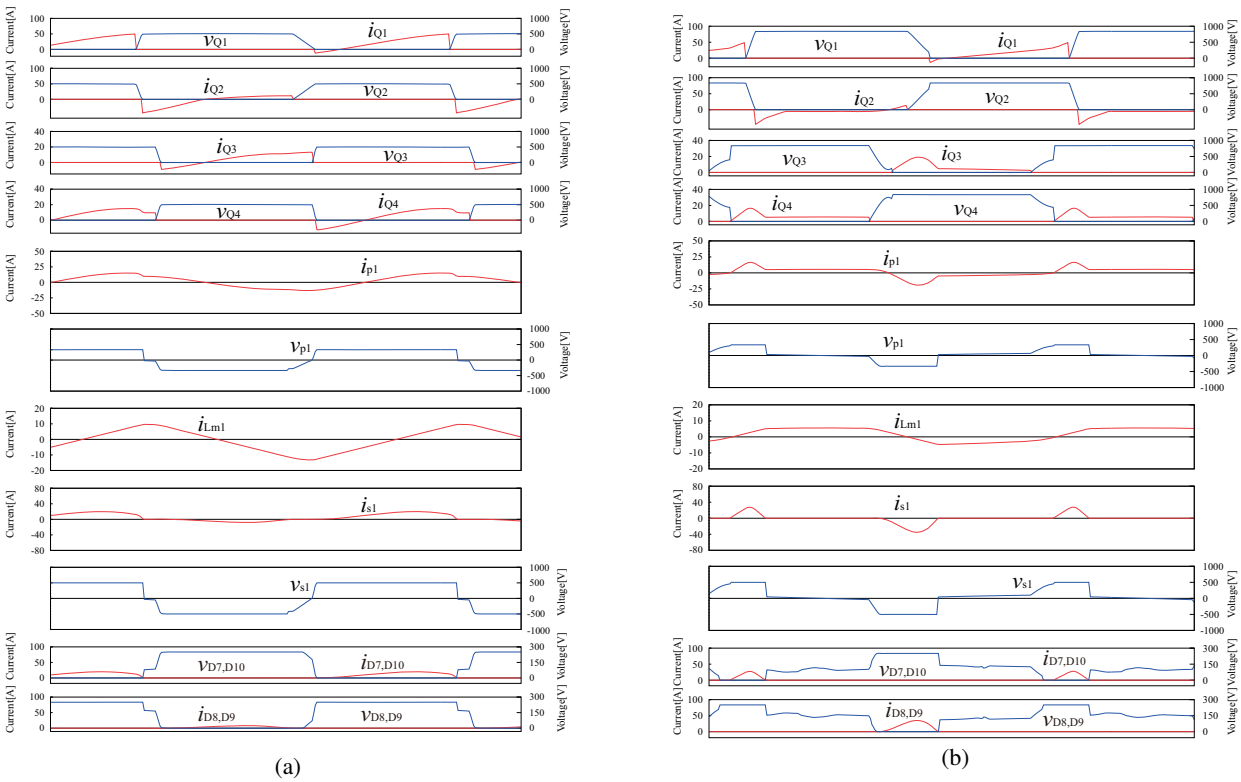



Fig. 13. Simulation waveforms of the switching performances with PS-PWM for $V_o = 400\,\mathrm{V}$: (a) CV and $\phi = 25\,^\circ$, and (b) CV and $\phi = 140\,^\circ$.

### *B. Prototype Specification*

The performances of the proposed converter is investigated by experiment of a downsizing model. The essential parameters of the prototype are listed in TABLE I. All the

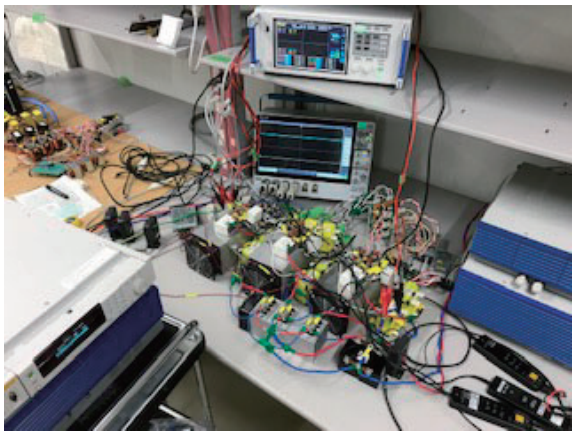


Fig. 14. Exterior appearance of the prototype and experimental system.

TABLE I
MAIN SPECIFICATION OF PROTOTYPE

| Item, Symbol | Value |
|---|---|
| AC input source voltage(rms) $V_{\mathrm{in.rms}}$ | 100-200 [V] |
| Output power (rating) $P_{\mathrm{o}}$ | 2 [kW] |
| Boost inductor $L_{\mathrm{b}}$ | 40 [$\mu$H] |
| DC-bus capacitor $C_{\mathrm{d}}$ | 5 [$\mu$F] |
| Series resonant inductor $L_{\mathrm{s}}$ | 30 [$\mu$H] |
| Series resonant capacitor $C_{\mathrm{s}}$ | 0.34 [$\mu$F] |
| HF-X magnetizing inductance $L_{\mathrm{m}}$ | 200 [$\mu$H] |
| HF-X winding turns ratio $a(=N_{\mathrm{p}}/N_{\mathrm{s}})$ | 2 |
| Line filter inductor $L_f$ | 200 [$\mu$H] |
| Line filter capacitor $C_f$ | 1.83 [$\mu$F] |
| Utility frequency $f_{\mathrm{u}}$ | 60 [Hz] |
| First resonant frequency $f_r$ | 50 [kHz] |
| Second resonant frequency $f_m$ | 18 [kHz] |
| Cut-off frequency of Line filters $f_{uc}$ | 8.8 [kHz] |

active switches are assembled by Silicon super junction power MOSFET (IXFN100N65X2, 650 V, 78 A, 30 m$\Omega$, IXYS), and the rectifier is comprised of Fast Recovery Epitaxial Diodes (FRED) DSEI2x-31-06C (600 V, 30 A, 50 ns, IXYS). The gate signal patters for the active switches are generated by a DSP microcontroller TMS320F28335F embedding PFM / PS-PWM hybrid control.

### C. Observed Waveforms and Steady-State Characteristics

The three-phase voltages and currents are displayed in Fig. 15. PFC can be confirmed in the three sets of source voltages and line currents, as a result an excellent PFC as high as 0.99 is recored in each phase module. Inequality of high frequency components appears among $i_a$, $i_b$ and $i_c$ due to the parameters' imbalance of line filters $L_f$ and $C_f$. The inductive and capacitive values of filters are same among the three phases as $L_f = 200\,\mu$H, $C_f = 1.83\,\mu$F and the cut-off frequency is $f_{uc} = 8.8\,$kHz for the nominal switching frequency 50 kHz. Small glitch among those parameters may occur in the process of fabrication, then the impedance imbalance generates among the low pass filters of the three-phase power sources; consequently elimination of the high frequency components is slightly mismatched in the three-phase line currents. However,

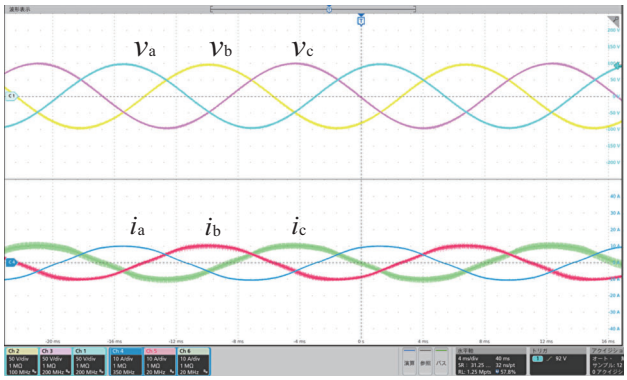



Fig. 15. Observed waveforms of three-phase power sources ($v_a$, $v_b$, $v_c$: 50 V/div., $i_a$, $i_b$, $i_c$: 10 A/div).

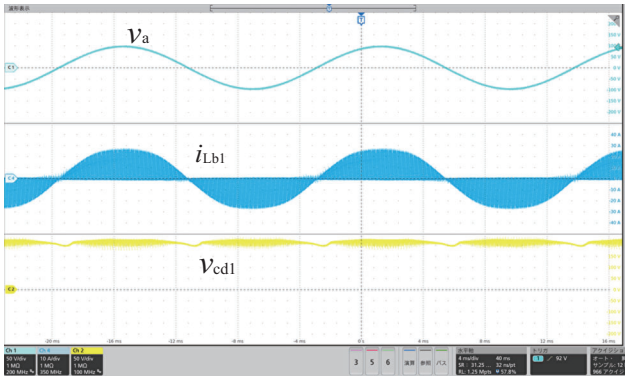



Fig. 16. Voltage and current waveforms of phase-$a$ BFB circuit ($v_a$, $v_{cd}$:50 V, $i_{Lb1}$:10 A/div).

there are no significant difference in THDs as discussed in the forthcoming section IV-D, thus the inequality of the three-phase line currents has no outstanding impact on the converter performance.

The ac inductor current $i_{Lb1}$ and the clamping capacitor voltage $V_{cd1}$ are displayed wth its phase voltage $v_a$ in Fig. 16. It can be understood that the clamping film capacitor voltage can be regulated at the low voltage ripple while the ac inductor current swings in the high frequency switching cycle by DCM. The rectified currents of each phases are displayed in Fig. 17. It can be revealed from $i_{o1}$–$i_{o3}$ that 120 ° displacement of phase angle achieves successfully with the double utility frequency and switching frequency components among the three-phase modules. The small amounts of currents imbalance due to difference of circuit parameters may occur in the prototype, however it can be reduced by additionally implementing the output current-based balancer compensation in generating the PS angle command signals in each phase independently. Consequently, the smoothed dc voltage and current can be obtained in $V_o$ and $I_o$ as shown in Fig. 18.

The observed switching waveforms are displayed in Fig. 19. It can be conformed that ZVS commutation can attain under the principle of $LCC$ converter. In addition, good agreement with the simulation result especially in Fig. 12 (a) can be obtained in the experimental result.

The converter performances are evaluated under the condi-

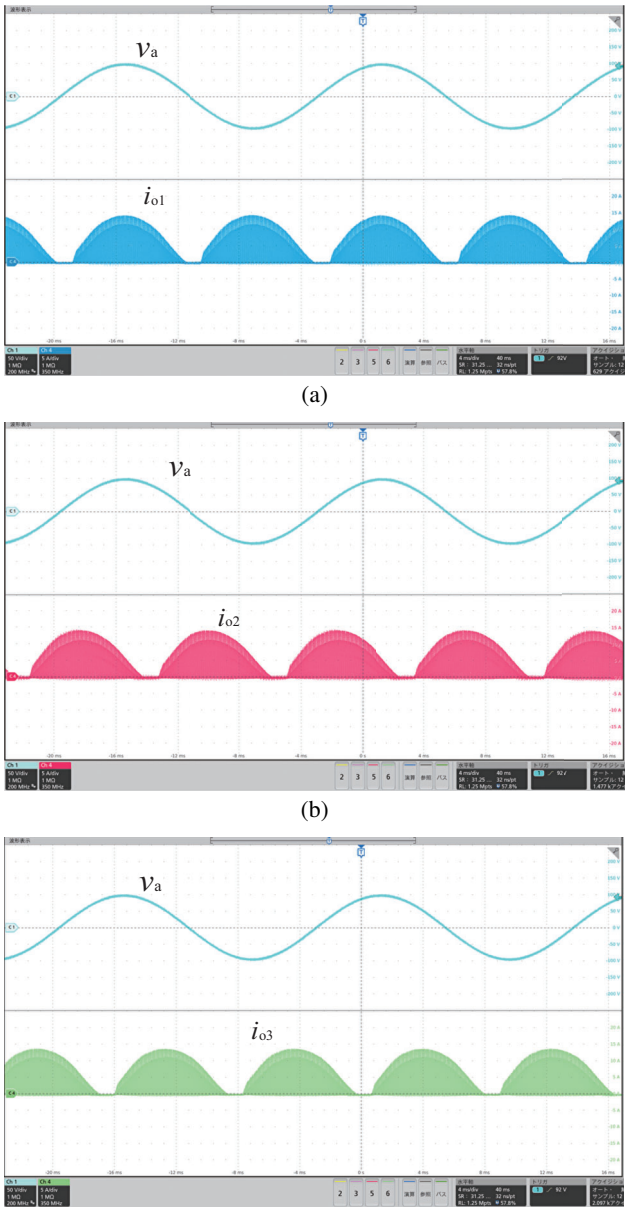



Fig. 17. Rectified currents of each phases referring to the base waveforms $v_a$: (a) phase-$a$, (b) phase-$b$, and (c) phase-$c$ ($v_a$: 50 V/div., $i_{o1}$, $i_{o2}$, $i_{o3}$: 5 A/div).

tion of CCCV load profile assuming for a lithium-ion battery charging. The setting values are as follows; CC command 7 A and CV command 200 V. The measured curves are presented in Fig. 20. The first stage of CC mode is carried out by PFM with the fixed PS angle as shown in Fig. 20 (a), where the dc output current $I_o$ is regulated at 7 A while the dc output voltage $V_o$ increases gradually from the initial value of 125 V toward the voltage command 200 V. Once the dc output voltage approaches 200 V, the circuit operation moves into Fig. 20 (b) where $V_o$ is controlled at the command value 200 V due to PFM while $I_o$ reduces gradually from its command 7 A. Furthermore, the circuit operation shifts into the fixed-frequency PS-PWM as demonstrated in Fig. 20 (c)

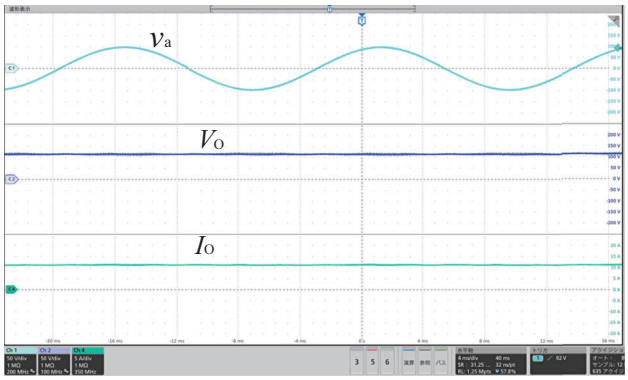



Fig. 18. Output voltage and current referring to the phase-$a$ source voltage ($v_a$, $V_o$; 50 V/div, $I_o$; 5 A/div.).

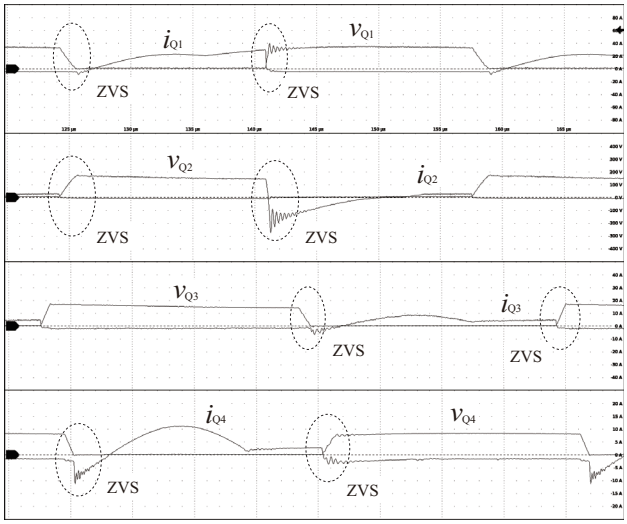
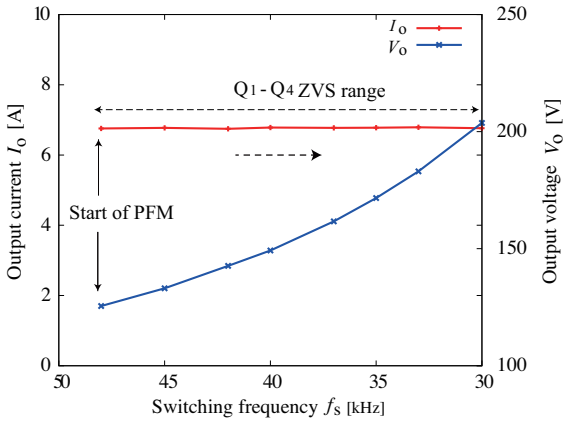



Fig. 19. Switching waveforms in the phase-$a$ BFB circuit ($v_{Q1}$, $v_{Q2}$, $v_{Q3}$, $v_{Q4}$; 100 V/div, $i_{Q1}$, $i_{Q2}$, $i_{Q3}$, $i_{Q4}$; 20 A/div, 4 $\mu$s/div).

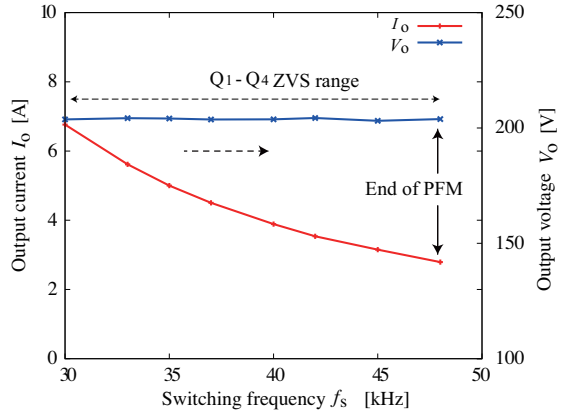
in order to reduce the dc output current with keeping the soft commutations of all the power devices. The ZVS performances can be observed in $Q_1$ and $Q_2$ over the wide range of PFM ad PS-PWM while $Q_3$ and $Q_4$ experiences an incomplete ZVS in the PS angle greater than 110°.

The actual efficiency curves of three-phase ac-dc power conversion stage that is controlled by PFM around the series resonant frequency $f_r = 50$ kHz are indicated in Fig. 21. The switching frequency varies from the limited range; 48 kHz–49.5 kHz while the PS angle is fixed at 0°. The maximum efficiency is observed in this curve as 91.5 % at 2.0 kW.

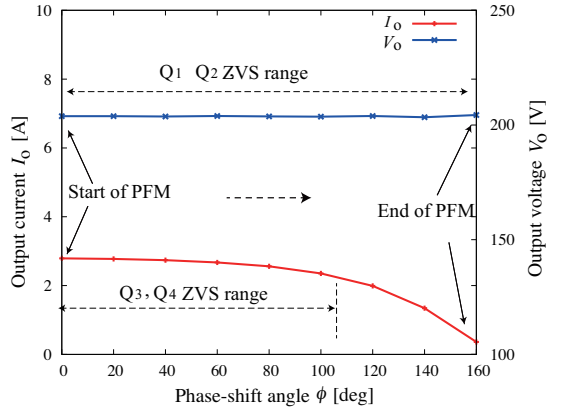
Power loss analysis based on the experimental measurements is displayed in Fig. 22. Note herein that all the switching losses are excluded since soft switching can attain in the active switches and diodes at $P_o = 2$ kW. The copper and iron losses in the HF-X, which are measured by the power meter, are relatively small due to a low-loss ferrite core PC-40. Conduction losses of the power devices dominate by a large part of breakdowns. Therefore, adoption of wide-band-gap power devices such as SiC-MOSFET may be an effective solution for power efficiency improvement.




(a)




(b)




(c)

Fig. 20. Measured curves of pseud CCCV-mode battery charging: (a) CC characteristics by PFM, (b) CV characteristics by PFM, and (c) CV characteristics by PS-PWM.

TABLE II
MEASURED THDS OF THREE-PHASE LINE CURRENTS

| PS angle $\phi$ | phase-$a$ | phase-$b$ | phase-$c$ |
|---|---|---|---|
| 20 ° | 2.45 % | 2.40 % | 2.37 % |
| 90 ° | 2.43 % | 2.3, % | 2.33 % |

### D. Analysis on Line Current Harmonics

The measured total harmonics distortion (THD) is listed in TABLE II, whereby the achievement of low distortion can be confirmed. In addition, the measured harmonics analysis of the line current are displayed in Fig. 23 with respect to the load variation around the series resonant frequency. It is revealed from the results that the line current harmonics are constrained well under the regulation values (IEC-61000-3-2-class A) regardless of the conditions of PS angle. Thus, the practical effectiveness of the proposed ac-dc converter is clearly verified.

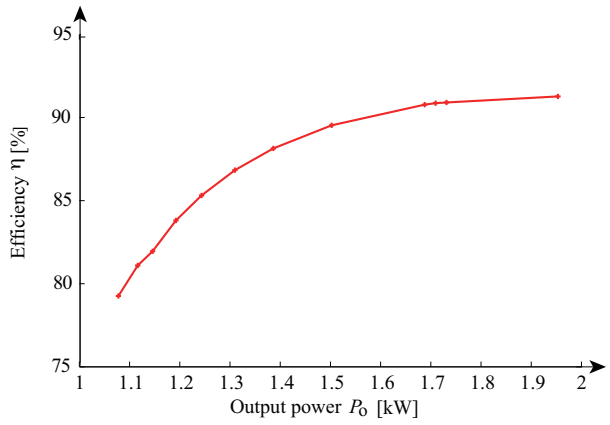



Fig. 21. Actual efficiency of three-phase ac-dc power conversion in the prototype (measured by Power analyzer HIOKI PW6001).

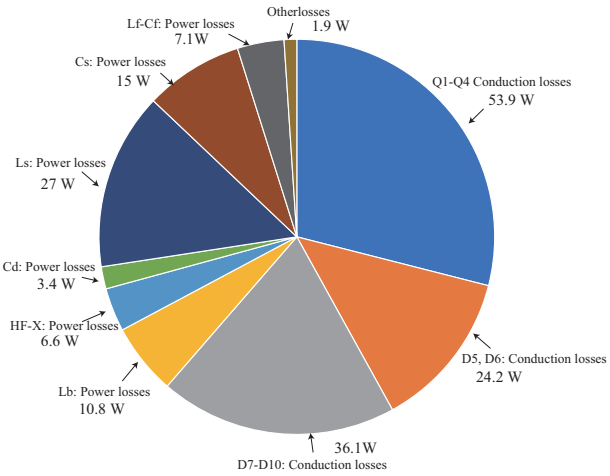
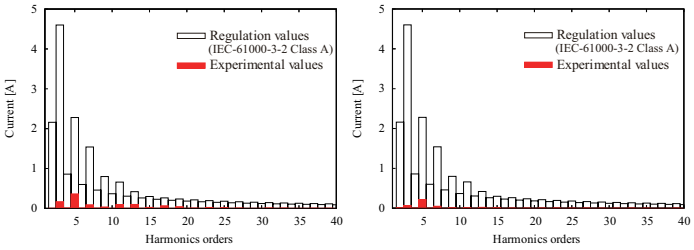



Fig. 22. Power loss analysis at $P_o = 2$kW.




(a) (b)

Fig. 23. Harmonics analysis of line current (phase-$a$): (a) $\phi$=20 °, and (b) $\phi$ = 90 °.

TABLE III
COMPARISON OF ISOLATED THREE-PHASE AC-DC CONVERTERS

| Circuit Topology<br>Features<br>Modularity | Switching frequency | DC-link Filter voltage ripple | THD of line currents | S-SW<br>Max. Efficiency | Modulation |
|---|---|---|---|---|---|
| Matrix converter[12]<br>unidirectional<br>one fullbridge rectifier<br>N/A | 50 kHz | None | Low | ZVS&ZCS<br>93.8 %@600 W | SVM |
| Matrix converter[3]<br>bidirectional<br>one active rectifier<br>N/A | 10 kHz | None | Low | ZVS&ZCS<br>82.1 %@1.5 kW | DPS† |
| Nine-switch[13]<br>(three-switch three-leg)<br>Low | 60 kHz | Bulky,<br>low | Low<br>2.89 % | ZVS<br>95 %@3 kW | PWM |
| Phase modular[20]<br>two-stage<br>PWM conv.& full-bridge conv.<br>Middle | 50 kHz | Small<br>high | High<br>6 % | NR<br>97 %@20 kW | DPS / TPS‡ |
| Phase modular[21]<br>Bridgeless TL-INV &<br>three voltage doubler<br>Middle | 30 kHz | Bulky,<br>low | Low | ZVS&ZCS<br>97 %@2 kW | PS-PWM |
| Phase modular[25]<br>single-stage BFB<br>High | 20 kHz | Small<br>film cap.<br>low | Middle<br>4 % | ZVS<br>83.7 %@3 kW | PS-PWM |
| Proposed converter<br>single-stage $LLC$-BFB<br>High | 30-50 kHz | Small<br>film cap.<br>low 6 % | Low<br>2.3-2.4 % | ZVS&ZCS<br>91.5 %@2 kW | PFM<br>PS-PWM |

† DPS: Dual Phase shift ‡ TPS: Triple Phase Shift.

### *E. Comparison with Other Systems*

Comparison with existing three-phase ac-dc converters with HF-link are summarized in TABLE III. The actual efficiency of prototype is not par with another topologies at the current stage since implementation of printed circuit boards and power device selection are not optimized, whereas efficiency should be compared under the same conditions of input voltage, power rating and so forth. However, the proposed converter has attractive features by high modularity and low voltage ripple in the primary-side clamping capacitor with a film capacitor as well as low electromagnetic noise owing to non-floating connection in the BFB circuit as aforementioned in Section II-A. Thus, a wide variety of system configurations are acceptable for the proposed converter such as series connection in each phase for medium voltage dc microgrid, three-phase four-wire telecommunication, and single-phase three-wire system for smart house EV battery charger applications.

## V. CONCLUSIONS

A new single-stage high frequency-link three-phase $LLC$ ac-dc converter has been proposed in this paper. The circuit topology and operation principle have been described with the remarkable features and the key design guideline of essential circuit parameters. The natural cancellations of double-frequency power and high frequency power fluctuations inherent to the single-stage principle are theoretically explained with the relevant equations, whereby the principle of large chemical capacitor-less circuit topology has been clarified. The hybrid pulse modulation of PFM and PS-PWM has been introduced schematically for extending the soft switching range of active switches. The soft switching conditions have been revealed individually for the fixed and lagging-phase switches in terms of inductive and capacitive energy of the edge resonant circuits. The practical effectiveness of the proposed converter has been investigated by experiment of prototype: i) The three-phase ac to dc power conversion with a single-stage UFAC to HFAC conversion has been demonstrated with PFC and ZVS operations of the $LLC$ converter phase unit. ii) The CCCV mode operations for a battery charger can attain by adopting the PFM and PS-PWM hybrid power controller. iii) The line current harmonics are well reduced by 2-3 %, consequently the high power factor 99 % has attained in the three-phase ac sources.

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