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ABSTRACT

We propose a compact computational method based on the capacitance model for the efficient design of graphene-based synaptic field effect transistors (FETs), in which the hysteresis of conduction characteristics due to the channel–gate interface trap is used as synaptic plasticity. Using our method to calculate the conduction properties of graphene and armchair graphene nanoribbon (AGNR) superlattice FETs, it is shown that the AGNR can achieve an efficient conductance change rate Δw, which is approximately 7.4 times that of graphene. It was also found that Δw was the greatest when the gate oxide thickness was around 2–3 nm, which is near the limit of miniaturization. These results suggest that the proposed synaptic FETs are a promising approach to realize large scale integration chips for biological timescale computation.

I. INTRODUCTION

With the advent of the big data era and the demand for real-time edge computing, the development of high speed and low power consumption electronic devices is becoming more important. Neuromorphic computing has attracted great attention as one of the promising directions in realizing low power signal processing by means of electronic circuit mimicking of biological nervous systems that are highly energy efficient.[1–4] It also has the potential to contribute to the development of medicine and neuroscience through mutual computation with the biological nervous system.[5,6]

Generally, a neuromorphic processor has two main components. The first one is the synapse, which is memory that stores binding weights with biologically relevant analog values. The second is the neuron, which generates spike outputs in response to spike inputs via the synapse. In recent years, synaptic devices using memristors, two-terminal devices whose resistance changes according to the current flowing through themselves via the phase change mechanisms, such as the formation of conductive filaments, have attracted attention and are expected to be applied to large scale integrated neuromorphic systems because of their ultrahigh speed drive, ultralow power consumption, and high scalability.[7,8] However, resistive two-terminal devices have difficulty in simultaneously transmitting synaptic signals and learning unlike natural synapses. Such difficulties can be overcome by using three terminal synaptic devices based on FETs, which have been shown to enable simultaneous synaptic signal transmission and learning with good stability and controllable device characteristics and have attracted attention as a new approach to replace two-terminal synaptic devices.[9–11]

As materials in FET fabrication, two-dimensional atomic film materials, such as graphene, have been attracting attention as next-generation materials due to their unique physical characteristics, such as high electron mobility and wider control of electronic transport properties by changing their widths.[12–14] For neuromorphic applications, high-performance synaptic devices can be realized by exploiting their sensitivity to the surrounding environment, such as charge trapping at the surface, which results in the hysteresis of conduction properties and makes it possible to realize synaptic functionality as experimentally reported in Refs. 15–17. From this viewpoint, two-dimensional atomic film materials are highly advantageous since the conducting channel is directly contacted to its surrounding environment, that is, insulating materials, such as SiO_2.

Despite recent experimental progress, an efficient and reliable computational methodology to study the synaptic behavior of graphene FET quantitatively has not been explored enough thus far except for a few simulation and modeling studies,[18–23] where the interface trap charge and the channel charge are treated in a separate way. Further detailed analysis of synaptic FETs for various

materials requires a unified general framework to treat the interface trap charge and the channel charge on equal footing. Moreover, it has not been studied enough so far how the controllable device parameters of graphene FET, such as the oxide thickness and the width of graphene in the form of the graphene nanoribbon (GNR), influence the device performance from the viewpoint of the synaptic functionality. With this motivation in mind, we propose a compact computational method to clarify the performance of graphene and GNR FETs as synaptic devices, in which the hysteresis of conduction characteristics due to the channel–gate interface trap is used as synaptic plasticity.

The remainder of the paper is organized as follows: Section II describes the method used to calculate the band structure and electrical conduction properties of the channel material and the model used to simulate the hysteresis of the conduction properties due to the interface trapping charge. Section III presents the results of the calculations, and Sec. IV discusses the results and summarizes the paper.

II. THEORETICAL FORMALISM

A. Tight-binding (TB) formalism

Figure 1 shows a schematic of the device structure considered in this study, where the channel property is described using the tight-binding (TB) method. In the TB formalism, the electronic properties of graphene and the GNR channel can be obtained by solving the eigenvalue problem $H(\boldsymbol{k})|\psi_l(\boldsymbol{k})\rangle = E_l(\boldsymbol{k})|\psi_l(\boldsymbol{k})\rangle$, where $H(\boldsymbol{k})$ is the wavenumber $\boldsymbol{k}$ dependent Bloch Hamiltonian of graphene or GNR spanned by the p_z orbitals within the unit cell and $E_l(\boldsymbol{k})$ describes the lth energy band.

Regarding GNR, we focus our attention to armchair GNR (AGNR) because of its semiconducting property with the finite bandgap that depends on the width of the AGNR. In particular, we consider the AGNR superlattices, in which the number of atoms in the width direction of AGNR is periodically varied. In the present study, we examine the superlattice of 7-AGNR and 9-AGNR illustrated in Fig. 2, where it has been theoretically shown that the occurrence of a zero-dimensional topological interface state at the interface between the topologically non-trivial region and another topologically non-trivial region generates a new band near the Fermi surface,[24,25] resulting in the narrowing of the bandgap depending on the lengths of the 7-AGNR and 9-AGNR regions.

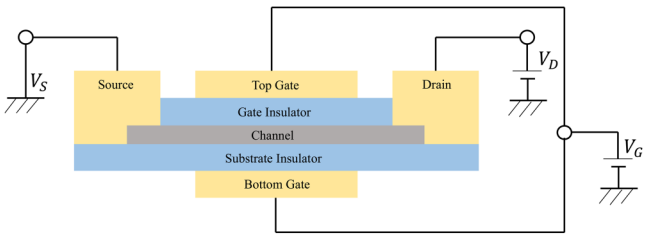

FIG. 1. Model diagram of the field effect transistors (FETs) assumed in this study. Double gating improves the gate voltage effect and doubles the interface area. In addition, it is thought to be able to prevent disturbances from factors other than the channel–oxide film interface.

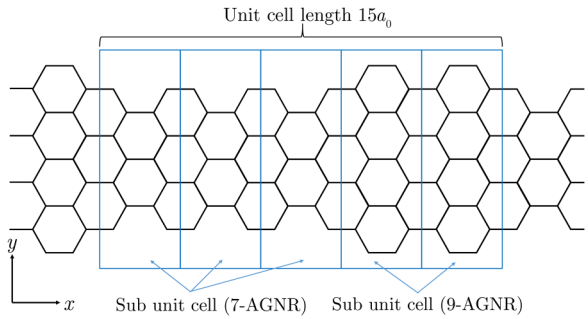

FIG. 2. Unit cell of the armchair graphene nanoribbon (AGNR) superlattice, which we call 7(3)/9(2)-AGNR from the number of sub-unit cells in the 7-AGNR (3) and 9-AGNR (2) regions, respectively.

B. Current calculation method under ballistic conditions

Once the band structure $E_l(\boldsymbol{k})$ and the wave function $|\psi_l(\boldsymbol{k})\rangle$ are calculated, the current density of a channel with ideal electrodes at both ends can be calculated as

$$I = \frac{q}{\hbar}\frac{1}{N_{\mathrm{kp}}S_{\mathrm{UC}}}\sum_{l}^{N_{\mathrm{UC}}^{\mathrm{orb}}}\sum_{\mathbf{k}\in\mathrm{BZ}}^{N_{\mathrm{kp}}}|v_l(\mathbf{k})| \times [f(E_l(\mathbf{k})+U_{\mathrm{C}}-E_{\mathrm{FL}}) - f(E_l(\mathbf{k})+U_{\mathrm{C}}-E_{\mathrm{FR}})], \quad (1)$$

$$v_l(\boldsymbol{k}) = \frac{1}{\hbar}\frac{\mathrm{d}E_l(\boldsymbol{k})}{\mathrm{d}\boldsymbol{k}} = \frac{1}{\hbar}\left\langle \psi_l(\boldsymbol{k})\left|\frac{\mathrm{d}H(\boldsymbol{k})}{\mathrm{d}\boldsymbol{k}}\right|\psi_l(\boldsymbol{k})\right\rangle. \quad (2)$$

Here, N_{kp} is the total number of $\mathbf{k}$ sampling points within the 1st BZ; $N_{\mathrm{UC}}^{\mathrm{orb}}$ is the total number of orbitals in the unit cell; $q = -e$ is the charge of an electron; $E_l(\mathbf{k})$ and $v_l(\mathbf{k})$ are the energy and the group velocity for the energy eigenstate $|\psi_l(\boldsymbol{k})\rangle$, respectively; $f(E)$ is the Fermi distribution function, where $E_{\mathrm{FL/FR}}$ is the Fermi energy in the left/right electrode; and U_{C} is the electrostatic potential of the channel. Note that in the case of nanoribbons, the current, not the current density, is derived because the wavenumber direction is considered only in one dimension.

C. Capacitance model considering interface trapped charge

In this subsection, we propose a computational methodology to analyze FETs with interface trapping charges with the assumption of the following properties. First, only trapping charges near the interface are considered, and trapping on defects inside the bulk oxide film are not considered. Second, the effect of trapping charges is uniformly distributed throughout the channel. The given trapping/de-trapping time constants and the interface density of

states are used, and the interface density of states is assumed to be constant with respect to energy.

The channel voltage V_C actually felt by electrons in the graphene channel is diminished from the applied gate voltage V_G due the channel induced charge Q_C and the interface trapped charge Q_{it}. To calculate the channel electrostatic potential $U_C = -eV_C$ taking the channel and the trapped charge into account, we use a capacitance model that considers the FET as a set of capacitors.[26] Figures 1 and 3 show the geometry of the FETs considered in the present study and the corresponding capacitance model that is electrostatically equivalent to Fig. 1. In this model, the following equation holds:

$$Q_C + Q_{it} = C_{ox}(V_C - V_G) + C_D(V_C - V_D) + C_S(V_C - V_S), \tag{3}$$

where C_S and C_D are the source and drain capacitances derived from the metal–semiconductor junction, respectively; C_{ox} is the gate oxide capacitance; and V_S and V_D are the source and drain voltages, respectively. Assuming source grounding and $C_S, C_D \ll C_{ox}$, Eq. (3) can be rewritten as

$$V_C = V_G + \frac{Q_C(V_C)}{C_{ox}} + \frac{Q_{it}(V_C)}{C_{ox}}, \tag{4}$$

where we emphasize that Q_C and Q_{it} are functions of V_C. The channel charge Q_C can be expressed as the product of the channel area, the elementary charge, and the number of electrons per unit area as follows:

$$Q_C(V_C) = S_{channel} \times (-e) \times \frac{N^{neq}_{ele/UC} - N^{eq}_{ele/UC}}{S_{UC}}, \tag{5}$$

where $S_{channel}$ is the channel area, $N^{neq}_{ele/UC}$ is the number of electrons per unit cell in the non-equilibrium state, and $N^{eq}_{ele/UC}$ is the number of electrons per unit cell in the charge-neutral state ($N^{eq}_{ele/UC} = 2$ for graphene without doping). Here, $N^{neq}_{ele/UC}$ is calculated as

$$N^{neq}_{ele/UC} = \frac{2}{N_{kp}} \sum_{l}^{N_{orb/UC}} \sum_{k \in BZ}^{N_{kp}} \times \left[\frac{f(E_l(\boldsymbol{k}) + U_C - E_{FL})}{2} + \frac{f(E_l(\boldsymbol{k}) + U_C - E_{FR})}{2} \right], \tag{6}$$

with $E_{FL/FR}$ being the Fermi energy of the left/right electrode, defined in terms of the drain voltage V_D as $E_{FL} = E_F$ and $E_{FR} = E_F - eV_D$.

Before describing how to derive Q_{it}, we will discuss the assumed phenomenon. It is known that hysteresis can be observed in the drain current I_D as a function of V_G depending on the surface condition of the gate oxide film in contact with the channel material.[27–29] In the case of SiO_2 oxide films, hysteresis characteristics are observed when there are many silanol groups (–SiOH) on the surface of the gate oxide film due to the trapping and de-trapping of channel electrons at the interface states derived from these groups.[30]

We introduce a model of the interface trap charge as shown in Fig. 4. Electron transfer from the channel to the interface states (trapping) occurs when the Fermi level E_F is higher than the top of the occupied interface level (hereafter denoted as E_{it}), while that from the interface states to the channel (de-trapping) occurs when E_F is lower than E_{it}. In the subsequent formulation to calculate E_{it}, we set the origin of energy at the Dirac point of graphene so that the Fermi energy is always positioned at $E = eV_C$ in graphene. On the basis of this phenomenological treatment, for a given arbitrary time varying gate voltage profile $V_G^{(j)}$ (not necessarily a monotonically increasing/decreasing function) with a time index j and time step Δt, Q_{it} at the jth V_G is calculated sequentially starting from $Q_{it}^{(0)}$ according to the following recurrence equations:

$$Q_{it}^{(j)} = Q_{it}^{(j-1)} + \Delta Q_{it}^{(j)}, \tag{7}$$

$$\Delta Q_{it}^{(j)} = -|e| \int_{E_{it}^{(j-1)}}^{E_{it}^{(j)}} D_{it}(E) dE, \tag{8}$$

$$E_{it}^{(j)} = \left(eV_C(V_G^{(j)}) - E_{it}^{(j-1)} \right) \left(1 - \exp(-\Delta t/\tau_{trap}) \right) + E_{it}^{(j-1)}, \tag{9}$$

$$E_{it}^{(0)} = eV_C(V_G^{(0)}), \; Q_{it}^{(0)} = 0, \tag{10}$$

where E_{it} is the top of the occupied interface level measured from the Dirac point in graphene, $V_C(V_G)$ is the graphene channel potential for a given gate voltage V_G, $D_{it}(E)$ ($eV^{-1}\,m^{-2}$) is the interface density of states, and τ_{trap} (ms) is the trapping/de-trapping time constant. On the basis of the experimental results of previous studies, $D_{it}(E)$ in Eq. (8) is treated as an energy independent constant.[29] In the special case of the linearly increasing or decreasing gate voltage, the time step is given in terms of the gate voltage sweep rate χ_{sweep} (V/ms) as $\Delta t = \Delta V_G/\chi_{sweep}$, which is interpreted as the time required to sweep the gate voltage by ΔV_G. The factor

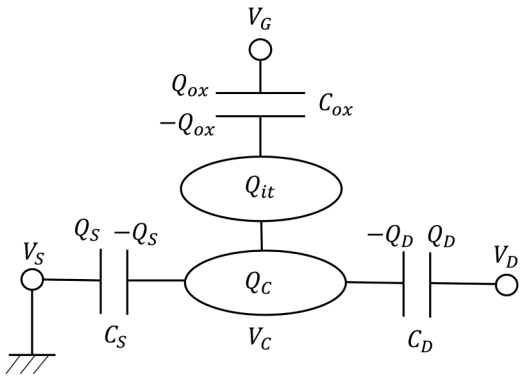

FIG. 3. Capacitance model electrostatically equivalent to the FET geometry shown in Fig. 1.

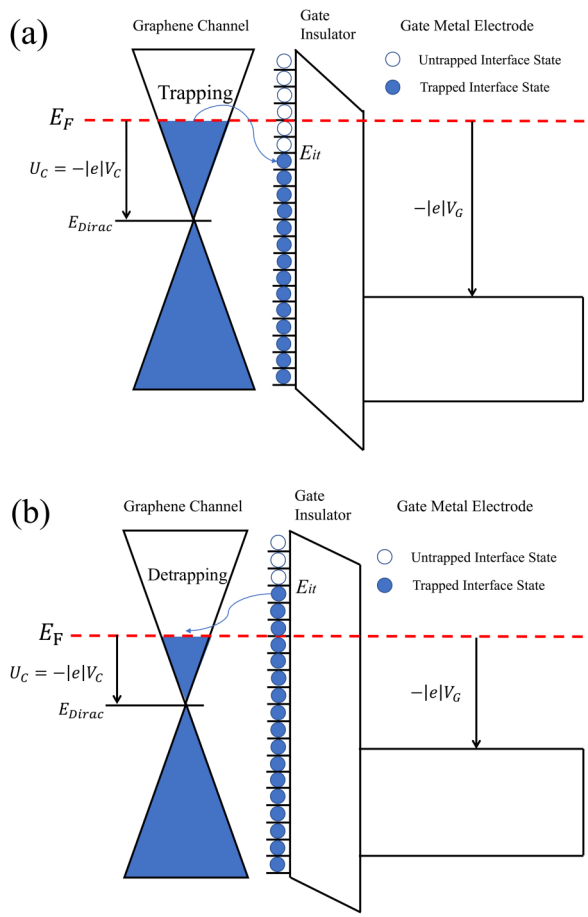

FIG. 4. Energy band diagram of FET and schematization of the interfacial trapping/de-trapping process at different bias conditions: (a) $E_{it} < E_F$ and (b) $E_{it} > E_F$. This figure is based on Figs. 2(c) and 2(d) in Ref. 29.

$1 - \exp(-\Delta t/\tau_{trap})$ is the probability that the interface states are actually trapped during the time step Δt.

In our actual simulations, this factor $1 - \exp(-\Delta t/\tau_{trap})$ is approximated as $\Delta t/\tau_{trap}$ since $\Delta t \ll \tau_{trap}$ in our simulation conditions. Equation (10) is used as the initial condition of the recurrence formulas. That is, under the assumption that the gate voltage is fixed at its initial value $V_G^{(0)}$ for a sufficiently long time, the trapping/de-trapping probability becomes one and then $E_{it}^{(0)}$ coincides with $eV_C(V_G^{(0)})$.

In the above proposed model, various electronic properties, such as the channel charge density, the channel potential, and the interface density of states, are assumed to be homogeneous. However, our model can be generalized to account for their spatial inhomogeneity, where the nonequilibrium Green function (NEGF) method plays a central role in performing a self-consistent calculation with the Poisson equation to account for the real spatial effects of the channel potential.[31]

III. RESULTS AND DISCUSSIONS

A. Hysteresis of conduction characteristics

To clarify the usefulness of the above proposed method, we first examine the case of linear gate voltage sweep and analyze the hysteretic properties. We employ the following parameter values in this paper unless otherwise noted. The parameter values for interface trap are $\tau_{trap} = 100$ ms and $D_{it} = 1.875 \times 10^{16}$ eV^{-1} m^{-2}, which are experimentally reported values.[32] Since we consider the double-gated FET structure as shown in Fig. 1, the value of D_{it} is actually doubled. The relative permittivity of the SiO_2 oxide film was given as $\kappa = 3.8$ and the thickness of the gate oxide film as $t_{ox} = 3$ nm.

In this subsection, we biased the graphene FETs with $V_D = 0.1$ V and swept V_G linearly from -2 to 2 V (forward sweep) with the various gate sweep rate χ_{sweep}, assuming that V_G was initially fixed at -2 V for a sufficiently long time and subsequently swept V_G from 2 to -2 V (backward sweep) with the same sweep rate. The calculated results of the I_D-V_G properties are shown in Fig. 5

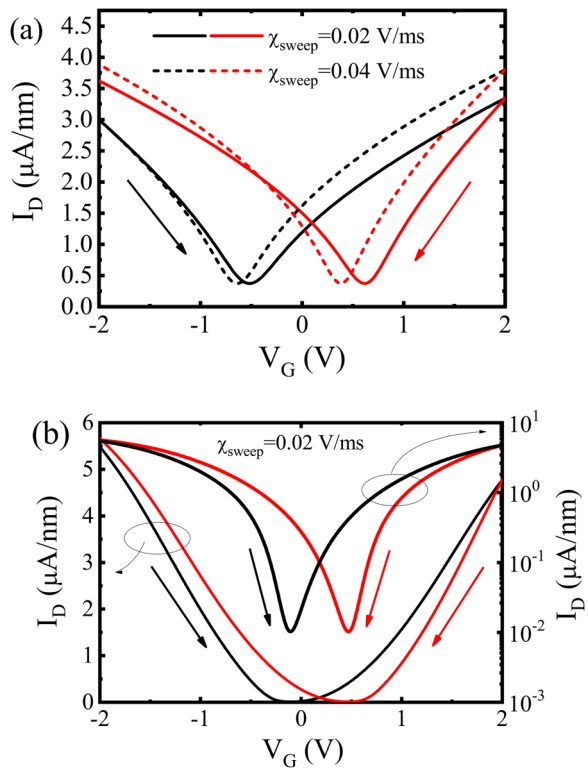

FIG. 5. Conduction characteristics of graphene-based FETs under linear gate voltage sweeps for (a) graphene and (b) 7(3)/9(2)-AGNR to demonstrate the appearance of the hysteresis behavior. In both (a) and (b), black and red curves correspond to the forward sweep (from -2 to 2 V) and backward sweep (from 2 to -2 V), respectively. In (a), results for two different gate sweep rates $\chi_{sweep} = 0.02$ (solid curves) and 0.04 (dashed curves) V/ms are compared, while in (b), the result for $\chi_{sweep} = 0.02$ is plotted in the linear (left axis) and logarithmic (right axis) scales. We note that in (b), the current flowing through AGNR is divided by the effective AGNR width to obtain the current density (see the text for detail).

for graphene (a) and AGNR (b). We note that in (b), the current flowing through 7(3)/9(2)-AGNR (in units of μA) is divided by the effective AGNR width 1.08 nm to obtain the current density to compare with the case of graphene, where the effective width of 7(3)/9(2)-AGNR is defined by $[N_7(7+1)+N_9(9+1)] \times (\sqrt{3}a_0/2)/N_{\rm tot}$ with $N_7 = 3$, $N_9 = 2$, and $N_{\rm tot} = N_7 + N_9$.

Here, it is observed that the overall conduction characteristics for backward V_G sweep is shifted to the positive V_G direction compared to that for backward V_G sweep. The direct reason for this behavior is that the channel voltage V_C at a given specific V_G is lower for the backward sweep case than for the forward sweep case, where the behind physical mechanism is that the interface trapped charge $[Q_{\rm it}(V_C) < 0]$ is continuously accumulated during the forward sweep, and in the subsequent backward sweep, this accumulated (negative) trapped charge causes the value of V_C to be less than the forward sweep through the third term in the RHS of Eq. (4). This result agrees qualitatively with the experimentally observed behavior,[21,28,29] suggesting that our model can capture the essential physics in the trap/detrap behavior. We also note that the amount of the shift of the I_D–V_G curve due to the interface trapped charge is larger for smaller values of gate sweep rate $\chi_{\rm sweep}$. This is because slower gate sweep results in larger probability for electrons to be trapped at the interface. Similar behavior can be observed for the case of 7(3)/9(2)-AGNR (hereafter, we simply call AGNR) channel as demonstrated in Fig. 5(b). It can be seen that the opening of a bandgap of about 0.50 eV creates an off region where almost no I_D flows. The width of the off region (transport gap) is approximately 200 mV if we define the off state as when $I_D < 20$ nA. Such a relatively narrow but clear transport gap and the significant shift of the I_D–V_G curve due to the interface trapped charge are preferable in designing energy efficient synaptic devices utilizing a biologically plausible spike voltage displacement of approximately 100–150 mV.

B. Synaptic FET application

So far, we have discussed the hysteresis behavior of graphene and AGNR FETs due to charge trap/detrap processes. Such hysteresis behavior can be used as a key mechanism to realize synaptic functionality as explained below. In Fig. 6(a), we show the schematic illustration of the synapse-neuron system premised in this study, where the pre-neuron is connected to the post-neuron via the synapse made of FET. Then, the superposition of voltage spikes launched by the pre- and post-neurons [i.e., $V_{\rm in}(t) + V_{\rm out}(t)$ in Fig. 6(b)] is assumed to be used as the time-dependent gate voltage $V_G(t)$ applied to synapse FET. Here, we illustrate in Fig. 6(b) the representative example of the time-dependence of $V_{\rm in}(t)$, $V_{\rm out}(t)$, and $V_G(t) = V_{\rm in}(t) + V_{\rm out}(t)$. As illustrated in this figure, the time-dependence of $V_G(t)$ is different depending on whether $\Delta t \equiv t_{\rm post} - t_{\rm pre} > 0$ or $\Delta t < 0$. Then, the required functionality of synaptic FET is that the electronic conduction property (more specifically the current or conductance at a reference gate voltage, for example, at $V_G = 0$) is changed between before and after completing the voltage pulse $V_G(t)$ shown in Fig. 6(b) in a way depending on the sign and/or value of Δt. This process is interpreted as the spike-timing dependent update of the synapse weight represented by the conductance value and is the essence of the mechanism

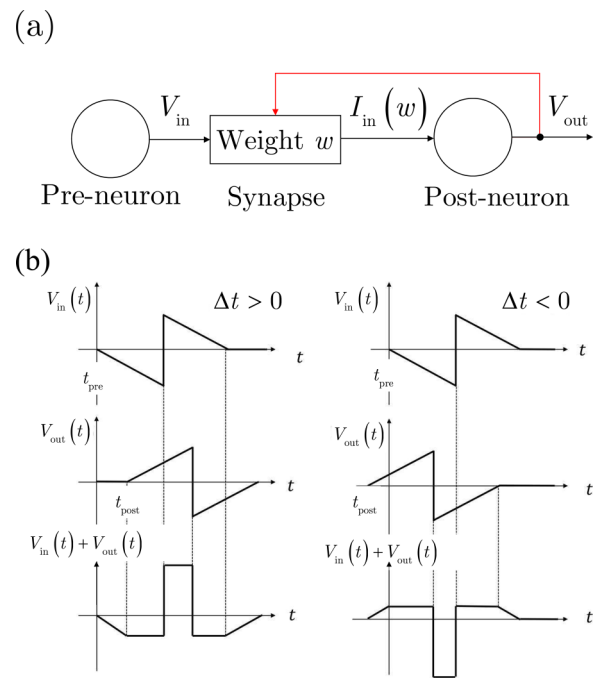

FIG. 6. (a) Schematic illustration of a synapse-neuron system. (b) Representative example of time-dependence of $V_{\rm in}(t)$, $V_{\rm out}(t)$, and $V_G(t) = V_{\rm in}(t) + V_{\rm out}(t)$. Time-dependence of $V_G(t)$ is different depending on whether $\Delta t \equiv t_{\rm post} - t_{\rm pre} > 0$ or $\Delta t < 0$.

called the spike-timing dependent plasticity (STDP). Therefore, the performance of synaptic FET can be evaluated by the current change rate (interpreted as the normalized synapse weight change) $\Delta w \equiv (I_{\rm D,\,after} - I_{\rm D,\,before})/I_{\rm D,\,before}$, where $I_{\rm D,\,before(after)}$ is the drain current at a reference V_G before (after) the voltage pulse $V_G(t)$ that starts and ends at $V_G = 0$. We note that normalized synapse weight w is updated every time a new voltage pulse is applied, and the resulting update of w is interpreted as the update of weight in the context of the spiking neural network (SNN).

C. Comparison of the conductance change rate between graphene and AGNR superlattices

To focus our discussion on how the weight w is changed by voltage pulses in graphene and AGNR FET systematically, we assume the simple linear functional forms of the voltage pulse [instead of a more realistic but complicated pulse form, such as illustrated in Fig. 6(b)], expressed as $V_G(t) = \chi_{\rm sweep} t$ for $t \le t_0$, $V_G(t) = \chi_{\rm sweep}(2t_0 - t)$ for $t_0 < t \le 2t_0$, and otherwise $V_G(t) = 0$, where $t_0 \equiv V_{\rm Gmax}/\chi_{\rm sweep}$ is the time required to reach the maximum gate voltage $V_{\rm Gmax}$ for a given gate sweep rate $\chi_{\rm sweep}$. In Fig. 7, we show the forward and backward I_D–V_G curves for graphene and AGNR cases, where we set $V_{\rm Gmax} = 0.1$ V while $\chi_{\rm sweep} = 0.002$ or 0.02 V/ms. By comparing the current at $V_G = 0$ between the forward and backward sweep, one can estimate the weight change Δw as $\Delta w = 13.8$ (4.2)% for graphene and

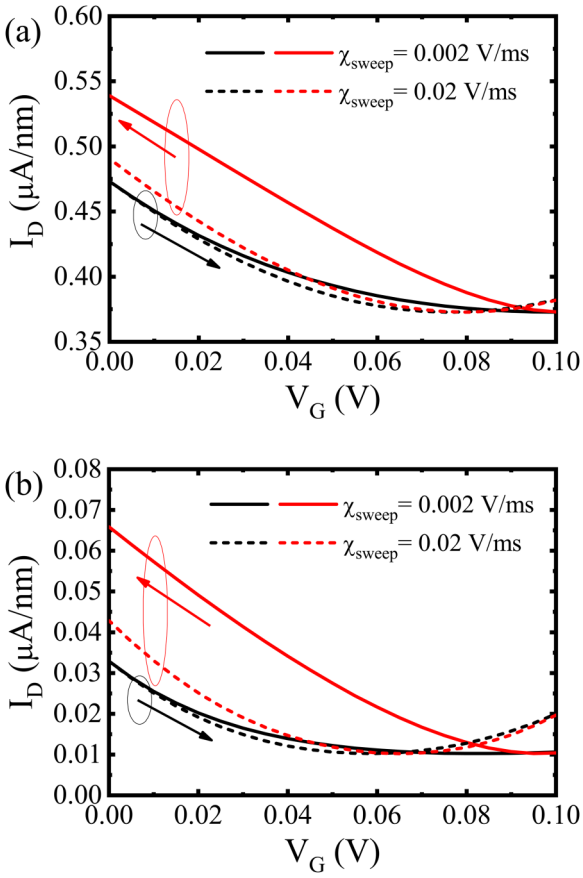

FIG. 7. Conduction characteristics and a conductance change rate of graphene-based FETs under a 0–100 mV linear gate voltage sweep: (a) graphene and (b) 7(3)/9(2)-AGNR. For the AGNR case, the current is divided by the effective AGNR width to obtain the current density. In both (a) and (b), black and red curves correspond to the forward sweep (from −2 to 2 V) and the backward sweep (from 2 to −2 V), respectively, and the results for two different gate sweep rates $\chi_{sweep} = 0.002$ (solid curves) and 0.02 (dashed curves) V/ms are compared.

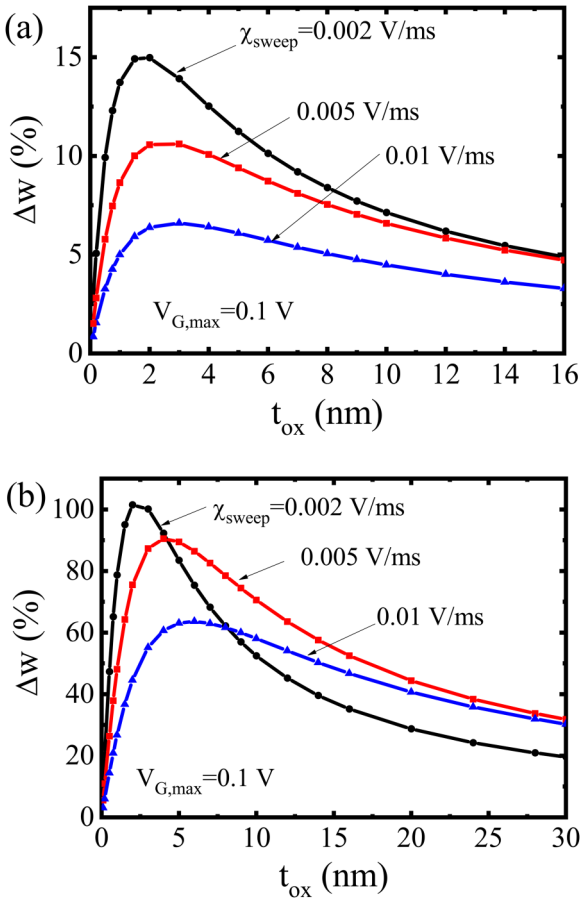

FIG. 8. Synapse weight changes Δw in the case of linear voltage sweep (see the text for detail) are plotted for (a) graphene and (b) 7(3)/9(2)-AGNR FETs as a function of the SiO_2 gate oxide film thickness t_{ox}. Results for various gate sweep rates χ_{sweep} are compared.

$\Delta w = 102.5$ (28.6)% for AGNR FET for $\chi_{sweep} = 0.002$ (0.02) V/ms. A large Δw means a large memory window, suggesting that 7(3)/9(2)-AGNR can construct a better synaptic FET than graphene. So far, we have assumed that the gate oxide thickness is $t_{ox} = 3$ nm. Next, we consider how t_{ox} and thus C_{ox} influence the synapse weight Δw. According to Eq. (4), one can see that C_{ox} suppresses the effect of the channel charge Q_C and interface trap charge Q_{it} on the channel voltage V_C. If the effect of Q_C is large, V_C becomes small and the effect of V_G degrades (quantum capacitance effect), which in turn reduces Q_{it} from Eqs. (7)–(9). From this observation, it looks that it is preferable to increase C_{ox} to diminish the effect of Q_C. However, larger C_{ox} results in the decrease of Q_{it} and suppresses the hysteresis behavior, which is not preferable as a synaptic device. Therefore, it is important to optimize C_{ox} to maximize the synapse weight change Δw. For this purpose, we plot Δw as a function of t_{ox} of the SiO_2 gate oxide film for various χ_{sweep} in Fig. 8. It can be seen that Δw reaches a maximum at $t_{ox} = 2-3$ nm. One interesting feature seen here is that a faster gate sweep rate χ_{sweep} results in the shift of the Δw peak to the thicker t_{ox} direction. This is because a faster gate sweep results in smaller amounts of trapped charge. Then, a too thin t_{ox} suppresses the hysteresis behavior. We also note that the thickness $t_{ox} = 2-3$ nm is around the scaling limit for a SiO_2 gate when tunneling is concerned, indicating that the scaling strategy works well for the synapse FET as well.

D. Long-term potentiation (LTP)/long-term depression (LTD) properties of synaptic FETs

So far, we have considered the linear gate sweep to clarify the fundamental aspects of graphene-based synapses. Finally, we consider a more experimentally accessible case, a square pulse train sweep given by $V_G(t) = \sum_i V_i \theta(t - t_i)\theta(t_i + T_{pulse} - t)$, where V_i is the pulse voltage, t_i is the pulse arrival time, and T_{pulse} is the

pulse width. We assume that i runs from 1 to 40, $V_i = V_p$ for $1 \leq i \leq 20$ and $V_i = -V_p$ for $21 \leq i \leq 40$ with V_p mentioned later, $T_{pulse} = 5$ ms, and $t_i = (T_{pulse} + T_{interval})i$ with $T_{interval} = 20$ ms. In Fig. 9, we show the results for graphene (a) and AGNR (b), where the results for two different pulse voltage values $V_p = 0.1$ and 0.2 V are compared. For both graphene and AGNR, the calculated Δw gradually increases as the multiple positive voltage pulses are applied and is saturated as the charging process is completed. When the pulse voltage becomes negative at $i = 21$, Δw is abruptly turned to negative, meaning that the synapse weight is turned from potentiation to depression and is interpreted as the realization of so-called long-term potentiation (LTP) and long-term depression (LTD), respectively. As we can expect from Figs. 7 and 8, AGNR shows a larger magnitude of Δw. It is also observed that the LTP process shows larger $|\Delta w|$ than in the LTD process. Such asymmetricity of $|\Delta w|$ between LTP and LTD is more significant in the AGNR case than graphene. To equalize the magnitudes of the positive and negative changes, the pulse waveform must be adjusted. The confirmed saturation and asymmetry have also been experimentally observed in the synaptic FETs based on $MoTe_2$ as a channel.[33] The above-mentioned asymmetry is basically due to the positive drain voltage V_D (= 0.1 V), which pushes the minimum current voltage to the positive V_G side. The larger asymmetry in GNR superlattices can be attributed to the presence of off-regions, which are absent in graphene. Although it has been said that synaptic devices with symmetry and linearity are ideal, it is noted that STDP-based unsupervised SNNs obtain high classification accuracy values in the modified National Institute of Standards and Technology (MNIST) classification by having synapses with nonlinear behavior.[34]

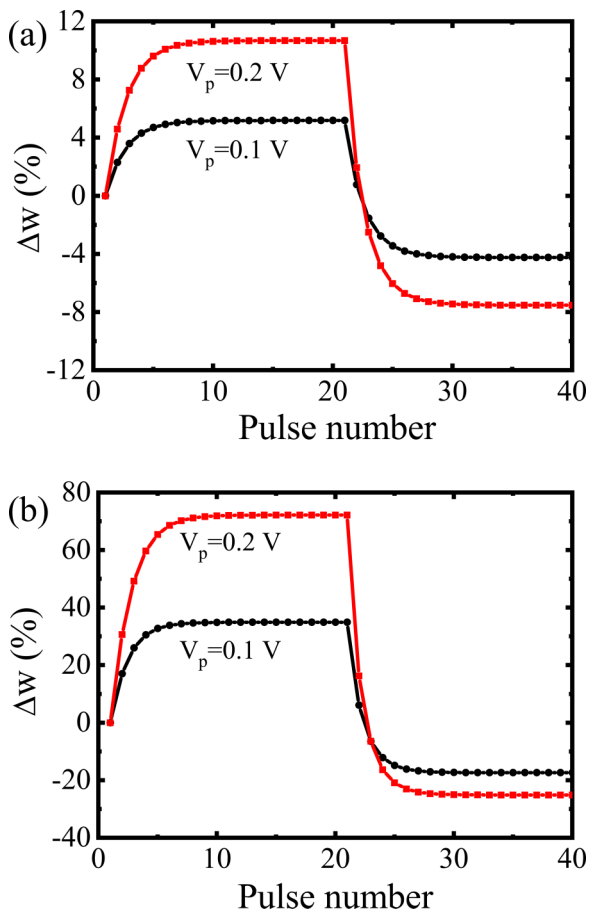

FIG. 9. Synapse weight changes Δw in the case of square pulse train voltage sweep (see the text for detail) are plotted for (a) graphene and (b) 7(3)/9(2)-AGNR FETs as a function of the SiO_2 gate oxide film thickness t_{ox}. Results for two different pulse voltage values $V_p = 0.1$ and 0.2 V are compared. We note that the first and second half of the voltage sweep correspond to the synaptic long-term potentiation (LTP) and synaptic long-term depression (LTD), respectively, as explained in the text.

IV. CONCLUSION

In this paper, we proposed a compact computational method based on the capacitance model for the efficient design of graphene-based synaptic field effect transistors (FETs), in which the hysteresis of conduction characteristics due to the channel–gate interface trap was used as synaptic plasticity. Using our method to calculate the conduction properties of graphene and armchair graphene nanoribbon (AGNR) superlattice FETs, we have succeeded to obtain the hysteresis behavior in the I_D–V_G curves of graphene and AGNR FETs, where it was clarified that the current modulation due to the hysteresis behavior (interpreted as the synaptic weight change) can be tuned by changing the gate sweep rate χ_{sweep} and the gate oxide thickness t_{ox}. Moreover, it was shown that the AGNR can achieve an efficient conductance change rate Δw, which is approximately 7.4 times that of graphene. It was also found that Δw was the greatest when the gate oxide thickness was around 2–3 nm, which is near the limit of miniaturization. We have also examined the case of square voltage pulse train sweep and demonstrated the pulse voltage dependent asymmetricity in the long-term potentiation/long-term depression behaviors. These results suggest that the proposed synaptic FETs are a promising approach to realize large scale integration chips for biological timescale computation.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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