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# Measurement of electromagnetic field immunity of voltage-controlled oscillatorbased analog-to-digital converters in 28 nm CMOS technology

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Internet-of-Things (IoT) devices are compact and low power. A voltage-controlled oscillator (VCO)-based analog-to-digital converter (ADC) benefits from scaled CMOS transistors in representing analog signals in the time domain and therefore meets those demands. However, we find the potential drawback of VCO-based ADCs for the electromagnetic susceptibility (EMS) to RF disturbances that are essentially present in an IoT environment. It is exhibited that the single and even differential designs of VCO-based ADC suffer from the EMS by RF disturbance, which behaves differently from the known common-mode noise rejection. A 28 nm CMOS 11-bit VCO-ADC prototype exhibits sensitivity against RF signals in the widely used 2.4 GHz frequency band. © 2022 The Author(s). Published on behalf of The Japan Society of Applied Physics by IOP Publishing Ltd

### 1. Introduction

Internet-of-Things (IoT) devices have proliferated over the last few years. Markets have grown for diversified application areas such as smart meters, medical and healthcare devices, autonomous mobility on roads and air, and many others. Edge nodes realize smart sensing in their surrounding environment, where digital data processing is tightly unified with analog signal capturing and wireless communication, with security features. 5,6) A tiny body with a small footprint as well as a low profile is in high demand, and therefore IC technologies are key for the realization of IoT devices.

Electromagnetic compatibility (EMC) is importantly referred to by IoT devices with respect to environmental electromagnetic (EM) disturbances. It becomes highly concerning when IoT devices are densely populated and wirelessly connected.<sup>7,8)</sup> There may exist large RF interferers from switching devices that belong to power converters as well as large-scale digital circuits. 9,10) In addition, the RF carriers for wireless communication standards like WiFi, LTE (long-term evolution), and 5G are also non-negligible. When IoT devices suffer from high EMS, the whole system may become unstable or even fall in an unexpected state. Though a commercial electronic product is verified for compliance to various EMC standards such as on emission<sup>11)</sup> and RF immunity,<sup>12)</sup> where the object distance is typically defined as 3 m or larger for far-field measurements in an anechoic chamber room. However, the level of disturbance can surpass its tolerance by high power EM irradiation when the IC chip and the RF source are closely positioned, assuming much less than 1 m, which can naturally happen when IoT devices are highly populated in an area. Analog functionality is essentially responsive to surrounding EM fields and can be the root cause of the vulnerability of IoT devices.

Analog quantity of interest is preferably converted to digital values in the earliest stage of signal processing. ADCs are unquestionably keys to this role and have been developed and transitioned over technology generations with a variety of conversion principles and associated circuit architectures for best performance. Successive approximation register (SAR) ADCs have been widely adopted due to their high energy efficiency across technology generations. Recently,

VCO-based ADCs have suitably emerged for low-voltage ultimately scaled CMOS technologies, thanks to analog signal expression in the time domain. <sup>18–22)</sup> The adoption of IoT applications has been launched for the sake of a small form factor and high energy efficiency. Additional features include the high tolerance to unexpected interactions with the surrounding EM environment, which can happen inevitably or even intentionally, in a passive<sup>23)</sup> or active<sup>24)</sup> manner. Those circuits need to be designed with the awareness of undesired EM interactions, and might also be embedded with the in-place detection of unexpected disturbance<sup>25)</sup> The baseline knowledge to accomplish the goal will be provided mainly through a variety of experimental explorations as what is addressed in this paper.

This paper focuses on the EM susceptibility of VOC-based ADCs, which is attributed to the frequency-domain response of oscillators. The major extensions to the abstract paper<sup>24)</sup> by the authors are given by in-depth experimental results that shed light on the mechanisms of susceptibility even on the differential circuit architecture. Section 2 details the circuit constructions and evaluation methodologies. Section 3 discusses the experimental results. Section 4 provides conclusions.

# 2. EM susceptibility of VCO-based ADCs

The schematic diagram of a VCO-based ADC is illustrated in Fig. 1. The ADC first converts an analog input voltage  $V_{\rm IN}$  to a clock signal with a corresponding frequency  $F_{\rm VCO}$ , and then to a digital code  $D_{\rm OUT}$ . The voltage-frequency conversion is executed by VCO as follows, where  $K_{\rm VCO}$  is the conversion coefficient.

$$F_{\text{VCO}} = K_{\text{VCO}} \cdot V_{\text{IN}} \tag{1}$$

A ring oscillator (RO) based analog-to-time conversion is chosen in the simplest VCO-based ADC architecture, which is designed on a test chip of this work. The RO includes current starved inverters as delay cells. The input voltage  $V_{\rm IN}$  controls the amount of current flowing during logic transition through the transistor stack, and thus influences the pulse delay of each cell and the output frequency of RO. After generating the clock signal with the input voltage-dependent

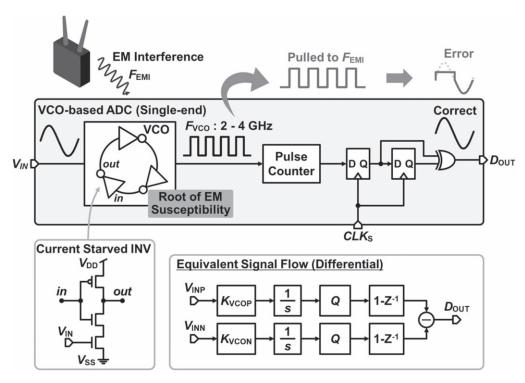


Fig. 1. VCO-based ADC circuit structures. Single and differential conversion principles are also shown. Reproduced from Ref. 24.

frequency, the clock pulses are counted by an asynchronous counter circuit. This operation is equivalent to the frequency signal integration. The subsequent quantization process is executed by acquiring the asynchronous counter value in flip flops (FFs) with a sampling clock  $CLK_s$ . Then, the output code can be obtained by taking the difference between two consecutive data in the first-order differentiator.

This overall conversion process, in the case of differential structures, is shown as a signal flow graph at the bottom of Fig. 1. After converting the input analog signal to the frequency of the clock like the output signal with the voltage-frequency coefficients  $K_{\rm VCOP}$  and  $K_{\rm VCON}$ , the clock signal is sequentially integrated, quantized and differentiated, which enables the first-order delta-sigma modulation. Thus, the VCO-based ADC can digitize the narrowband signals with a high signal-to-noise ratio (SNR), since the quantization noise is suppressed by the noise shaping function. In addition to such a high-resolution feature, the VCO-based ADC is an extremely simple configuration and mostly composed of digital circuits.

The EM waves affect the operation of ADC, where the VCO frequency  $F_{\rm VCO}$  can be pulled to the EM interference frequency  $F_{\rm EMI}$ , if the magnitude of the EM wave is sufficiently large. The VCO-based ADC is directly affected by the EM disturbance and produces an erroneous code in accordance with  $F_{\rm EMI}$ . This will not be prevented even when the VCO is biased by a replica phase-locked loop (PLL), because the EM disturbance remains in a short period of time where a feedback control will not respond. Since the oscillation frequency of the VCO is generally designed at several GHz, which is typically close to RF carrier frequencies in wireless systems such as WiFi and LTE, the EM interferers are naturally present in the field of operation.

The differential structure is widely known as an effective method to remove the influence of common-mode noise from the outside, however, it is not effective in the case of EM interference on the VCO-based ADCs since this frequency pulling differently changes the VCO output frequencies among the differential channels, and then generates erroneous codes as differential outputs.

Measurements will be discussed in the following section.

## 3. Experimental results

The test chip for the VCO-based ADC was implemented in a 28 nm CMOS technology with a chip size of 1.0 mm  $\times$  1.5 mm as shown in Fig. 2. The VCO-based ADC occupies only 20  $\mu m \times 60~\mu m$  thanks to its digital standard cell-based configuration and the scaled technology. Both single and differential structures are designed and fabricated for comparison, where the resolution and the sampling rate are 11 bits and 3 MHz, respectively. The controller of the whole chip and the subtraction circuit in the differential channels are also embedded as synthesized logic blocks in the test chip.

The EMS test setup is depicted in Fig. 3. We irradiate the test chip with an RF EM wave through a WiFi antenna. The RF signal is generated in two ways, as (1) precisely located at  $F_{\rm EMI}$  (typically at 2.4 GHz) by a signal generator (SG), and (2) naturally emitted in the 2.4 GHz band from a WiFi router. The ADC has the input control codes to be stored in the internal registers and the output codes to be collected after conversion, which is connected to external digital controllers implemented on a field-programmable gate array (FPGA) device. The outputs are then visibly shown on an oscilloscope for functional checks and also captured in a computer (PC) for the performance evaluation.

The object distance from the antenna is adjusted by using a positioner, as shown in Fig. 4, with respect to the device under test (DUT) board and also to the probe of either electrical field (E-field) or magnetic field (H-field) measurement. The test chip is directly assembled on the DUT board in a face-up way, as also shown in the figure, where its surface side faces the antenna.

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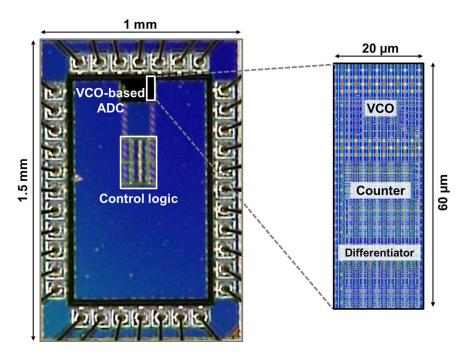


Fig. 2. (Color online) Photo of 28 nm CMOS test chip. The physical layout of VCO-based ADC is also shown. Reproduced from Ref. 24.

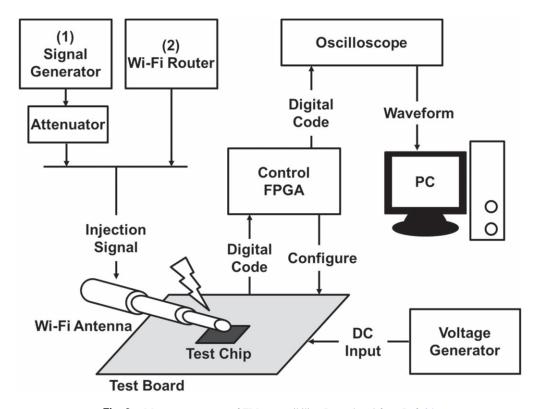


Fig. 3. Measurement setup of EM susceptibility. Reproduced from Ref. 24.

The response of VCO-based ADC against the EM radiation by (1) SG and (2) WiFi router are compared in Figs. 5(a) and 5(b), respectively. The input to ADC is the DC voltage swept for the whole input voltage range from 0.6 V to 0.8 V. The output code from ADC changes smoothly to the input voltage without RF EM irradiation, however, starts to be stacked at the fixed level once it is irradiated with a sufficiently large magnitude. Here, the single-ended (non-differential) version is tested. The locking of ADC output codes is exhibited due to the frequency pulling to EM waves by both sources. In (1), the  $F_{\rm EMI}$  of 2.4 GHz and also 2.5 GHz

are exploited, showing that the locking can occur at any frequency around 2.4 GHz and sustain for a certain range of input voltage. The output power of SG,  $P_{\rm in}$ , was kept constant at 12 dBm In (2), as magnified in Fig. 5(b) for the input voltage range of sensitivity, since the WiFi signal is modulated around 2.4 GHz and intermittently emitted, the pulling happens randomly in time and therefore appears unevenly in the curve. The RF EM waves are naturally present in the environment and potentially cause erroneous codes. The VCO-based ADC responds almost linearly to the input voltage from 0.60 V to 0.65 V as shown in Fig. 5(a),

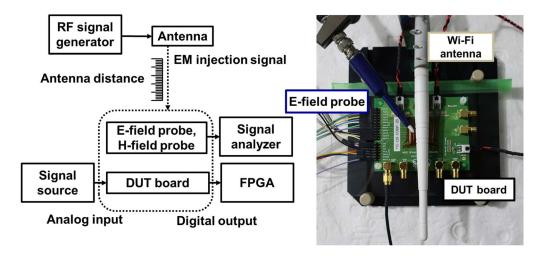


Fig. 4. (Color online) Relative positions of WiFi antenna and DUT board and field probes. Photo is also shown in the case with the E-field probe.

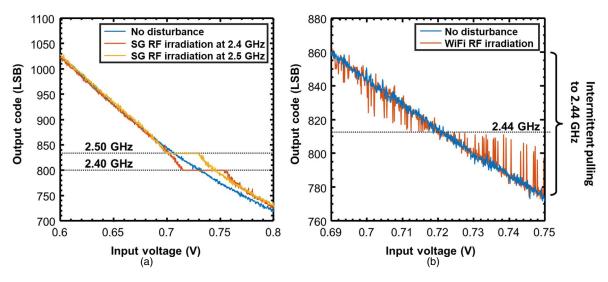


Fig. 5. (Color online) Input voltage to output codes of VCO-based ADC under RF EM irradiation.

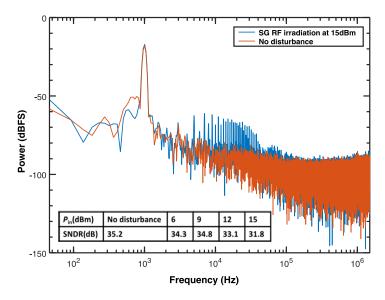
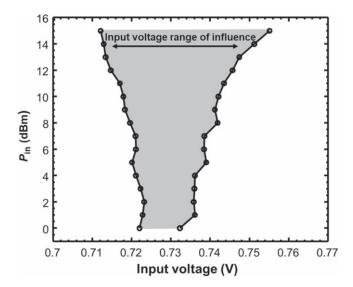


Fig. 6. (Color online) Frequency spectrum and SNDR compared among no RF disturbance and with RF EM irradiation at different power levels.

then deviates clearly from the linear region if the input becomes larger than 0.65 V. Within the whole linear region of 0.50 V to 0.65 V, the internal VCO is oscillating at around 3.3 GHz when the input voltage is 0.56 V. To test the impact

of the EM disturbance at the corresponding frequency, we applied a continuously irradiating EM disturbance at 3.3 GHz. As shown in Fig. 6, the frequency spectrum of the ADC output exhibits the harmonic components with © 2022 The Author(s). Published on behalf of



**Fig. 7.** Input voltage range of influence by frequency locking with RF EM irradiation.

respect to the input sinusoid of 1 kHz in a wide frequency range, which indicates a significant impact on the ADC performance. The signal to noise and distortion ratio (SNDR) is 35.2 dB with the input signal amplitude of 50 mV and without the EM disturbance. This becomes more deteriorated with the larger amplitude of EM disturbance and reduces roughly by 3 dB with the largest RF power of 15 dBm in this experiment.

The frequency locking of VCOs through pulling by intentional injection of sinusoidal waves has been widely

known, among theoretical investigations<sup>26,27)</sup> and active utilization for performance circuitry.<sup>27–29)</sup> However, the phenomena conversely appear here as the source of EMS, in an unexpected or in an intentional way<sup>30)</sup> and should be prevented by IoT devices for the higher tolerance to environmental disturbances.

The range of input voltage that is affected by the frequency locking of VCO by pulling is measured on the DUT, as in Fig. 7. In the zone colored in gray, corresponding to the input voltage range of influence, the output is forced at the code equivalent to  $F_{\rm VCO}$  at  $F_{\rm EMI}$ , due to the frequency pulling. It is also shown that the larger  $P_{\rm in}$  to the antenna generates the stronger electric field nearby the ADC, and results in a wider range of input voltage of influence with the forced output code.

The differential version of the ADC is also tested, as in Fig. 8. The better linearity is expected by the nature of differential signaling, as in Fig. 8(a). The output codes measured on the respective P-path and N-path, named for convenience, are shown on the bottom chart against the input voltage given to ADC. The differential output is shown on the top chart. In contrast, the P-path and N-path are individually locked to respective codes in the different zone of the input voltage range of influence by the RF EM irradiation at the same frequency and with the same power, as shown in the bottom chart of Fig. 8(b). This makes the differential output suffer from the locking, which appears as being distorted in the input-output response [the top chart of Fig. 8(b)]. Because of the fact that each path is differently influenced by EMS, the EM interference is essentially

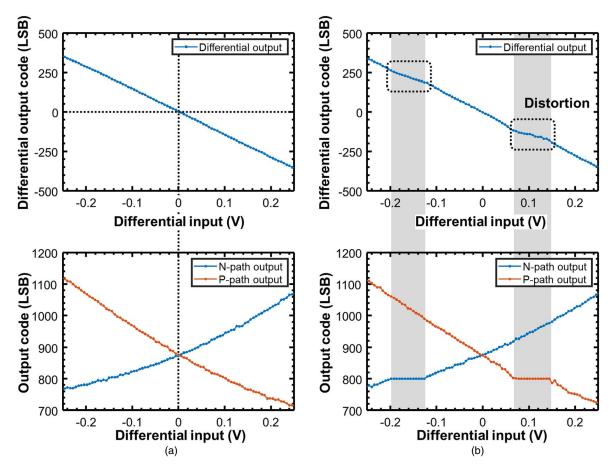


Fig. 8. (Color online) Differential channels of VCO-based ADC (a) without RF EM irradiation and (b) with RF EM irradiation.

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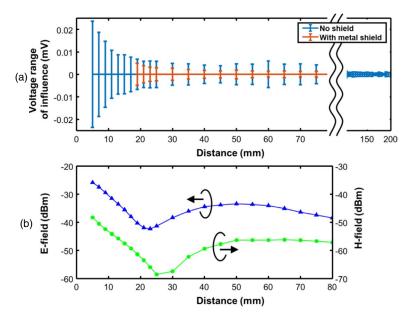


Fig. 9. (Color online) (a) Input voltage range of influence with dependency to object distance from WiFi antenna. (b) Measured E-field and H-field strengths.

different from the common-mode disturbance and not mitigated with the differential circuit constructions.

The strength of EM fields is related to the input voltage range of locking by using the experimental setup of Fig. 4, with changing the objective distance and the power of irradiation. It is shown in Fig. 9(a) where the EM wave at 2.4 GHz with the source output power of 12 dBm sustains the EM sensitivity of VCO-based ADCs even at the distance of 20 mm away from the source. The electrical (E) and magnetic (H) fields are respectively measured in Fig. 9(b), showing that both E- and H-fields contribute specially in the near field. It is preliminarily confirmed that the measurement gain of H-field probing is 20 dB relatively smaller than E-field one, by the far-field measurements with a distance more than two times the wavelength of 125 mm.

The larger field strengths in general lead to the wider voltage range. It is also evaluated when the DUT board is covered by metallic shields except for the area of the test chip and additionally shown in the red bars in Fig. 9(a). The input voltage range of influence decays faster with the shielding if we compare the red bars with blue ones for the distance larger than 18 mm. This indicates that there are some parts of coupling within the DUT board, however, the contribution is weaker than the direct coupling to VCO-based ADC circuits on the test chip. It is noted here that the shielding structure is located 15 mm above the test chip.

These measurements clarify the fact that the VCO is highly sensitive to EM waves nearby an IC chip, and physically needs isolation structures.

#### 4. Conclusions

We have demonstrated that the VCO-based ADC exhibited EMS when  $F_{\rm EMI}$  coincides with  $F_{\rm VCO}$  which the situation is not apart from the nominal environment for IoT devices. The experimental results in this paper contribute to the first step of exploration toward practical considerations or standardization on the EMC design of IoT devices. It is also keen in future

research to investigate the circuit techniques for desensitization.

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- O. Vermesan and P. Friess (ed.) "Internet of Things from research and innovation to market deployment," *Internet of Things - From Research and Innovation to Market Deployment* (River Publishers, Ljubljana, 2014).
- A. Zanella, N. Bui, A. Castellani, L. Vangelista, and M. Zorzi, "Internet of Things for smart cities," IEEE Internet Things J. 1, 22 (2014).
- S. M. Riazul Islam, D. Kwak, M. H. Kabir, M. Hossain, and K.-S. Kwak, "The Internet of Things for health care: a comprehensive survey," IEEE Access 3, 678 (2015).
- A. Fotouhi, H. Qiang, M. Ding, M. Hassan, L. G. Giordano, A. Garcia-Rodriguez, and J. Yuan, "Survey on UAV cellular communications: practical aspects, standardization advancements, regulation, and security challenges," IEEE Commun. Surv. Tutor. 21, 3417 (2019).
- Y. Yang, L. Wu, G. Yin, L. Li, and H. Zhao, "A Survey on security and privacy issues in Internet-of-Things," IEEE Internet Things J. 4, 1250 (2017).
- B. Hammi, A. Fayad, R. Khatoun, S. Zeadally, and Y. Begriche, "A lightweight ECC-based authentication scheme for Internet of Things (IoT)," IEEE Syst. J. 14, 3440 (2020).
- K. Wiklundh and P. Stenumgaard, "EMC challenges for the era of massive Internet of Things," IEEE Electromagn. Compat. Mag. 8, 65 (2019).
- J. Wu et al., "Review of the EMC aspects of Internet of Things," IEEE Trans. Electromagn. Compat. 42, 2604 (2020).
- S. Shimazaki, S. Taga, T. Makita, N. Azuma, N. Miura, and M. Nagata, "Emulation of high-frequency substrate noise generation in CMOS digital circuits," Jpn. J. Appl. Phys. 53, 04EE06 (2014).
- 10) M. Nagata, K. Watanabe, Y. Sugimoto, N. Miura, S. Tanaka, Y. Miyazawa, and M. Yamaguchi, "Evaluation of near-field undesired radio waves from semiconductor switching circuits," Proc. of the 2019 Int. Symp. on Electromagnetic Compatibility (EMC Europe 2019), 2019, p. 866.

- CISPR 32, 2015, Ed. 2.0, "Electromagnetic compatibility of multimedia equipment – Emission requirements," IEC, 2015.
- 12) IEC 61000-4-3, 2020, Ed. 4.0, "Electromagnetic compatibility (EMC) Part 4-3: Testing and measurement techniques Radiated, radio-frequency, electromagnetic field immunity test," IEC, 2020.
- B Razavi, Principles of Data Conversion System Design (Wiley, New York, 1995).
- Boris Murmann, "ADC Performance Survey1997-2021," [Online].
   Available (http://web.stanford.edu/~murmann/adcsurvey.html).
- 15) R. R. Harrison et al., "A Low-power integrated circuit for a wireless 100-electrode neural recording system," IEEE J. Solid-State Circuits 42, 123 (2007).
- 16) T. Miki, T. Ozeki, and J. Naka, "A 2-GS/s 8-bit time-interleaved SAR ADC for millimeter-wave pulsed radar baseband SoC," IEEE J. Solid-State Circuits 52, 2712 (2017).
- 17) Y. Hwang, Y. Song, J. Park, and D. Jeong, "A 0.6-to-1V 10k-to-100kHz BW 11.7b-ENOB noise-shaping SAR ADC for IoT sensor applications in 28 nm CMOS," 2018 IEEE Asian Solid-State Circuits Conference (A-SSCC)=, p. 247, 2018.
- M. Hovin, A. Olsen, T. S. Lande, and C. Toumazou, "Delta-sigma modulators using frequency-modulated intermediate values," IEEE J. Solid-State Circuits 32, 13 (1997).
- R. Muller, S. Gambini, and J. M. Rabaey, "A 0.013 mm2, 5 uW, DC-coupled neural signal acquisition IC With 0.5 V supply," IEEE J. Solid-State Circuits 47, 232 (2012).
- A. Iwata, N. Sakimura, M. Nagata, and T. Morie, "The architecture of delta sigma analog-to-digital converters using a voltage-controlled oscillator as a multibit quantizer," IEEE Trans. Circuits Syst. II 46, 941 (1999).
- 21) T. Miki, N. Miura, K. Mizuta, S. Dosho, and M. Nagata, "A 500MHz-BW -52.5dB-THD voltage-to-time converter utilizing a two-step transition

- inverter," Proc. IEEE 2016 European Solid-State Circuits Conf. (ESSCIRC 2016), 2016, p. 141.
- 22) J. Huang and P. Mercier, "A 112-dB SFDR 89-dB SNDR VCO-based sensor front-end enabled by back-ground-calibrated differential pulse code modulation," IEEE J. Solid-State Circuits 56, 1046 (2021).
- 23) T. Miki, N. Miura, H. Sonoda, K. Mizuta, and M. Nagata, "A random interrupt dithering SAR technique for secure ADC against reference-charge side-channel attack," IEEE Trans. Circuits Syst. Express Briefs 67, 14 (2020).
- 24) H. Sonoda, T. Miki, and M. Nagata, "Electromagnetic susceptibility of VCO-based ADC in 28 nm CMOS technology," Ext. Abstr. of the 2021 Int. Conf. on Solid State Devices and Materials (SSDM 2021), 2021, p. 698.
- 25) T. Wadatsumi, T. Miki, and M. Nagata, "A dual-mode successive approximation register analog to digital converter to detect malicious offchip power noise measurement attacks," Jpn. J. Appl. Phys. 60, SBBL03 (2021).
- S. Verma, H. R. Rategh, and T. H. Lee, "A unified model for injection-locked frequency dividers," IEEE J. Solid-State Circuits 38, 1015 (2003).
- 27) B. Hong and A. Hajimiri, "A general theory of injection locking and pulling in electrical oscillators—part I: time-synchronous modeling and injection waveform design," IEEE J. Solid-State Circuits 54, 2109 (2019).
- 28) J. Lee and H. Wang, "Study of subharmonically injection-locked PLLs," IEEE J. Solid-State Circuits 44, 1539 (2009).
- M. Hossain and A. C. Carusone, "CMOS oscillators for clock distribution and injection-locked deskew," IEEE J. Solid-State Circuits 44, 2138 (2009).
- M. Dumont, M. Lisart, and P. Maurine, "Modeling and simulating electromagnetic fault injection," IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 40, 680 (2021).