An 11-bit 0.008mm2 charge-redistribution digital-to-analog converter operating at cryogenic temperature for large-scale qubit arrays

Miki, Takuji

Takahashi, Ryozo

Nagata, Makoto

(Citation)
IEICE Electronics Express,19(8):20220099

(Issue Date)
2022-04-25

(Resource Type)
journal article

(Version)
Version of Record

(URL)
https://hdl.handle.net/20.500.14094/90009517

ELectronics EXpress

IEICE Electronics Express, Vol.19, No.8, 1–6

LETTER

An 11-bit 0.008 mm^2 charge-redistribution digital-to-analog converter operating at cryogenic temperature for large-scale qubit arrays

Takuji Miki[1, a)], **Ryozo Takahashi**[2], **and Makoto Nagata**[1]

Abstract This letter presents a cryogenic digital-to-analog converter (DAC) for controlling qubits in a large-scale quantum computer. The capacitor arrays composing a charge-redistribution DAC are miniaturized by effectively utilizing the cryogenic characteristics of extremely low noise and leakage. Furthermore, capacitor mismatches due to their small size are automatically corrected by a newly proposed calibration technique with a small area-overhead. Fabricated in 40 nm CMOS and measured at cryogenic temperature, the prototype 11-bit DAC achieved a very small area of 0.3 mm^2 and low power consumption of 5.8 µW, while realizing a nonlinearity error within +/−2 LSB.

Keywords: cryogenic, digital-to-analog converter (DAC), mismatch calibration, quantum computer

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Quantum computers are promising technologies in the near future owing to their theoretical potentials for extremely high computational speed by utilizing superposition and entanglement phenomenon of quantum mechanics. Experimental quantum supremacy, which surpasses the performance of classical supercomputers, has already been demonstrated by a quantum computer prototype consisting of 53 superconducting qubits [1]. However, to achieve more complex calculations on a quantum computer with error correction algorithms, much larger number of qubits are required [2, 3]. A silicon spin qubit is one of the major candidates to realize such large-scale quantum computers, since it can be integrated on a silicon chip by effectively using an existing scaled semiconductor process [4, 5, 6, 7, 8]. Superconducting qubits have also been studied for increasing the number of qubits [9, 10]. These types of qubits need to be operated at cryogenic temperature using a dilution refrigerator, and have traditionally been controlled from outside a refrigerator [11, 12]. However, as the number of qubits increases, it will be difficult to install cables to deliver control signals to qubit arrays if we consider the limited space of a dilution refrigerator. Therefore, the development of a cryogenic control chip placed on a 4–8 K plate in a refrigerator is one of the biggest challenges for realizing large-scale superconducting or silicon quantum computers [13, 14, 15, 16, 17]. Among the qubit control circuits, a bias voltage generator is definitely one of key components to provide arbitrary voltages for multiple purposes to manipulate, read-out and initialize the qubit arrays. This means a large number of DACs for bias voltage generation must be implemented on the control chip and will occupy most of the entire chips. Hence, cryogenic DACs must be designed with extremely small area and low power consumption to meet the limited area and power budgets of the cryogenic control chip installed in a refrigerator.

Several cryogenic DACs for qubit control have been reported so far. A current steering DAC described in [18] operates at 4.2 K with fast response time and can be fully configured by only transistors, which is suitable for integration. However, non-negligible current constantly flows, resulting in the waste of power dissipation in this bias voltage generator even during static operation [19]. A capacitive DAC operating at cryogenic temperature has also been presented [20]. Its quiescent current is very small, however, it requires multiple intermediate voltages to calibrate capacitor mismatches. In addition, the calibration value cannot be estimated in a closed loop, thus, it is not suitable for large-scale DAC arrays.

In this letter, an ultra-small cryogenic capacitive DAC for biasing quantum bits in an array is proposed. The size of capacitors for charge-redistribution is considerably reduced by utilizing the cryogenic characteristics. Furthermore, the process mismatches in capacitor arrays due to their small size are calibrated with extremely small area overhead, thus the proposed calibration can be used for control chips including a number of DACs. The prototype DAC is practically measured at a temperature of 8 K using a cryogenic probe station. The rest of this letter is organized as follows. Section 2 presents the architecture of cryogenic DAC for a quantum computer system. Section 3 introduces the capacitor mismatch calibration technique for multiple DAC arrays. Section 4 shows the measurement results of the prototype DAC at both room temperature and cryogenic temperature. Finally, section 5 gives the conclusion.

2. Cryogenic DAC

2.1 Bias voltage generation for quantum computing systems

Superconducting or silicon qubits are mounted on the coldest plate below 100 mK in a dilution refrigerator. In many quan-

[1] Graduate School of Science, Technology and Innovation, Kobe University, Kobe 657-8501, Japan
[2] Graduate School of System Informatics, Kobe University, Kobe 657-8501, Japan
[a)] miki@cs26.scitec.kobe-u.ac.jp

DOI: 10.1587/elex.19.20220099
Received February 22, 2022
Accepted March 7, 2022
Publicized March 16, 2022
Copyedited April 25, 2022

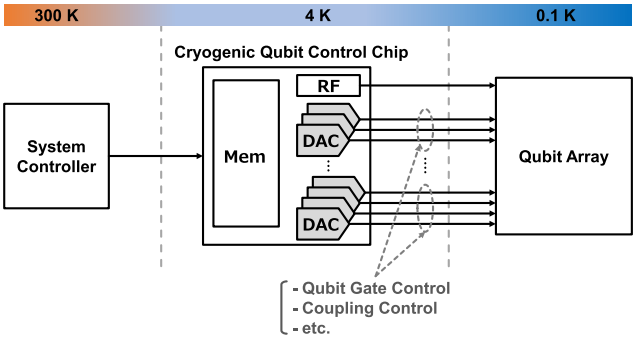

Fig. 1 Quantum computing system.

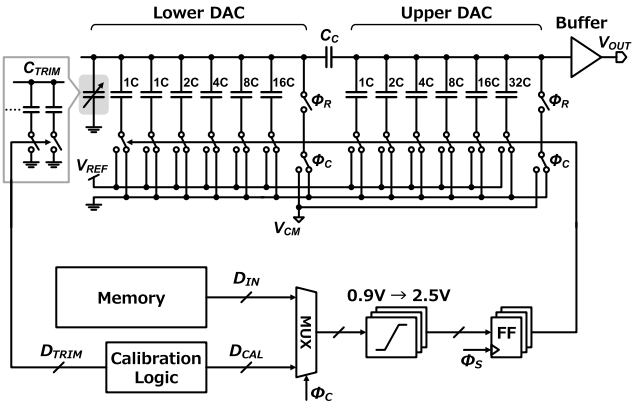

Fig. 2 Circuit diagram of cryogenic charge-redistribution DAC.

tum computers today, these qubits are directly controlled from outside the refrigerator. Considering the explosive increase in the number of qubits in a future quantum computing system, this conventional scheme will not be suitable since the huge number of control cables are needed. In such upcoming systems, the control circuits will also be placed inside the dilution refrigerator, as a cryogenic control chip, to control the qubits from a 4 K stage as shown in the simplified control diagram of Fig. 1. This enables to minimize the number of cablings from the outside since the system controller at room temperature only needs to interact with the memory in the cryogenic control chip by a serial interface protocol. The cryogenic qubit control chip generates various analog signals to manipulate, read out, and initialize qubits. They include many kinds of highly accurate bias voltages, such as the gate voltage to maintain the quantum state and the bias voltage to adjust the coupling strength among qubits. Thus, a large number of high-resolution DACs are required in the cryogenic control chip. This number will further increase with the scale of the qubit. Due to the limited budgets of area and power inside a dilution refrigerator, DACs are required to be compact size in physical dimensions as well as low power dissipation.

2.2 Charge-redistribution DAC architecture

The simplified circuit schematic of the cryogenic DAC is depicted in Fig. 2. It follows to a charge redistribution architecture with binary weighted capacitor arrays. Unlike current steering DACs, quiescent currents are negligible in such capacitive DACs, resulting in low power consumption [21, 22, 23, 24, 25, 26]. To decrease the total number of capacitors and minimize the layout area, the capacitor array is divided into 6-bit upper DAC and 5-bit lower DAC connected by a series capacitor C_C. This significantly reduces the total capacitance value of the capacitor array, however, a gain difference between the upper and the lower DACs occurs due to the capacitor mismatch and unexpected parasitic capacitance, degrading the linearity of the DAC output voltage [27, 28]. This error can be calibrated by trimming a variable capacitor C_{TRIM} provided in the lower DAC to equalize the gains among the lower and upper DACs. The mismatch calibration is automatically executed in a closed loop by an embedded calibration logic, which will be explained in detail in the next section.

The bias voltage generation scheme in normal operation starts from loading the corresponding 11-bit data stored in a memory to the DAC. The voltage levels of the data are shifted up from 0.9 V to 2.5 V, then, the data are latched by the flip-flops located near the bottom plate switches at the timing of sampling clock φ_S. This clock is enabled only when the bias voltage is changed, and the sampling rate is around several kHz in the bias control of quantum computing systems. Before the data loading, the top plate nodes of the both upper and lower capacitive DACs are preliminarily set to the ground level during the reset phase φ_R, and then the reset switches are opened. Thus, the bottom plate switching according to the latched 11-bit data generates the corresponding output voltage on the top plate node of the upper DAC, in a charge redistribution manner. The output voltage is buffered using an amplifier to drive heavy loads due to the long and narrow cablings in the dilution refrigerator.

The size of capacitors in a charge redistribution DAC is generally determined by considering thermal noise. In this case, the noise is applied at the reset phase as a sampling noise expressed with KT/C_{total}, where C_{total} is the total capacitance of the upper DAC. Since the temperature T is extremely small value, the size of unit capacitance can be reduced to 6 fF, contributing to small area and low current consumption during capacitor charging and discharging. However, such the small size of a unit capacitor induces two issues. One is a process mismatch of capacitors, which causes the degradation in linearity. Especially, the gain mismatch between the upper and lower DACs is a decisive factor. The error can be corrected according to its quantitative estimation through the calibration logic operated at the phase of φ_C, and deriving the calibration value D_{TRIM} as a size of trimming capacitor. This mismatch calibration will be provided in the next section. The other issue is a subthreshold leakage through the reset switches. This leakage causes a large variation in the output voltage as the capacitor size becomes smaller. However, the subthreshold current also has temperature characteristics, however, which becomes almost non-existent at the cryogenic temperature. Thus, the refresh frequency can be drastically suppressed, or the output voltages of the DAC can be maintained during the qubit operation.

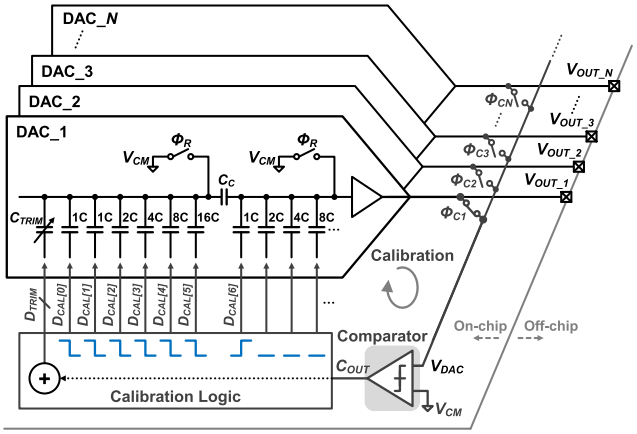

Fig. 3 DAC array with mismatch calibration circuit.

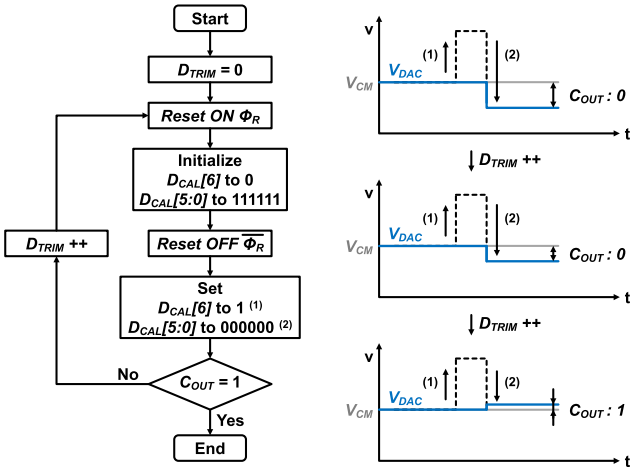

Fig. 4 Calibration scheme.

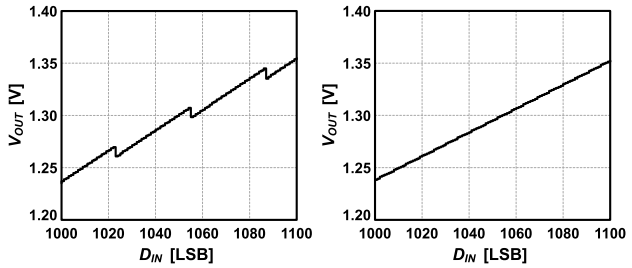

Fig. 5 Simulation results (a) before calibration, (b) after calibration.

3. Mismatch calibration for DAC array

The circuit diagram of the proposed capacitor mismatch calibration for DAC array is depicted in Fig. 3. Each output of the DAC array aligned in an N-parallel structure is connected to the respective IO pad, from V_{OUT_1} to V_{OUT_N}, and is also connected to the shared bus via the switches from φ_{C1} to φ_{CN}. The shared bus is input to the comparator for use in the calibration described later. By sharing one additional calibration circuit with N-parallel DACs, the overhead related to the calibration can be minimized. Each DAC is calibrated one by one in a time division way. In this example shown in the Fig. 3, DAC_1 is selected as the calibration target by turning on the connection switch with the shared bus φ_{C1} during the calibration period. Then, the control signals $D_{CAL}[6:0]$ from the calibration logic are given to the input of the DAC_1. The variable capacitance value D_{TRIM} is also controlled by the calibration logic. In this way, feeding the output voltage of the target DAC to the shared comparator and arbitrarily controlling the input to the DAC allows the execution of subsequent calibration sequences. It is noted that this mismatch calibration is performed once in the start-up sequence since capacitor mismatch is much less dependent on the temperature. Thus, the increase in the calibration time due to the time division will not be a big problem in this system.

After selecting the target DAC, the individual capacitor trimming process is executed according to the calibration scheme shown in Fig. 4. First of all, the control circuit sets D_{TRIM} to 0 to minimize the trimming capacitor C_{TRIM}, which is equivalent to maximizing the gain of the lower DAC. Then, the reset switch is closed at the phase of φ_R to give an intermediate potential V_{CM} to the top plate of the capacitors. At the same time, the control circuit initializes the LSB of the upper DAC $D_{CAL}[6]$ to 0, and all the inputs of the lower DAC $D_{CAL}[5:0]$ to 1. After releasing the reset switch, $D_{CAL}[6]$ is set to 1 and $D_{CAL}[5:0]$ are set to 0. These operations make the output voltage shift as shown in the right waveforms of Fig. 4. Initially, the gain of the lower DAC is greater than that of the upper DAC, thus, the output voltage of the DAC V_{DAC} becomes smaller than the original value V_{CM}. These two voltages are compared by the comparator, and the decision C_{OUT} in this case is 0. When the result of the comparator is 0, D_{TRIM} is incremented to decrease the gain of the lower DAC, and then the above control scheme is executed again. This process is repeated until C_{OUT} becomes 1 while incrementing the D_{TRIM}. In other words, when the voltage shift by moving the LSB of the upper DAC from 0 to 1 and by changing all the bits of the lower DAC from 1 to 0 are almost equal as shown in the bottom right waveform in Fig. 4, the gain mismatch between upper and lower DACs is eliminated.

The simulation results of the proposed calibration are shown in Fig. 5. With a mismatch, nonlinear gaps are clearly seen at every 32-LSB on the output line, which correspond to the associated switching points from the lower DAC to the upper DAC as shown in Fig. 5(a). After the calibration, the gaps are compensated as shown in Fig. 5(b), improving the non-linearity error.

In order to complete the mismatch calibration accurately, the offset of the comparator must be removed beforehand. The offset error of the comparator leaves a gain error between the upper and lower DACs. In this design, the comparator offset is eliminated by adjusting the output load as described in [29]. The comparator circuit is designed in the double-tail latch architecture that can minimize noise and also reduce dynamic power [30].

4. Measurement results

The proposed cryogenic DAC was implemented in 40 nm 1P10M CMOS process. The photo of the prototype chip

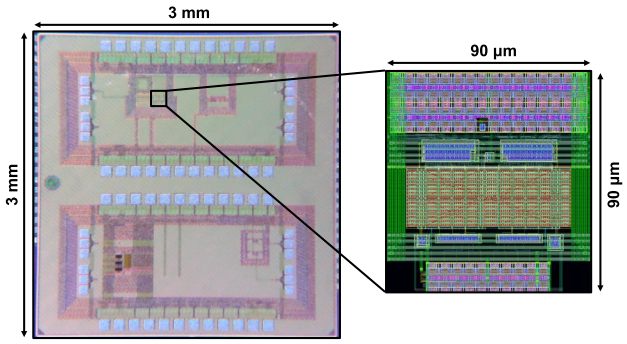

Fig. 6 Prototype chip photo and DAC layout.

and the DAC core layout are shown in Fig. 6. The chip size is 3 mm × 3 mm, and the IO pads are placed for direct contacts with a multipin probe and a ground-signal-ground (GSG) type probe on a probing station. The DAC core is only 90 µm × 90 µm thanks to the compact architecture with small unit capacitor. The charge-redistribution capacitors are composed of metal-oxide-metal capacitors using multiple metal layers, occupying approximately 30% of the total area. The other area is mainly filled with the voltage level shifters from 0.9 V to 2.5 V. The chip also has some register banks for storing digital input data and associated serial-parallel interface circuits.

The evaluation was performed using a cryogenic probing station that could be set to any temperature from 300 K to 8 K. The prototype DAC chip is placed in a cryogenic chamber, and an external FPGA at room temperature controls input data and reset trigger by serially accessing the internal register banks, then, the output voltage is acquired with an oscilloscope via micro-probe.

The measured input-output characteristics at room temperature (300 K) and cryogenic temperature (8 K) are shown in Fig. 7(a) and Fig. 7(b), respectively. The output voltages are properly generated in both conditions across the entire input range. The linearity of the DAC output was also measured as shown in Fig. 8. In both temperature conditions of 300 K as in Fig. 8(a) and 8 K as in Fig. 8(b), respectively, the characteristics of INL and DNL are quite similar since the linearity degradation is caused by a capacitor mismatch which is not temperature dependent. Fortunately, this particular sample exhibited relatively smaller mismatches, and thus, experienced no much change in INL and DNL before and after applying the proposed calibration. However, we believe the calibration technique will definitely be effective if the resolution of the DAC is increased necessarily toward the future quantum computing systems with the large number of qubits. In this prototype, the measured INL is +/−2 LSB and the DNL is from −2 LSB to +0.5 LSB after the calibration.

The leakage characteristics of the DAC were measured by monitoring output voltage fluctuations over time as shown in Fig. 9. At room temperature, the voltage drop is immediately seen after setting the voltage. This drop is caused by the leakage current through the channel of MOS switches for a reset operation. However, the cooling of only 50 degrees eliminates the apparent voltage drop within a second, which indicates the DAC does not need to be refreshed during a

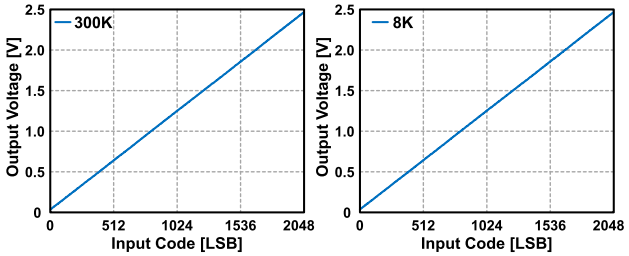

Fig. 7 Measured DAC output at (a) room temperature (b) 8 K.

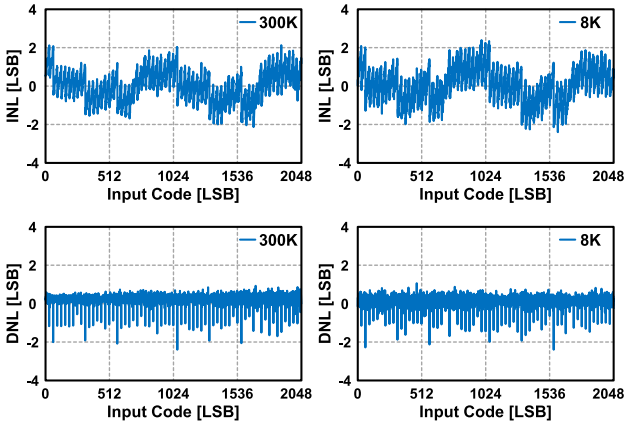

Fig. 8 Measured INL and DNL at (a) room temperature and (b) 8 K.

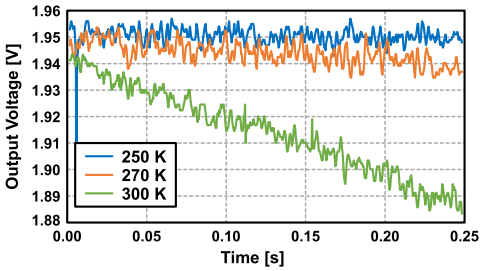

Fig. 9 Measured leakage.

single quantum operation since the coherence time of a qubit is generally shorter than the voltage sustainable time of the DAC.

The performance summary of the prototype cryogenic DAC and its comparison with the state-of-the-art cryogenic DACs are shown in Table I. The power consumption of the DAC is 5.8 µW at a sampling rate of 3.9 kHz. Since the power consumption of the charge redistribution DAC highly depends on the sampling rate, the power was measured at the same frequency as the refresh rate of the other charge redistribution type [20] for a fair comparison. The breakdown of power consumption is 5.7 µW for digital circuit (0.9 V), 0.1 µW for analog circuit (2.5 V), and 20 nW for charging and discharging the capacitors. From the comparison table, our proposed DAC achieved the smallest area and competitively low power consumption among the other state-of-the-art cryogenic DACs, which proves it can be effectively used as the bias voltage generation DAC for qubit control implemented on the limited resources in a dilution refrigerator.

Table I Performance comparison.

	This work	SSC-L 2020 [20]	SSC-L 2020 [18]	T-CAS II 2017 [19]
Technology	40 nm CMOS	65 nm CMOS	28 nm FDSOI	0.5 µm SOS
Architecture	Charge Redistribution	Charge Redistribution	Current Steering	Current Steering
Temperature	8 K	6 K	4.2 K	4.2 K
Supply	2.5 / 0.9 V	2.5 / 1.2 V	1.8 / 1 V	3 V
Resolution	11-bit	13-bit	8-bit	6-bit
Sampling Rate	3.9 kHz	3.9 kHz	100 MHz (Estimated)	-
Power	5.8 µW	2.6 µW	7 µW (Static)	3.1 mW
Area	0.008 mm^2	0.0175 mm^2	0.04 mm^2	0.012 mm^2

5. Conclusion

In this letter, the compact DAC for bias voltage generation in a quantum computing system has been described. It will be operated at cryogenic temperature in a dilution refrigerator, and meet the requirements of small area and low power consumption. The capacitive DAC architecture without static current is considered, and the total area is suppressed by using small unit capacitors thanks to low noise and low leakage at cryogenic temperature. Moreover, an auto-calibration technique is also proposed to compensate the nonlinearity error due to the capacitor mismatches. This only needs one comparator and associated small calibration logics, resulting in low area overhead. The simulation results prove that the calibration effectively eliminates the mismatch errors. The DAC was fabricated in 40 nm process and evaluated at 8 K temperature using a cryogenic probe station. The measurement results prove the cryogenic DAC achieves INL and DNL of less than $+/-2$ LSB with compact layout area of 0.008 mm^2 and low power dissipation of 5.8 µW, which is applicable to the control circuit for large-scale qubit arrays.

Acknowledgments

This work was supported by JST [Moonshot R&D] [Grant Number JPMJMS2065].

References

[1] F. Arute, *et al.*: "Quantum supremacy using a programmable superconducting processor," Nature **574** (2019) 505 (DOI: 10.1038/s41586-019-1666-5).
[2] A.Y. Kitaev: "Fault-tolerant quantum computation by anyons," arXiv (1997) quant-ph. 9707021v1 (DOI: 10.1016/S0003-4916(02)00018-0).
[3] P.W. Shor: "Scheme for reducing decoherence in quantum computer memory," Phys. Rev. A **52** (1995) R2493 (DOI: 10.1103/PhysRevA.52.R2493).
[4] N. Lee, *et al.*: "Enhancing electrostatic coupling in silicon quantum dot array by dual gate oxide thickness for large-scale integration," Appl. Phys. Lett. **116** (2020) 162106 (DOI: 10.1063/1.5141522).
[5] A. Noiri, *et al.*: "Coherent electron-spin-resonance manipulation of three individual spins in a triple quantum dot," Appl. Phys. Lett. **108** (2016) 153101 (DOI: 10.1063/1.4945592).
[6] R. Brunner, *et al.*: "Two-qubit gate of combined single-spin rotation and interdot spin exchange in a double quantum dot," Phys. Rev. Lett. **107** (2011) 146801 (DOI: 10.1103/PhysRevLett.107.146801).
[7] T. Nakajima, *et al.*: "Robust single-shot spin measurement with 99.5% fidelity in a quantum dot array," Phys. Rev. Lett. **119** (2017) 017701 (DOI: 10.1103/PhysRevLett.119.017701).
[8] J. Yoneda, *et al.*, "A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%," Nat. Nanotech. **13** (2018) 102 (DOI: 10.1038/s41565-017-0014-x).
[9] A. Nersisyan, *et al.*: "Manufacturing low dissipation superconducting quantum processors," IEDM Tech. Dig. (2019) (DOI: 10.1109/IEDM19573.2019.8993458).
[10] S. Krinner, *et al.*: "Engineering cryogenic setups for 100-qubit scale superconducting circuit systems," EPJ Quantum Technology **6** (2019) 2 (DOI: 10.1140/epjqt/s40507-019-0072-0).
[11] J.I. Colless and D.J. Reilly: "Modular cryogenic interconnects for multi-qubit devices," Rev. Sci. Instrum. **85** (2014) 114706 (DOI: 10.1063/1.4900948).
[12] D.J. Reilly: "Engineering the quantum-classical interface of solid-state qubits," NPJ Quantum Information **1** (2015) 15011 (DOI: 10.1038/npjqi.2015.11).
[13] X. Xue, *et al.*: "CMOS-based cryogenic control of silicon quantum circuits," Nature **593** (2021) 205 (DOI: 10.1038/s41586-021-03469-4).
[14] B. Patra, *et al.*: "Cryo-CMOS circuits and systems for quantum computing applications," IEEE J. Solid-State Circuits **53** (2018) 309 (DOI: 10.1109/JSSC.2017.2737549).
[15] J.C. Bardin, *et al.*: "Design and characterization of a 28-nm bulk-CMOS cryogenic quantum controller dissipating less than 2 mW at 3 K," IEEE J. Solid-State Circuits **54** (2019) 3043 (DOI: 10.1109/JSSC.2019.2937234).
[16] L. Le Guevel, *et al.*: "A 110 mK 295 uW 28 nm FDSOI CMOS quantum integrated circuit with a 2.8 GHz excitation and nA current sensing of an on-chip double quantum dot," ISSCC Dig. Tech. Papers (2020) 306 (DOI: 10.1109/ISSCC19947.2020.9063090).
[17] J.P.G. Van Dijk, *et al.*: "A scalable cryo-CMOS controller for the wideband frequency-multiplexed control of spin qubits and transmons," IEEE J. Solid-State Circuits **55** (2020) 2930 (DOI: 10.1109/JSSC.2020.3024678).
[18] M.E.P.V. Zurita, *et al.*: "Cryogenic current steering DAC with mitigated variability," IEEE Solid-State Circuits Lett. **3** (2020) 254 (DOI: 10.1109/LSSC.2020.3013443).
[19] M.T. Rahman and T. Lehmann: "A self-calibrated cryogenic current cell for 4.2 K current steering D/A converters," IEEE Trans. Circuits Syst. II, Exp. Briefs **64** (2017) 1152 (DOI: 10.1109/TCSII.2016.2631489).
[20] P. Vliex, *et al.*: "Bias voltage DAC operating at cryogenic temperatures for solid-state qubit applications," IEEE Solid-State Circuits Lett. **3** (2020) 218 (DOI: 10.1109/LSSC.2020.3011576).
[21] J. McCreary and P.R. Gray: "All-MOS charge redistribution analog-to-digital conversion techniques — Part I," IEEE J. Solid-State Circuits **10** (1975) 371 (DOI: 10.1109/JSSC.1975.1050629).
[22] M. van Elzakker, *et al.*, "A 10-bit charge-redistribution ADC consuming 1.9 uW at 1 MS/s," IEEE J. Solid-State Circuits **45** (2010) 1007 (DOI: 10.1109/JSSC.2010.2043893).
[23] B.P. Ginsburg and A.P. Chandrakasan: "500-MS/s 5-bit ADC in 65-nm CMOS with split capacitor array DAC," IEEE J. Solid-State Circuits **42** (2007) 739 (DOI: 10.1109/JSSC.2007.892169).
[24] T. Miki, *et al.*: "A 4.2 mW 50 MS/s 13 bit CMOS SAR ADC with SNR and SFDR enhancement techniques," IEEE J. Solid-State Circuits **50** (2015) 1372 (DOI: 10.1109/JSSC.2015.2417803).
[25] C. Liu, *et al.*: "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," IEEE J. Solid-State Circuits **45** (2010) 731 (DOI: 10.1109/JSSC.2010.2042254).
[26] T. Yousefi, *et al.*: "An energy-efficient DAC switching method for SAR ADCs," IEEE Trans. Circuits Syst. II, Exp. Briefs **65** (2018) 41 (DOI: 10.1109/TCSII.2017.2676048).
[27] J.A. Fredenburg and M.P. Flynn: "Statistical analysis of ENOB and yield in binary weighted ADCs and DACs with random element mismatch," IEEE Trans. Circuits Syst. I, Reg. Papers **59** (2012) 1396 (DOI: 10.1109/TCSI.2011.2177006).
[28] T. Miki, *et al.*: "A 2-GS/s 8-bit time-interleaved SAR ADC for

millimeter-wave pulsed radar baseband SoC," IEEE J. Solid-State Circuits **52** (2017) 2712 (DOI: 10.1109/JSSC.2017.2732732).

[29] M. Miyahara, *et al.*: "A low-noise self-calibrating dynamic comparator for high-speed ADCs," A-SSCC Dig. (2008) 269 (DOI: 10.1109/ASSCC.2008.4708780).

[30] D. Schinkel, *et al.*: "A double-tail latch-type voltage sense amplifier with 18 ps setup+hold time," ISSCC Dig. Tech. Papers (2007) 314 (DOI: 10.1109/ISSCC.2007.373420).