A Study on Circuit Design for Low-Voltage and Soft-Error Resilient SRAM in Nanometer CMOS Technology

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A Study on Circuit Design for Low-Voltage and Soft-Error Resilient SRAM in Nanometer CMOS Technology

（ナノメートル CMOS における低電圧・耐ソフトエラーSRAM に向けた回路設計技術に関する研究）

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Abstract

This dissertation reports robust circuit designs for low-voltage, low-power, and soft-error resilient SRAM in nanometer CMOS technology.

Chapter 1 presents the background of the dissertation and basic characteristics for the SRAM. The soft-error mechanism is also explained in the chapter.

In Chapter 2, intrinsic issues related to the nanometer CMOS technology are presented: decreased operating margin in a read and write cycle, energy dissipation induced by bitline swing variation, and decreased critical charge incurring soft error. The issues are considered for robust SRAM design. This dissertation presents robust circuit designs in Chapter 3 – Chapter 6 to address issues related to the nanometer CMOS technology.

Chapter 3 describes two disturb-tolerant 8T SRAM designs: 1) a dual write wordline 8T cell with a sequential writing technique and 2) a low-power disturb mitigation scheme.

1) The dual write wordline 8T SRAM mitigates disturb (half-select) problems in a write cycle. The 8T SRAM cell has two write wordlines, which are activated sequentially in a write cycle. The cell's combination with the half-VDD precharge suppresses the half-select problem. We implemented a 256-Kb DW8T SRAM and a half-VDD generator with a 40-nm CMOS process. The measurement results obtained for the seven samples show that the proposed 8T SRAM improves the average VDD_{min} by 367 mV compared to the conventional 8T SRAM.
2) The proposed low-power disturb mitigation scheme reduces the power overhead of a general write-back scheme for low-voltage 8T SRAM using a floating write bitline technique and a low-swing bitline driver (LSBD). The LSBD consists only of nMOSes, which pull up and down write bitlines in unselected columns. The pulled up bitline goes up to VDD - V_{thn}. The suppressed bitline swing reduces the write-back power consumption. A test chip with the proposed scheme is implemented. Measurement results show 1.52-μW/MHz writing active energy and 72.8-μW leakage power, which are 59.4% and 26.0% better than those of the conventional write-back scheme.

Chapter 4 presents two techniques to limit bitline swings for low-power 8T SRAM: 1) a read bitline amplitude limiting circuit and 2) a selective source line control scheme with an address preset structure.

1) The read-bitline amplitude limiting (RBAL) scheme suppresses dynamic energy dissipation to charge the read bitlines. The RBAL consists of an nMOS switch that is inserted between a source line and which is grounded in the dedicated read port. In addition, a discharge acceleration (DA) circuit is proposed to decrease the delay overhead of RBAL. The proposed scheme improves the active energy dissipation in a read cycle by 22% at the center–center corner and 25°C. The maximum delay overhead is 32% at the fast–slow corner and -40°C.
2) The selective source line control (SSLC) scheme reduces a read bitline voltage swing in an unselected column with a floating source line (SL) of dedicated read ports. Furthermore, an address preset structure is presented for a successive readout operation. The preset address enables the SRAM to be read out with no access time penalty for preferred use of the SSLC scheme. We observed that the proposed SSLC scheme with the address preset structure saves 38.1% of the readout power of a test chip, on average.

In Chapter 5, two margin-enhancement techniques are explained for the bit-error and soft-error tolerant SRAM design: 1) a bit-error and soft-error resilient 7T/14T SRAM and 2) soft-error resilient 8T bitcell with divided wordline structure.

1) Reliability of the 7T/14T SRAM can be changed dynamically using a control signal depending on an operating condition and application. The 14T dependable mode allocates one bit in a 14T cell and simultaneously improves the bit-error rate (BER) in a read operation and the soft-error rate (SER) in a retention state. In our measurements, the minimum operating voltage was improved by 100 mV, the alpha-induced SER was suppressed by 80.0%, and the neutron-induced SER was decreased by 34.4% in the 14T dependable mode over the 7T normal mode.
2) The soft-error tolerant 8T SRAM cell layout is presented to mitigate multiple-bit upset (MBU) in a divided wordline structure. In the 8T cell array, horizontally adjacent latches are separated completely by a p-substrate of the dedicated read ports. The MBU in the proposed 8T SRAM is improved by 90.70% and the MBU SER is decreased to 3.46 FIT / Mb at 0.9 V when single-error correction

and double-error detection (SEC-DED) ECC are implemented. The proposed 8T SRAM array has a 48% area overhead over the conventional 6T SRAM. However, the minimum operation voltage can be improved by 0.45 V. Therefore, the operation power is decreased by 77.2%.

Chapter 6 describes a soft-error simulator and two multiple-bit-upset tolerant 6T bitcell layouts: 1) a neutron-induced soft-error simulator using a particle transport code (PHITS), 2) an nMOS-inside 6T cell layout, and 3) an nMOS–pMOS reversed 6T cell layout.

1) The proposed soft-error simulation tool can calculate the SER according to various data patterns and the layout structure of the memory cells in an SRAM. Additionally, the tool distinguishes a single-event-upset (SEU) SER, a horizontal multiple-cell-upset (MCU) SER, and a vertical MCU SER using an extraction function. We evaluated the following layouts using the estimation tool.
2) The nMOS-centered 6T SRAM cell layout reduces a neutron-induced MCU SER on the same wordline. We implemented a 1-Mb SRAM macro in a 65-nm CMOS process and irradiated neutrons as a neutron-accelerated test to evaluate the MCU SER. The proposed 6T SRAM macro improves the horizontal MCU SER by 67–98% compared with a general macro that has pMOS-centered 6T SRAM cells.
3) The proposed nMOS-pMOS reversed 6T cell leverages pMOS characteristics of smaller dopant variation and larger saturation current than that of nMOS in the advanced process. In 22-nm node, the static-noise margin and the saturation current of the proposed cell are enhanced respectively by factors of 2.04 and 2.81. The 6T cell also improves the single-bit-upset and multiple-cell-upset soft-error rates by 11–51% and 34–70%, respectively, because the proposed n-p reversed cell has a 33% smaller nMOS diffusion than the conventional one and reduces a collected charge induced by a secondary ion.

Finally, Chapter 7 concludes this dissertation. This thesis presents low-voltage, low-power, and soft-error tolerant SRAM designs. The work contributes to achievement of an energy-efficient and robust SRAM design for the advanced technology.

Keywords: SRAM, Low power, Soft Error, Single event upset, Multiple cell upset, Multiple bit upset, 6T cell, 8T cell, 7T/14T cell, divided wordline structure.

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Chapter 1 Introduction

1.1 Background of Research Area

Process technology has been scaled down continuously, reflecting Moore's law [1]. Process scaling has integrated more transistors to enhance the functionality of SoCs. As shown in Fig. 1.1, the International Technology Roadmap for Semiconductor (ITRS) predicts that the number of processing engines and total memory size in a mobile SoC are likely to increase by a factor of 18 during 2013–2025 [2]. Hugely integrated transistors will probably expand dynamic and static power consumption and decrease mobile battery life. The greater energy dissipation is expected to limit the usefulness of wireless applications such as biomedical sensors, on-field monitoring, and smart mobile devices.

Soft error, an important reliability issue in a scaled process, is a temporary error incurred by radiation strikes to a semiconductor device [3]. Several researchers have reported that cosmic ray neutrons have strongly affected the total soft-error rate (SER) of SoCs [4–6]. If a neutron becomes incident on a chip and collides with the silicon nucleus, then some secondary ions are generated by the nucleus reaction, as shown in Fig. 1.2. The circuit becomes upset if the ions deposit charges to a latch circuit over a critical threshold (= critical charge). Therefore, process scaling has important effects on the total SER because of the decreased critical charge and the shortened transistor pitches.

Static Random Access Memory (SRAM), the most common type of embedded memory for modern SoCs, has better compatibility with logic circuits and faster random access than other memories have. Processors leverage the SRAM as cache memory, scratch pad memory, and main memory for use with a general CPU, video coding, and speech recognition. As the process technology is scaled down, SRAM occupies more than 50% of the total area and 65% of the total power in 2022 [2]. Figure 1.3 shows a trend of logic and memory supply voltages: standard operating voltages of processors and minimum operating voltages of memories. The standard operating voltage decreases with process scaling. However, the minimum operating voltage of SRAM increases because of process variation [7]. SRAM cells are generally designed with the

minimum feature size in each process so that SRAM is the most sensitive device to the transistor variation [8]. Moreover, process scaling increases the SER of SRAM because of its large capacity. A recent report described that the SER per device in 22-nm node is expected to be increased by seven times compared to that in 130-nm and that the multiple cell upset (MCU) ratio to the total SER will become as high as 46% for 22 nm [9].

Consequently, SRAM presents imperative issues of energy dissipation, minimum operating voltage, and soft-error effects that must be resolved for nanometer-scale CMOS technology.

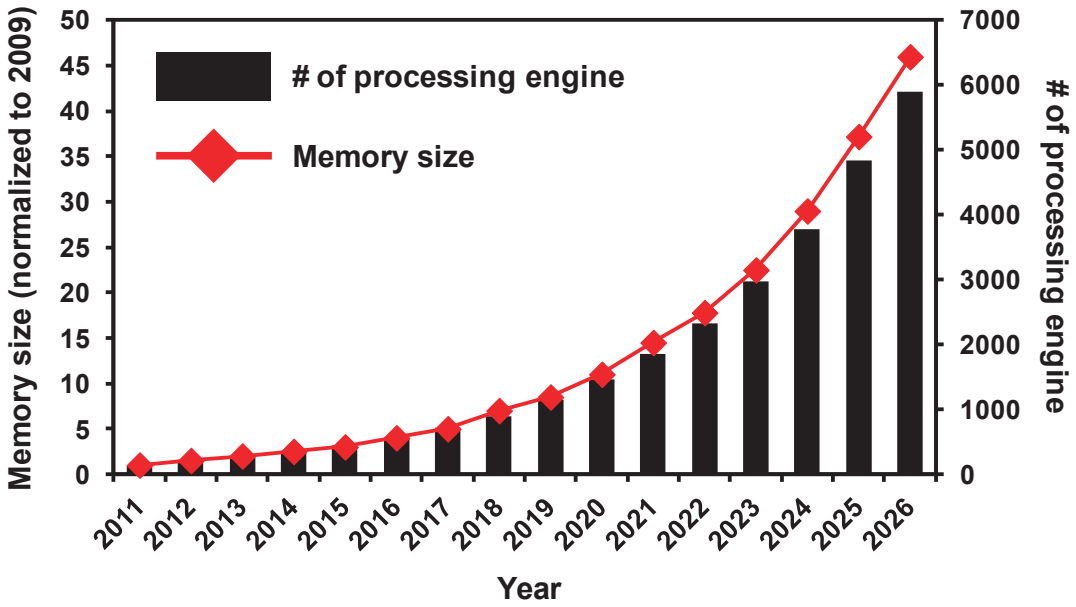


Fig. 1.1 Trend of total memory size and the number of processing engines in a mobile SoC as predicted by ITRS 2011 [2].

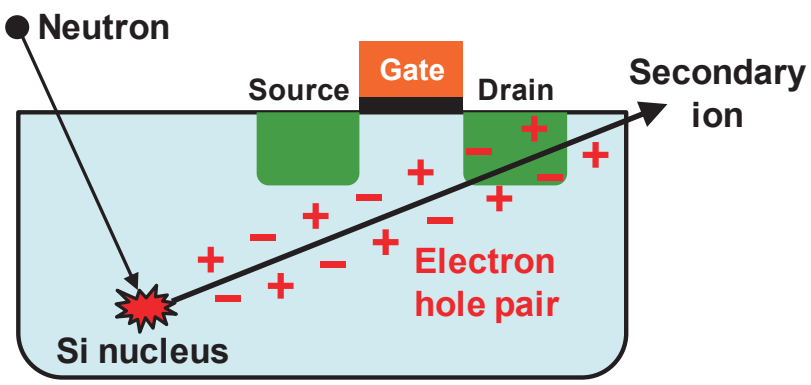


Fig. 1.2 Secondary ion generated by nucleus reaction of a silicon nucleus and a cosmic ray neutron.

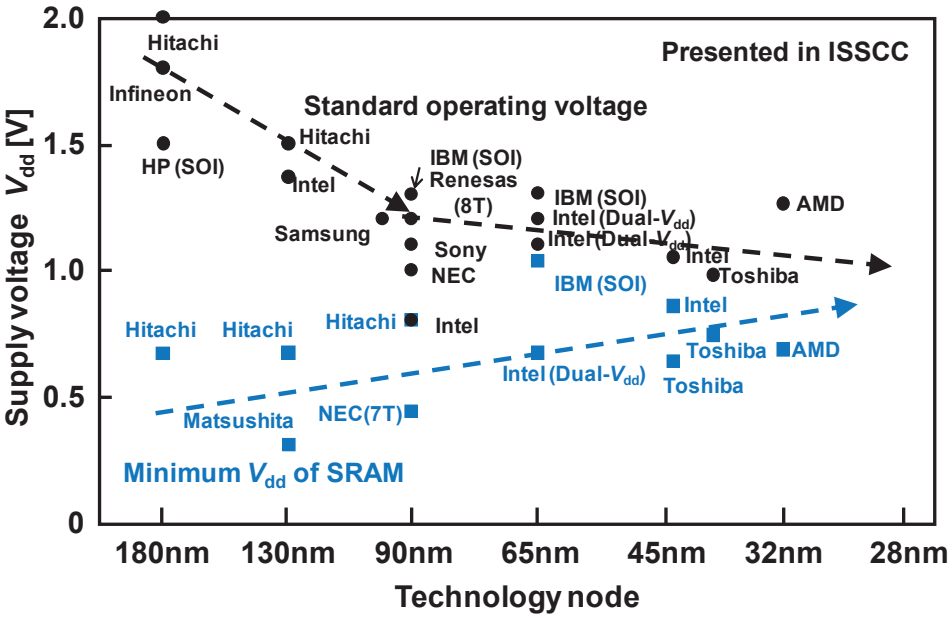


Fig. 1.3 Trend of supply voltage of processor and static random access memory presented in ISSCC.

1.2 Objective of This Study

This dissertation specifically examines robust circuit design for low voltage, low power, and soft-error resilient SRAM.

The first objective of this study is to enhance operating margins in write and read operations. The operating margins are degraded significantly because of the process variations, especially with low-voltage operation. This dissertation uses six transistors (6T), 8T, and 7T/14T transistors and presents margin enhancement techniques for SRAMs.

The second objective is to improve the energy efficiency of low-voltage operation. As described above, voltage scaling becomes difficult in the scaled process. This paper presents a low-swing write-back scheme and bitline swing limiting technique to improve energy efficiency.

The third objective is to decrease the single-bit-upset (SBU) and multiple-bit-upset (MBU) soft-error rate of SRAM. Process scaling decreases the critical charge and transistor pitch, which degrades SBU immunity and which increases the MBU ratio to the total SER. This presentation of the study describes the soft-error tolerant 14T cell

and MBU-hardened layouts for 6T and 8T SRAMs.

1.3 Overview of This Dissertation

Figure 1.4 presents an overview of this dissertation. First, the background, objectives, and overview of this study are explained in Chapter 1. Second, issues of SRAM in nanometer CMOS technology are presented in Chapter 2: decreased operating margins in the low voltage region, degraded energy efficiency, and poor soft-error immunity. This dissertation presents novel techniques to address the issues described in Chapters 3–6.

Chapter 3 explains two half-select tolerant 8T SRAM designs. First, a proposed dual write wordline 8T SRAM leverages a sequential writing technique with a half-VDD precharged bitline. The proposed scheme enhances the half-select disturb margin in the unselected column and improves the minimum operating voltage of 8T SRAM. Second, a disturb-mitigating scheme is presented for 8T SRAM. The proposed scheme decreases write-back dynamic energy and leakage energy using a low-swing bitline driver and a precharge-less equalizer. The bitline driver consists solely of nMOSes, which suppress the write bitline swing but which do not degrade the disturb margin of 8T SRAM cells.

In Chapter 4, two bitline swing-limiting techniques are proposed for low-power 8T SRAM. First, the read-bitline amplitude limiting (RBAL) scheme is presented to limit the bitline swing in faster cells. A gate of the limiter (nMOS transistor) is connected to the read bitline and becomes a cut-off state when the bitline level decreases. A discharge acceleration technique is also proposed to decrease the access time penalty of the RBAL scheme. Second, a selective source line control (SSLC) technique is introduced to reduce the read bitline swing in unselected columns. The source line is shared by dedicated read ports of 8T cell arrays in a column and is selectively floated using nMOS switches. The floated source lines suppress the read bitline swing in a successive readout operation.

Chapter 5 introduces two margin enhancement techniques for bit-error and soft-error tolerant SRAM. First, 7T/14T SRAM is presented with 3-D device simulation, neutron accelerated measurement results. The 14T dependable mode has bit-error and soft-error immunity because of compensating current through control transistors. Second, a latch-separated 8T bitcell layout is proposed for low-voltage SRAM with a divided

wordline structure. Horizontally adjacent latches of SRAM are separated completely by a p-substrate, which improves multiple-bit-upset SER. The proposed 8T SRAM with a divided wordline structure simultaneously improves the bit-error rate and soft-error rate.

Chapter 6 presents a neutron-induced soft-error simulator and two multiple-bit-upset tolerant 6T cell layouts. First, the soft-error simulator is developed for analysis and evaluation of the soft-error rate of SRAM using a particle transport code (PHITS) [10]. The soft-error simulator evaluates 3-D SRAM cell structures and data patterns to optimize the soft-error resilient SRAM design. Second, an nMOS-centered 6T cell layout is presented to mitigate multiple-bit-upset soft-error rate. Generally, the nMOS is four times more sensitive than pMOS. The horizontally adjacent nMOSes are separated by n-wells so that the multiple-bit-upset immunity is improved. Third, an nMOS-pMOS reversed 6T SRAM cell is proposed. Process scaling increases the pMOS saturation current. The current ratio of I_{pMOS} to I_{nMOS} is almost one. The 6T cell has a larger operating margin and improved soft-error immunity leveraging the pMOS.

Finally, the conclusion of this dissertation is presented in Chapter 7. The work presents robust circuit design for low voltage, low power, and soft-error resilient SRAM using nanometer CMOS technology.

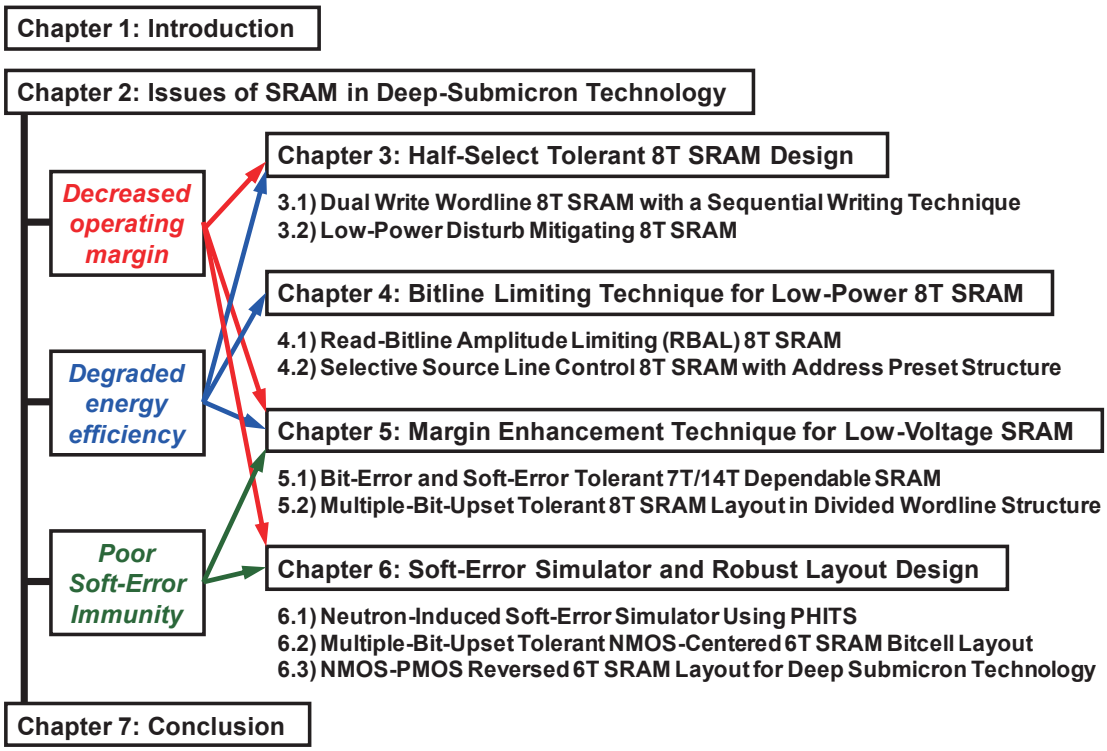


Fig. 1.4 Overview of this dissertation.

Chapter 2 Issues of SRAM in Nanometer CMOS Technology

This chapter presents a summary of issues of SRAM in nanometer CMOS technology: decreased operating margin, degraded energy efficiency, and poor soft-error immunity.

First, the decreased operating margins in read and write cycles are introduced. General 6T and 8T SRAM cells are also presented. Second, degraded energy efficiency is introduced. Because the process variation and swing variation increase energy efficiency, the bitline swing is varied. Third, poor soft-error immunity in the scaled process is introduced. Process-scaling and voltage-scaling decrease the critical charge of the SRAM cell. In addition, cosmic rays simultaneously affect several cells because of the shortened transistor pitch.

2.1 Decreased Operating Margin

2.1.1 6 Transistor (6T), 8T SRAM Cells and Block Diagram

Figure 2.1 presents a general 6T SRAM cell. The 6T cell consists of pMOS load transistors (PL0 and PL1), nMOS access transistors (NA0 and NA1), and nMOS driver transistors (ND0 and ND1). Wordlines (WLs) and bitline pairs (BLs and BLNs) are respectively aligned in horizontal and vertical directions. The BLs are precharged to VDD in a standby state and a WL is activated in a write or read cycle. The WL is shared in each cycle. Therefore, designing a 6T SRAM cell has been more difficult: both read and write margins must be considered [11].

An 8T SRAM cell consists of the 6T cell and a dedicated read port, as shown in Fig. 2.2 [12]. The dedicated read port comprises an nMOS read access transistor (NRA) and a read driver transistor (NRD), which provide disturb-free read operation. Furthermore, the read and write circuits can be optimized. Therefore, the 8T cell, in which only the write margin must be considered, is expected to be a smaller layout and to be less expensive than the 6T cell in the scaled process [13].

Figure 2.3 shows the SRAM block diagram. Row and column addresses respectively select a WL and a BL pair. In the read cycle, sense amplifiers read the voltage difference

between BL and BLN and the SRAM outputs the readout data. In the write cycle, BL and BLN are forced to (VDD, GND) or (GND, VDD) by write drivers according to input data.

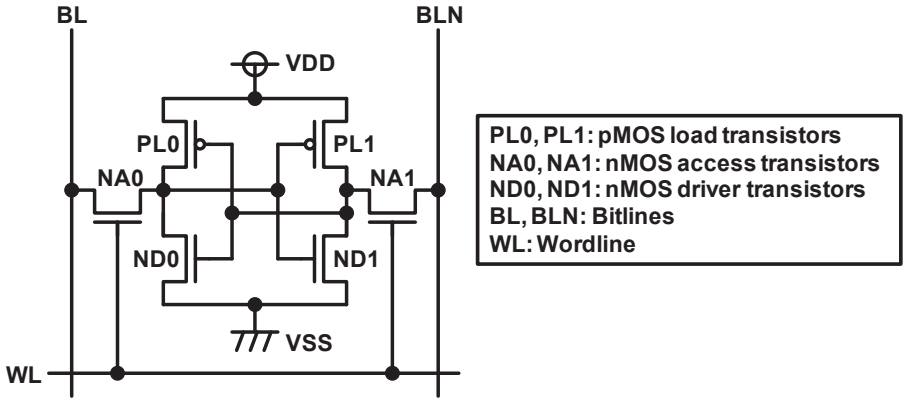


Fig. 2.1 6T SRAM cell circuit diagram.

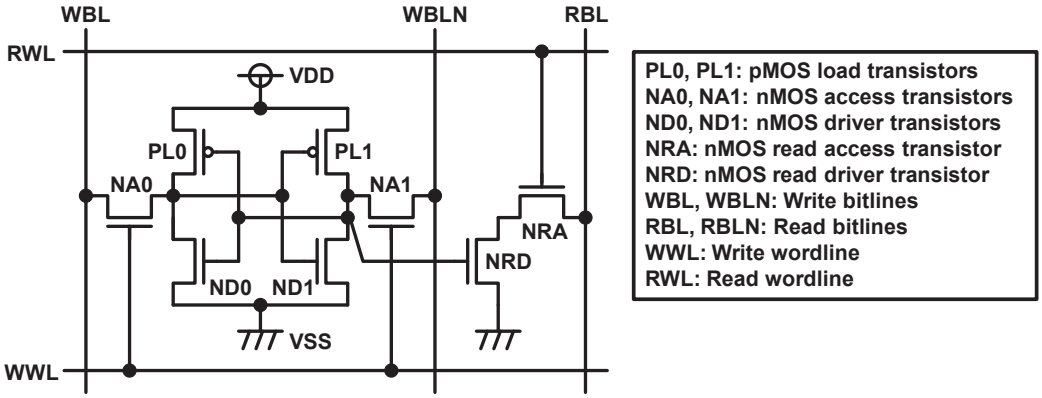


Fig. 2.2 8T SRAM cell circuit diagram.

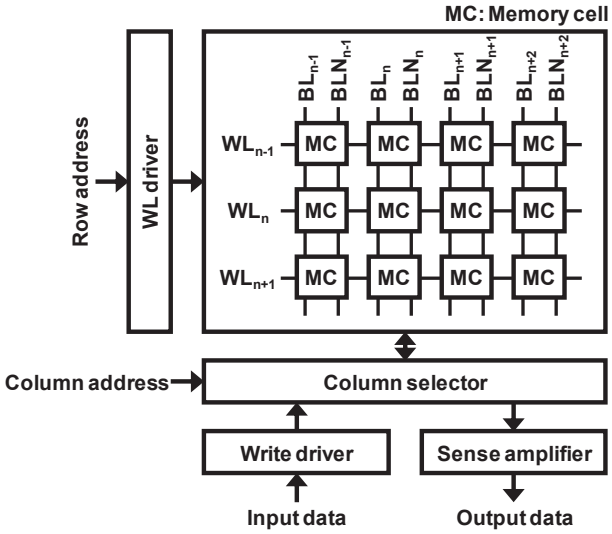


Fig. 2.3 SRAM block diagram.

2.1.2 Read Margin and Write Margin

Figures 2.4(a) and 2.4(b) respectively depict circuit setups for read margin calculation and static noise margin (SNM) definition [14]. The SNM is described as the maximum size square that can be nested into the cross-coupled voltage transfer characteristics. The read margin in the 6T cell correlates with a logical V_{th} of the inverter latches, and is inversely related to the minimum output voltage of the inverter (V_{MO} in Fig. 2.4(b)) [15]. If the access transistor width is increased, then V_{MO} becomes larger, which necessarily reflects a smaller read margin. The β ratio, the size ratio of a driver transistor and an access transistor, must be increased to ensure the SNM.

Figures 2.5(a) and 2.5(b) respectively portray the circuit setup for write margin calculation and write trip point (WTP) definition [16]. When the WL and BLN are forced to VDD, the BL is pulled down from VDD to GND. The WTP is defined with the BL voltage in the flipped point. The WTP also correlates to the logical Vth of the inverter latches and a γ ratio (a size ratio of an access transistor and a load transistor).

The β and γ ratios are also important design factors for the other read and write margin metrics [17, 18].

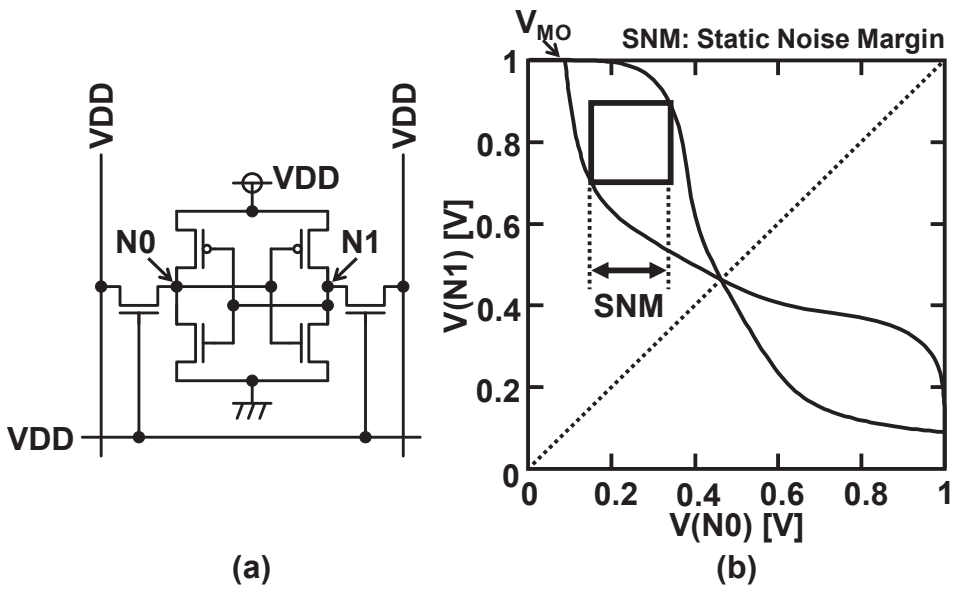


Fig. 2.4 (a) Circuit setup for read margin calculation and (b) static noise margin (SNM) as the read margin.

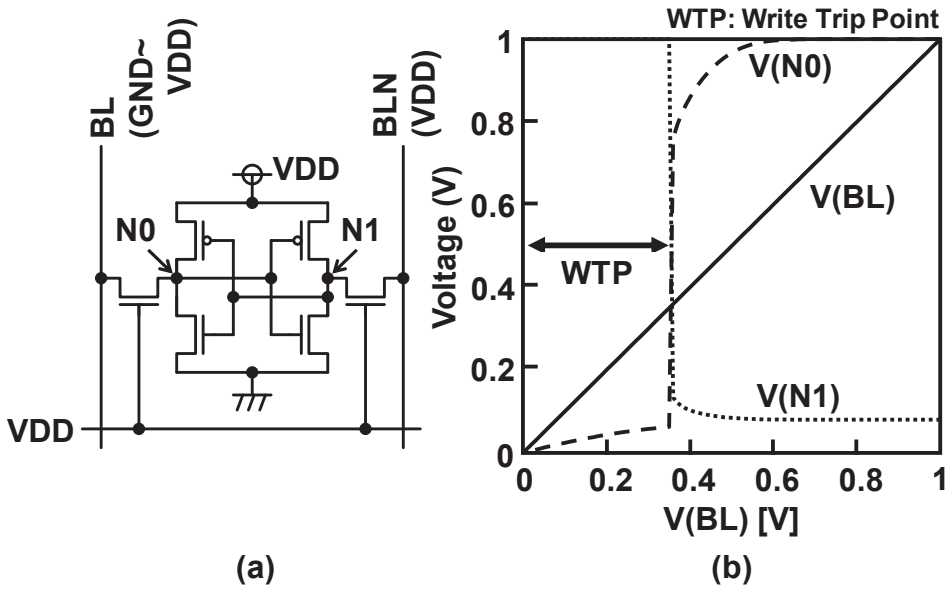


Fig. 2.5 (a) Circuit setup for write margin calculation and (b) write trip point (WTP) as the write margin.

2.1.3 Systematic and Random Threshold Voltage Variation

Figure 2.6 shows the systematic and random threshold voltage (V_{th}) variation of transistors. Systematic variation is inter-die (chip-to-chip) variation. Random variation is intra-die (transistor-to-transistor) variation.

Figure 2.7 presents a milky-way plot and five process corners (FF, FS, CC, SF, SS) with read and write limits [19]. The read margin is decreased at nMOS-fast and pMOS-slow (FS) corner and the write margin is decreased at the nMOS-slow and pMOS-fast (SF) corner.

The standard deviation of Vth coming from random variation is given as [20]

$$\sigma_{\mathrm{Vth}} \propto T_{\mathrm{ox}} \cdot \frac{\sqrt[4]{N \cdot T \cdot \ln(N / n_{\mathrm{i}})}}{\sqrt{L_{\mathrm{eff}} \cdot W_{\mathrm{eff}}}},$$

where T_{OX} stands for the gate oxide thickness, N denotes a channel dopant concentration, T signifies an absolute temperature, n_i represents the intrinsic carrier concentration, and L_{eff} and W_{eff} respectively represent the effective channel length and width of a transistor. In fact, σ_{Vth} is becoming larger generation by generation because the channel area ($L_{eff} \times W_{eff}$) shrinks as manufacturing processes become increasingly advanced.

The process variations drastically decrease the operating margins of SRAM in nanometer CMOS technology.

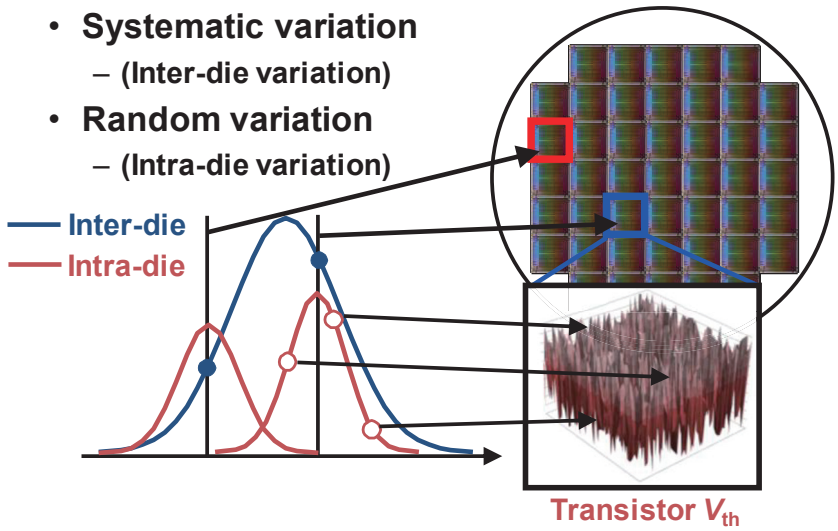


Fig. 2.6 Systematic (inter-die) and random (intra-die) threshold voltage (V_{th}) variation.

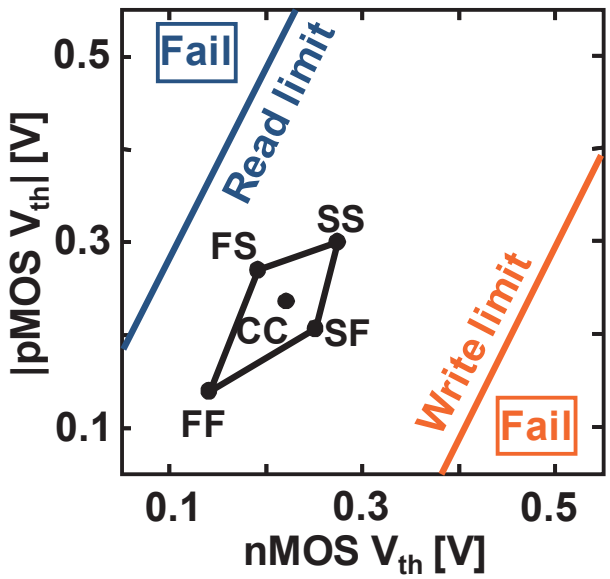


Fig. 2.7 Milky-way plot and five process corners (FF, FS, CC, SF, SS) with read and write limits of SRAM [19].

2.2 Degraded Energy Efficiency

2.2.1 Sense Amplifier Offset and Bitline Swing Variation

Figure 2.8(a) exhibits a block diagram of a 6T SRAM cell array and a sense amplifier (SA). One of the bitline pair (BL and BLN) is selected by column switches. When the wordline (WL) is asserted, the BL or BLN is discharged by the activated memory cell. The SA is activated by a SA enable signal (SAE) when the difference between a pair of bitline voltages exceeds the SA offset. Figure 2.8(b) shows bitline waveforms at normal and lower supply voltages. As described in Section 2.1, the SA offset is also much larger because of the process variation. The lower supply voltage makes the offset larger and the SAE timing slower, which degrades the energy efficiency.

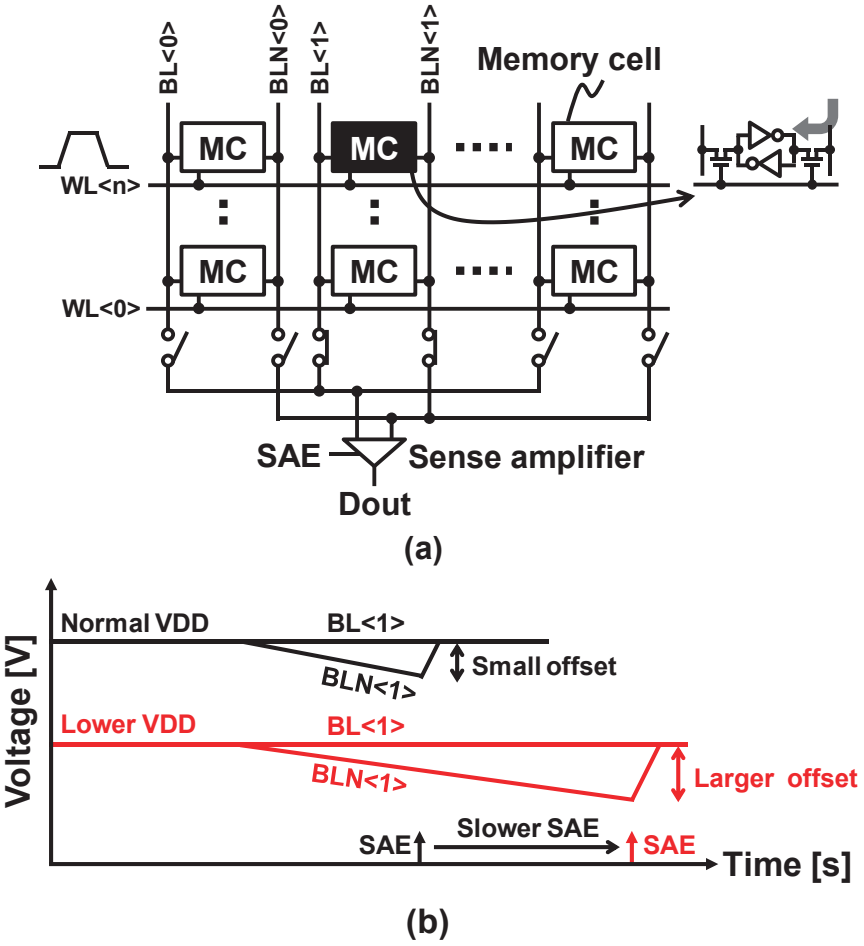


Fig. 2.8 (a) Block diagram of a memory cell array and a sense amplifier. (b) Bitline waveforms at normal and lower VDD.

Recent reports have described the effectiveness of low-voltage operation for energy reduction in SRAM degrades at the scaled process [25, 26]. Figure 2.9 presents a simulated histogram of the read current in an SRAM cell at 0.5 V. The read current of the slowest cell in 5000 Monte Carlo simulations was 0.016 times slower than that of the nominal cell. The SRAM designers configure a pulse width of the wordline by the slowest cell and the SA offset. Figure 2.10 depicts simulated waveforms of the bitline including random variation. In most cases, BLs are greatly discharged by faster cells, although the slowest cell pulls down the bitline.

The bitline swing variation and slower SAE signal increase the dynamic energy by 82% compared to the nominal simulation without random variation, as reported in an earlier research paper [26]. The energy efficiency degradation entails a difficulty for voltage scaling.

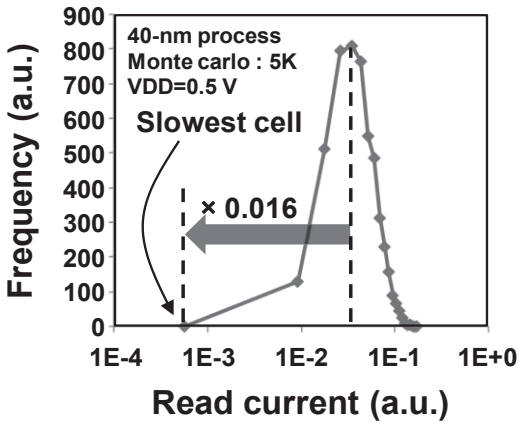


Fig. 2.9 Histogram of read current of a 40-nm SRAM cells operating at 0.5 V.

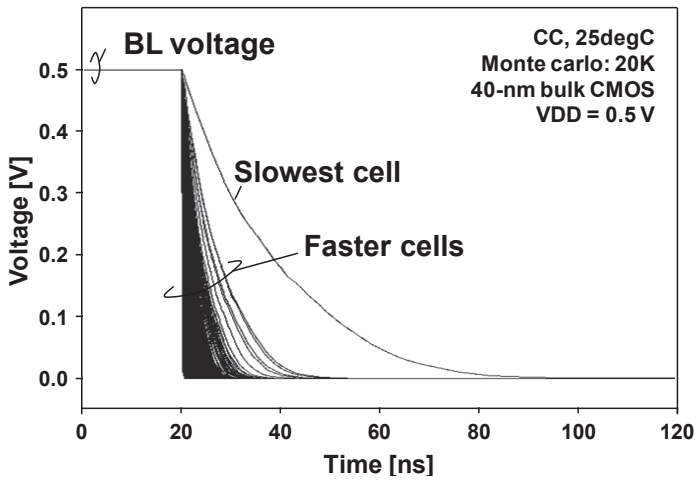


Fig. 2.10 Waveforms of bitlines operating at 0.5 V.

2.3 Poor Soft-Error Immunity

As process technology has produced more miniaturized products over time, the embedded memory, SRAM, has become increasingly susceptible to particle-induced soft error effects because of its low critical charge [27]. Figure 2.11 presents a trend of critical charge (Q_{crit}) for SRAM in 15-nm to 130-nm process nodes [27, 29, 30, 31, 67]. Q_{crit} is the minimum charge that is capable of flipping the data stored in an SRAM cell. The vulnerability of SRAM to soft error depends on the Q_{crit}. When the Q_{crit} decreases linearly, the soft error rate (SER) increases exponentially [57]. Process scaling decreases Q_{crit} because of the reduced node capacitance and the voltage scaling, which degrades the SRAM reliability.

Neutron particles, although not electrically charged, are known to cause soft error effects in electrical devices via a nuclear reaction [28]. When secondary ions generated by the reaction pass through integrated circuits, electron–hole pairs are produced along the ion track. The carriers are collected to an electrical memory device by drift and diffusion processes. The memory cell is flipped if the collected charge exceeds its Q_{crit}. In the scaled process, the secondary particles via single nuclear reaction can cause not only a single event upset (SEU) but also multiple cell upset (MCU) in a dense SRAM [32]. An MCU ratio to the total SER in the SRAM is predicted to increase from several percent in a sub-100 nm process to about 50% over a 22-nm process [9].

Figure 2.12 presents a definition of multiple cell upset (MCU) and multiple bit upset (MBU). The MCU indicates one or more upsets in different words, which can be corrected by single-error-correction and double-error-detection ECC (SEC-DED). However, the MBU includes MCU in the same word, which cannot be corrected by SEC-DED. To prevent the MBU, a bit-interleaving structure allocates logical words in physically separated positions. The number of the interleaving bits is an important factor to design the robust SRAM. Wide interleaving bits improve the MBU immunity. However, the long wordline degrades access performance and increases the unselected (half-select) cells. Consequently, the scaled SRAM must be designed carefully considering the tradeoff between the soft-error immunity and energy efficiency.

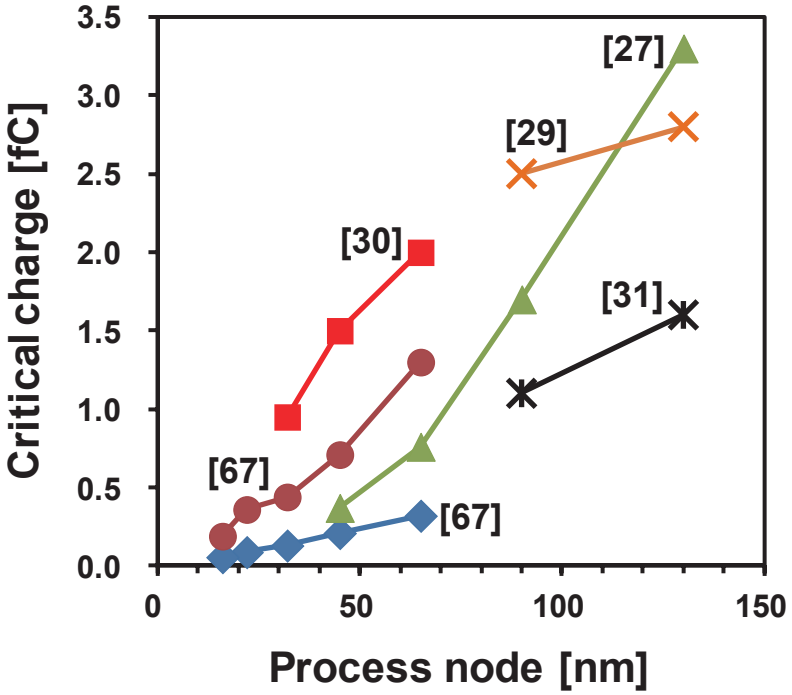


Fig. 2.11 Trend of simulated critical charge for SRAM in 15 nm to 130 nm process nodes.

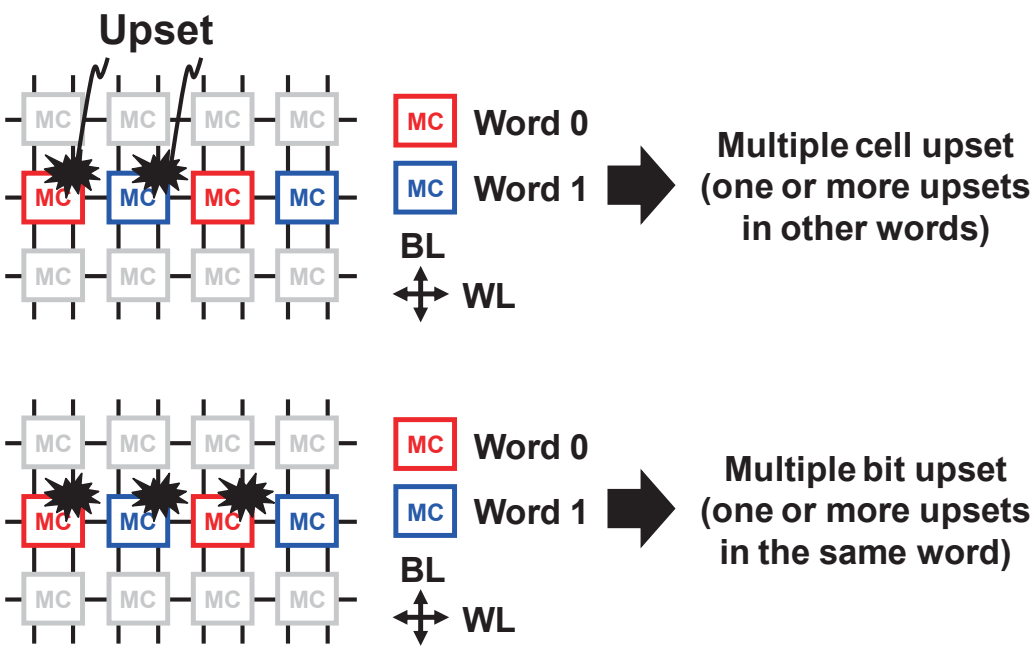


Fig. 2.12 Multiple cell upset and multiple bit upset definition.

2.4 Summary

This section summarized the three issues of SRAM in the nanometer CMOS technology.

- Decreased operating margin

  The SRAM cell is designed by the minimum feature size in a process. Process variation degrades the operating margin of the SRAM because of process scaling and voltage scaling.
- Degraded energy efficiency

  At low-voltage operation, the energy efficiency is degraded by process variation in the nanometer CMOS technology. The SRAM has a wordline pulse width that is designed by the slowest cell. During the readout for the slowest cell, other faster cells fully discharge the bitlines, which increases the energy consumption.
- Poor soft-error immunity

  Soft error constitutes an important reliability issue for scaled SRAMs. Process scaling increases the ratio of multiple cell upsets to single-bit upset. The multiple upset in the same word must be considered in order to prevent system errors.

These issues must be regarded when one strives to achieve robust SRAM design. In this dissertation, novel techniques are presented in Chapters 3–6 to address the issues.

Chapter 3 Half-Select Disturb Tolerant 8T SRAM Design

This chapter presents a description of two half-select disturb tolerant 8T SRAM designs:

1) Dual write wordline 8T cell with a sequential writing technique
2) Low-power disturb mitigation scheme

Half-select disturb is an important issue for low-voltage operating 8T SRAM in a scaled process. The two techniques mitigate the disturb issue and achieve low-voltage and low-power operation.

3.1 Dual Write Wordline 8T SRAM with a Sequential Writing Technique

3.1.1 Half-Select Disturb Issue for Low-Voltage 8T SRAM

Dual port 8T cells have been proposed to free the SNM/WNM tradeoff with its dedicated read port, which enables lower-voltage operation than 6T SRAMs. The 8T cells, however, have a half-select problem, which is a disturbance to unselected cells in a write cycle [33] as illustrated in Fig. 3.1. The half-selected cell in the unselected column is disturbed because the 8T cell is usually comprised of minimum sizing transistors and the β ratio is one; the cell content might be flipped when the write wordline (WWL) is activated for turning on all the access gates in the horizontal direction.

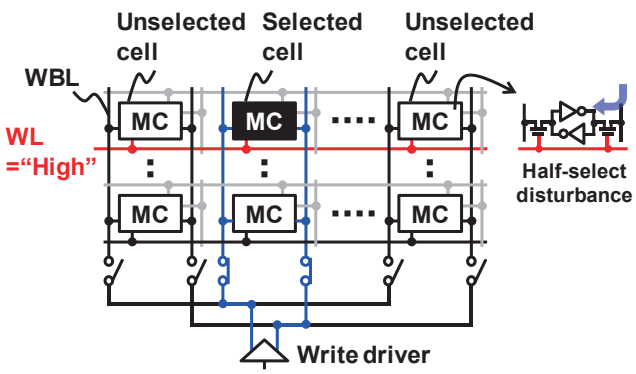


Fig. 3.1 Half-select disturb issue for low-voltage 8T SRAM [33].

3.1.2 Dual Write Wordline 8T SRAM

Figure 3.2 presents a schematic of the proposed dual write wordline 8T (DW8T) cell and the concept of the sequential writing technique. In the proposed DW8T cell, the write bitlines (WBLs) are precharged to a half of the supply voltage (a half VDD), which decreases the disturbing currents through the WBLs. The proposed 8T cell has two WWLs: they are called "dual write wordlines" in this paper and are sequentially activated in a write cycle. The sequential writing technique eliminates one of the two disturbing currents flowing from a high-state node to WBL and from WBLN to a low-state node. Utilizing the half-VDD precharging WBLs and the dual write wordlines, the proposed scheme mitigates the half-select problem.

Figure 3.3 shows waveforms of the conventional and proposed 8T cells in the half-selected situation. In a write operation, the conventional 8T cell is disturbed by the noise current from a write bitline to a low-state node. On the other hand, the proposed DW8T cell is disturbed by either of the two disturbing currents mentioned above: one is from a high-state node and the other is to a low-state node.

The proposed sequential writing technique can separate the two disturbing currents because the dual write wordlines are sequentially activated in the proposed DW8T cell. The disturbing current in the DW8T is suppressed lower than the conventional 8T and its SNM is improved because the WBLs are precharged to a half VDD.

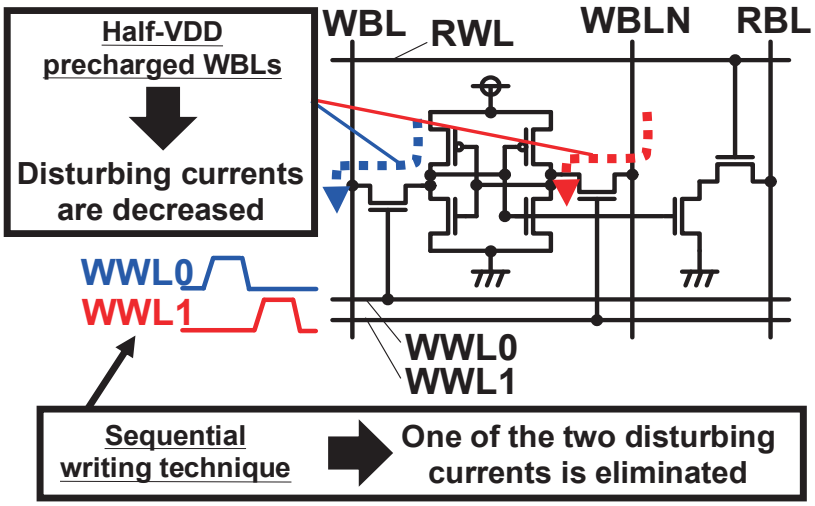


Fig. 3.2 The proposed dual write wordline 8T (DW8T) cell and novel sequential writing technique.

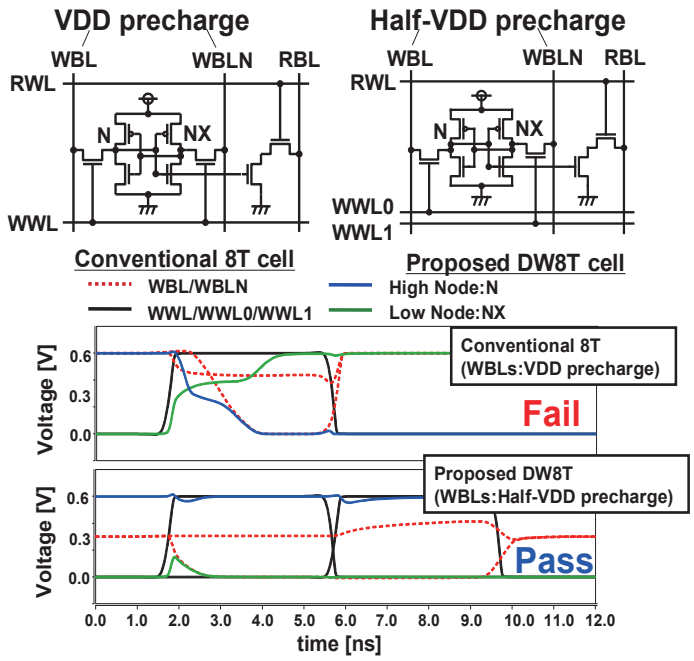


Fig. 3.3 Waveforms of the conventional 8T cell and the proposed DW8T cell when half-selected in a write cycle.

Figure 3.4 presents a comparison of the SNMs in the conventional and proposed 8T cells when no variation is considered. The butterfly curves for the proposed DW8T, however, become asymmetric because either of the access gates is merely asserted. The proposed scheme improves the SNM to 86 mV from 68 mV (18 mV = 26.5% improvement).

Figure 3.5 shows the simulated bit error rates (BERs) of the conventional 8T, DW8T and DW8T with a negative WBL scheme. The both DW8Ts use the proposed sequential writing technique. The DW8T (without the negative WBL) has disadvantages in the write margin due to the proposed sequential write technique; in the write worst corner (SF, -40°C), the write BER of the DW8T is degraded by 1.5 orders of magnitude, compare with the conventional 8T. Therefore, we adopt negative WBL scheme [34] to improve the write margin. The negative bitline level is -0.1 V (20% of VDD). The BERs of the DW8T with the negative WBLs are limited by the half-select margin at the disturb worst corner (FS, 125°C) and a typical corner (CC, 25°C), whereas at the write worst corner, its BER is indeed limited by the write margin. The DW8T improves the half-select BER by 71% at the disturb worst corner and by 79% at the typical corner over the conventional 8T, respectively. Its write BER is degraded by 11% at the write

worst corner; however it is not the global worst point. The performance in terms of BER is restricted by the disturb worst corner in our design.

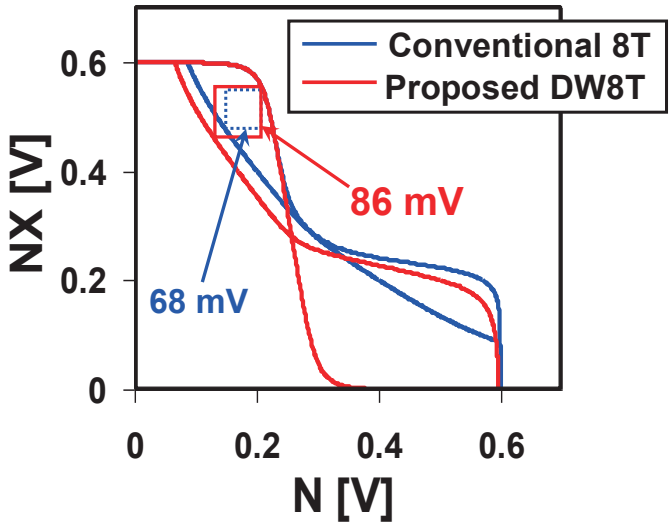


Fig. 3.4 SNM comparison between the conventional 8T cell and the proposed DW8T cell (CC corner, 25°C).

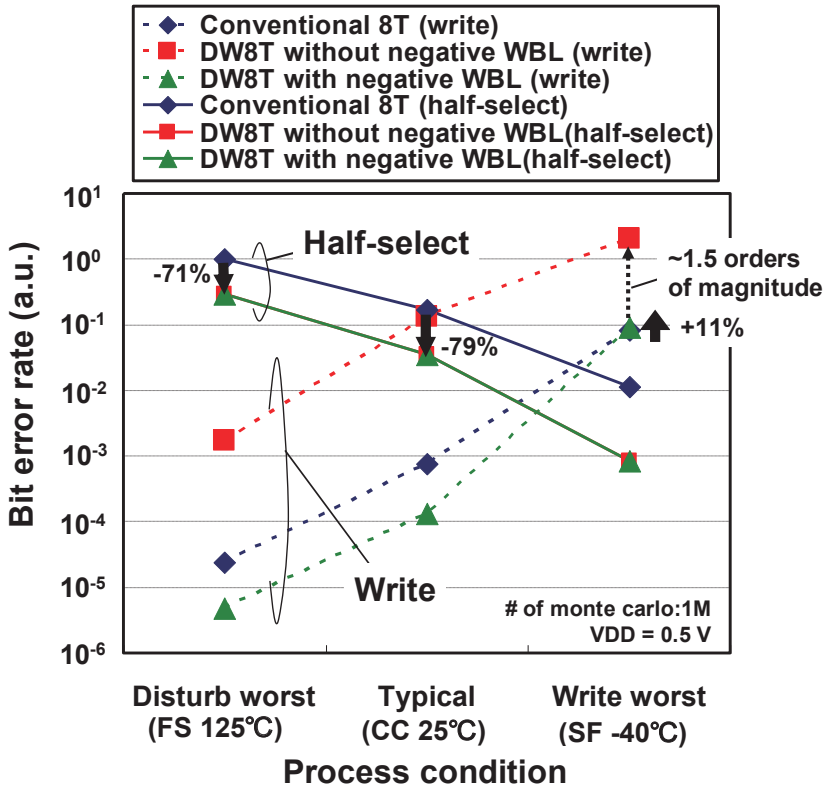


Fig. 3.5 Simulated BERs of the conventional 8T SRAM, DW8T SRAM, and DW8T SRAM with negative WBLs.

3.1.3 Experiment Results

We designed a 256-Kb DW8T SRAM test chip in a 40-nm CMOS process. We also implemented half-VDD generators on the chip [35]. Each 8-Kb SRAM block has a half-VDD generator. Figures 3.6(a) and 3.6(b) illustrate the schematic and the layout of the half-VDD generator. The layout size is 35 × 5 μm^2. The area overhead is less than 0.5% in the 256-Kb SRAM macro.

Figure 3.7 shows the measured output voltages of the half-VDD generators in three test chips implemented in the CC corner. In the output range of 0.2 V to 1.1 V, the output voltage follows the half VDD within an error of -45 mV to +35 mV at room temperature (RT).

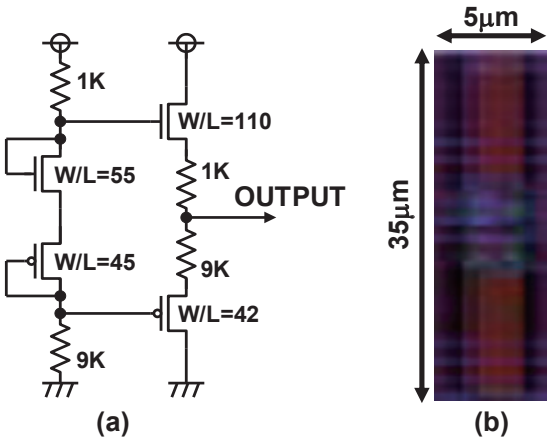


Fig. 3.6 (a) Schematic and (b) layout of the half-VDD generator [35].

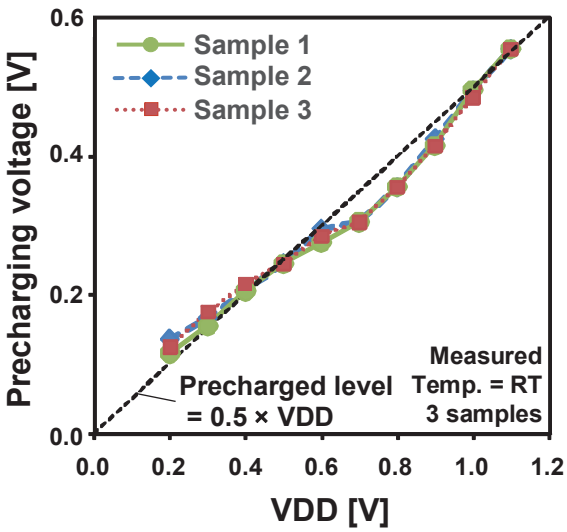


Fig. 3.7 Measured output voltages of the half-VDD generators in three test chips. The nominal VDD is 1.1 V.

Figure 3.8 illustrates the measured half-select BERs of the conventional 8T SRAM and the proposed DW8T SRAM with the sequential writing technique on the best chip. The measurement result of the conventional 8T SRAM was obtained by reusing the proposed DW8T SRAM; the dual write wordlines are simultaneously controlled in a similar manner and the WBLs are precharged to VDD in this case. The precharge level can be changed to an arbitrary value on the test chip. The measurement results show that the proposed DW8T SRAM with the sequential writing technique can operate at a VDD_{min} of 0.6 V and can improve the VDD_{min} by 0.4 V on the best chip.

By using seven test chips, we also measured the VDD_{min}'s of the conventional 8T SRAM and the proposed DW8T SRAM. Figure 3.9 shows the data from the seven samples. The number six is the best chip mentioned above. The VDD_{min} is improved by 367 mV (from 1.019 V to 0.652 V) on average in the proposed DW8T SRAM.

Figure 3.10 illustrates a shmoo plot of the access time and VDD. The operation is restricted by a read operation rather than the write operation. So, we confirmed that the proposed scheme does not affect its access time although the proposed DW8T has the dual write wordlines to be sequentially activated. The best chip can operate at an access time of 20.0 ns even when the VDD is 0.6 V. The access time at the nominal VDD of 1.1 V is 8.5 ns.

The leakage power was measured in the standby mode as shown in Fig. 3.11. The VDD and the operating frequency were set to 0.6 V and 10 MHz, respectively. In the figure, the precharging voltage on the WBLs are changed to a half VDD (= 0.3 V) in the proposed scheme. The leakage power is decreased by 25%, compared with the conventional 8T SRAM. The leakage power is decreased with a precharging voltage because bitline leakage is accordingly reduced.

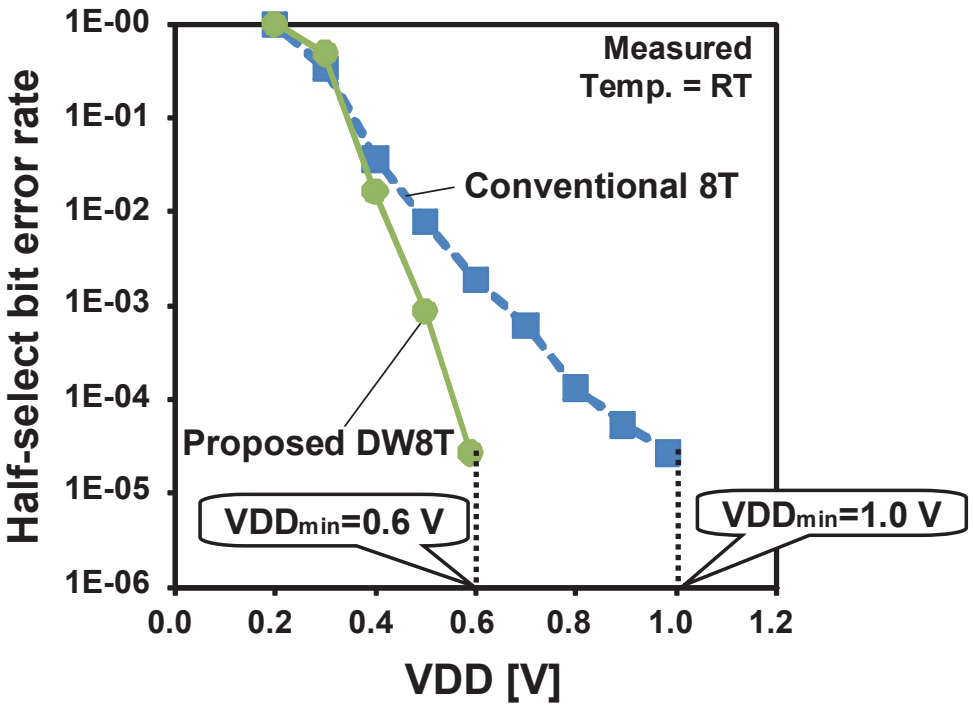


Fig. 3.8 Measured half-select BERs of the conventional 8T SRAM and the proposed DW8T SRAM (best chip). The operating frequency is 10 MHz.

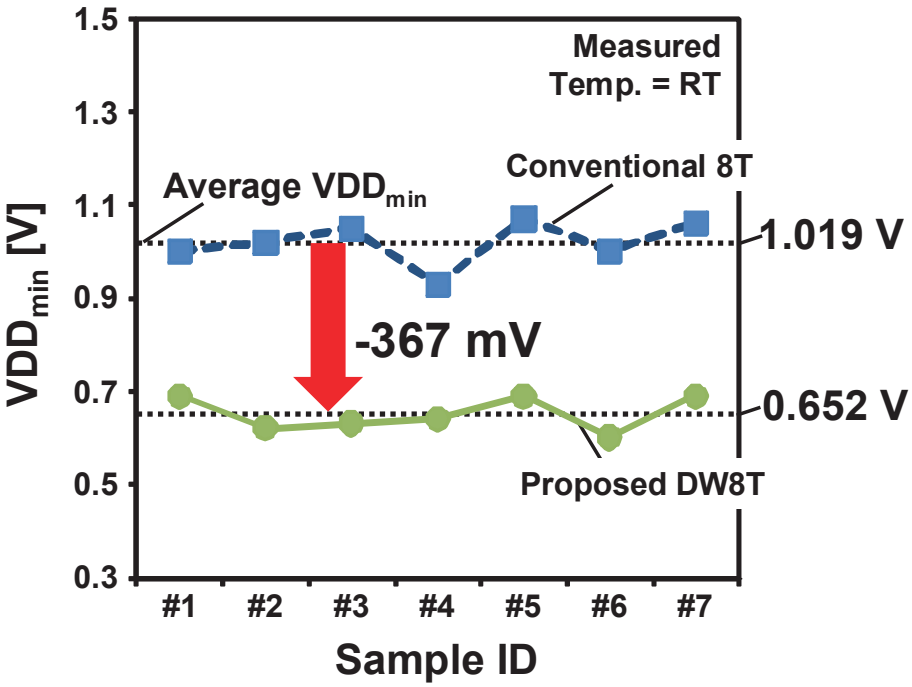


Fig. 3.9 Measured VDD_{min}'s of the coventional 8T SRAM and the proposed DW8T SRAMs. #6 is the best chip.

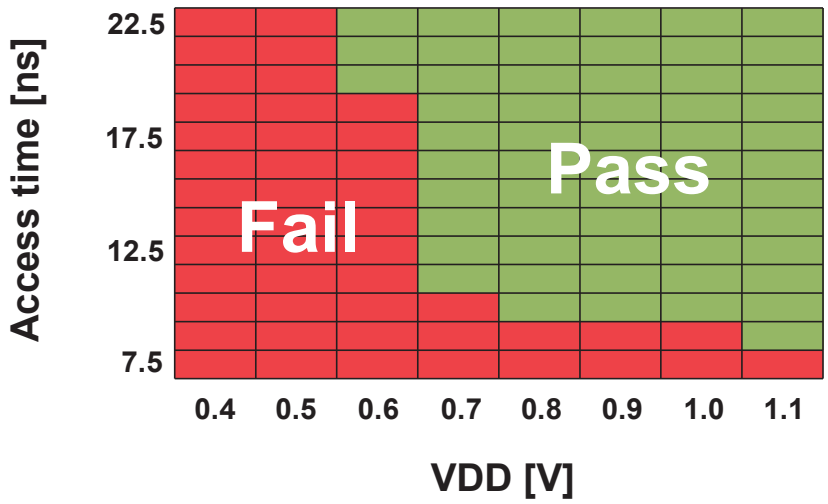


Fig. 3.10 Shmoo plot of the proposed 256-Kb DW8T SRAM.

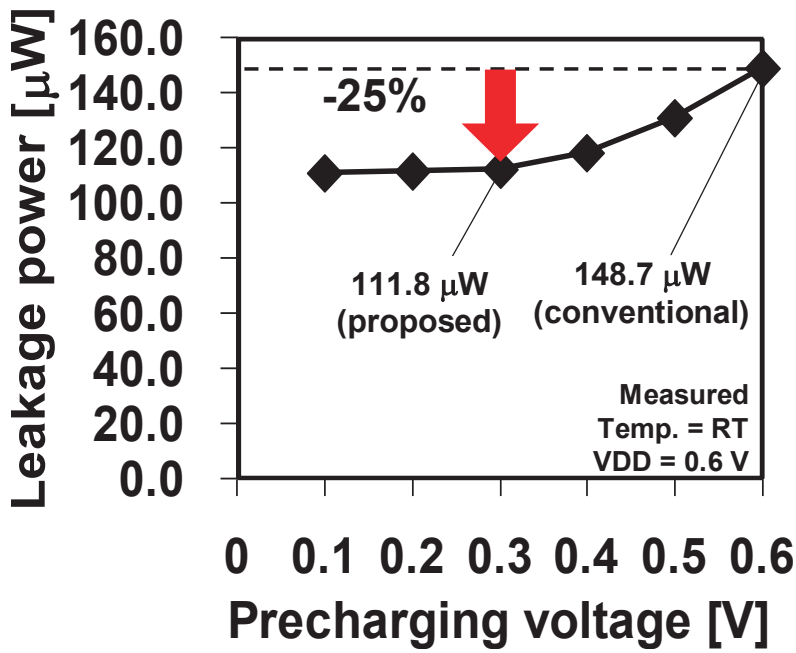


Fig. 3.11 Measured leakage power in the proposed DW8T SRAM when a precharging voltage is changed.

We also investigated area overheads; the proposed 8T SRAM requires an additional WWL and an extra driver for it to implement the sequential writing technique. The additional WWL can be laid out without any area overhead in the given process, whereas the extra WWL driver occupied some area. The area overhead for the extra WWL driver is, however, small because it merely drives either of the access gates in the proposed DW8T cell and the capacitance is small (usually, the conventional SRAM

drives the two access gates, which has to be designed twice larger). Consequently, the area overhead for the dual write wordline drivers is only 2.3% in the SRAM macro. The area overhead derived from the negative WBL scheme is 2%. The proposed DW8T cell area is 0.6679 μm^2 on a logic rule basis, which is 21% larger than the classic 6T cell (the same size as that of the conventional 8T cell).

The configurations of the test chip are summarized in Table 3.1. The chip size is 2.5 × 2.5 mm^2, and the 256-Kb SRAM macro is 900 × 1420 μm^2. The SRAM macro is comprised of 16 bits per word × 512 words × 32 blocks. A die photograph is presented in Fig. 3.12.

Table 3.1 Configurations of the implemented test chip.

Technology	**40-nm CMOS Process**
Chip size	**2.5 mm × 2.5 mm**
SRAM macro size	**900 μm × 1420 μm**
Capacity	**256 Kbit**
SRAM organization	**16 bits/word × 512 words × 32 blocks**
Cell area	**0.6679 μm^2 (logic rule)**
# of cells / bitline	**64**
Performance (Access time @ VDD)	**8.75 ns @ 1.1 V, 20.0 ns @ 0.6 V (=VDD_{min})**

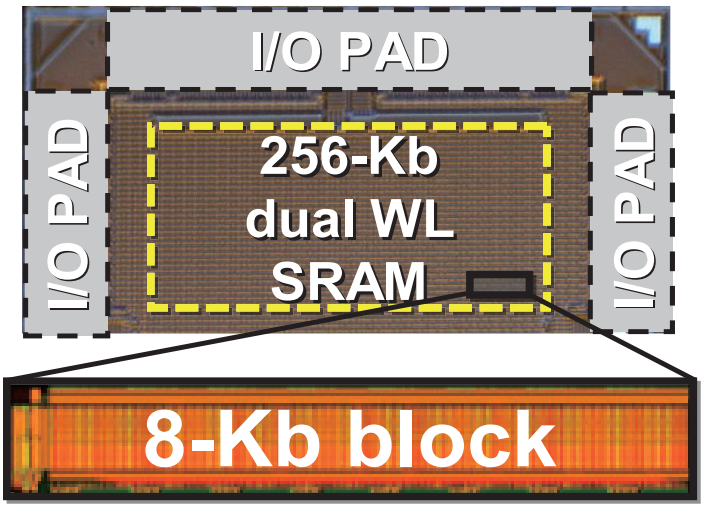


Fig. 3.12 Die photograph of the test chip.

3.2 Low-Power 8T SRAM Using Disturb Mitigation Scheme

3.2.1 Write-Back Scheme

To mitigate the half-select problem and lower the operating voltage, the divided wordline structure [21] and the write-back scheme [22] (Fig. 3.13) are useful in the 8T SRAM at a single supply voltage. In the latest SRAMs necessitate various functionalities, and although one functionality is the partial-write operation [23], the partial-write operation cannot be implemented in the divided wordline structure because a separated wordline is incorporated.

The write-back scheme for the 8T SRAM design can be implemented in the bit-interleaving structure, which provides soft-error immunity and partial-write functionality. The write-back scheme eliminates the half-select problem; however, a read operation is required even in a write cycle. In the write-back scheme in the write operation, input data to be written go to target cells at target columns, but at half-selected columns, readout data are written back to half-selected cells. Because the readout data at the half-selected columns do not need to be transferred to output buffers, the speed penalty in the write-back scheme can be minimized.

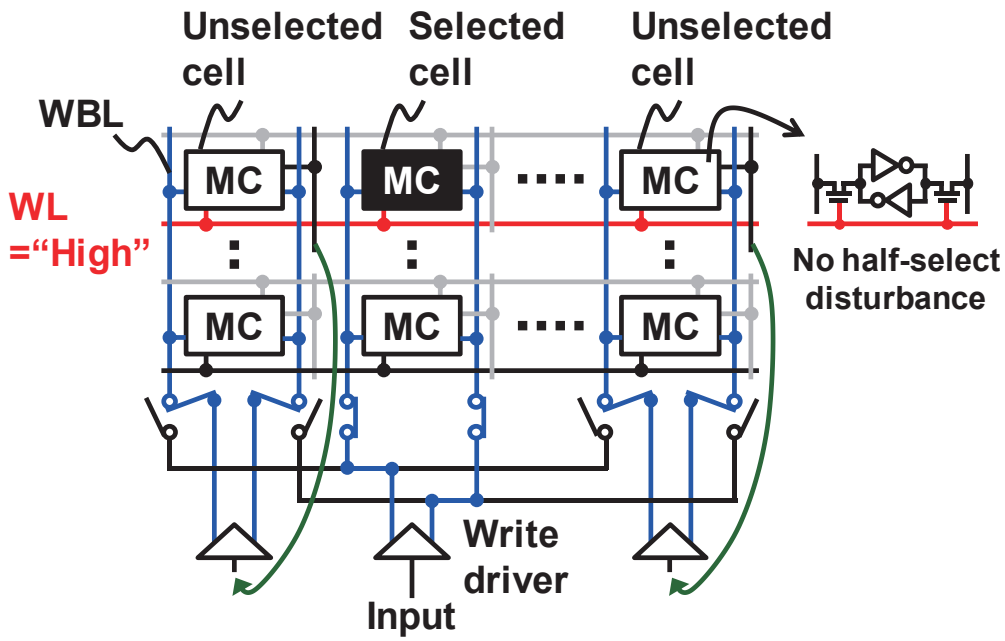


Fig. 3.13 Conventional write-back scheme for preventing half-select disturbance issue [22].

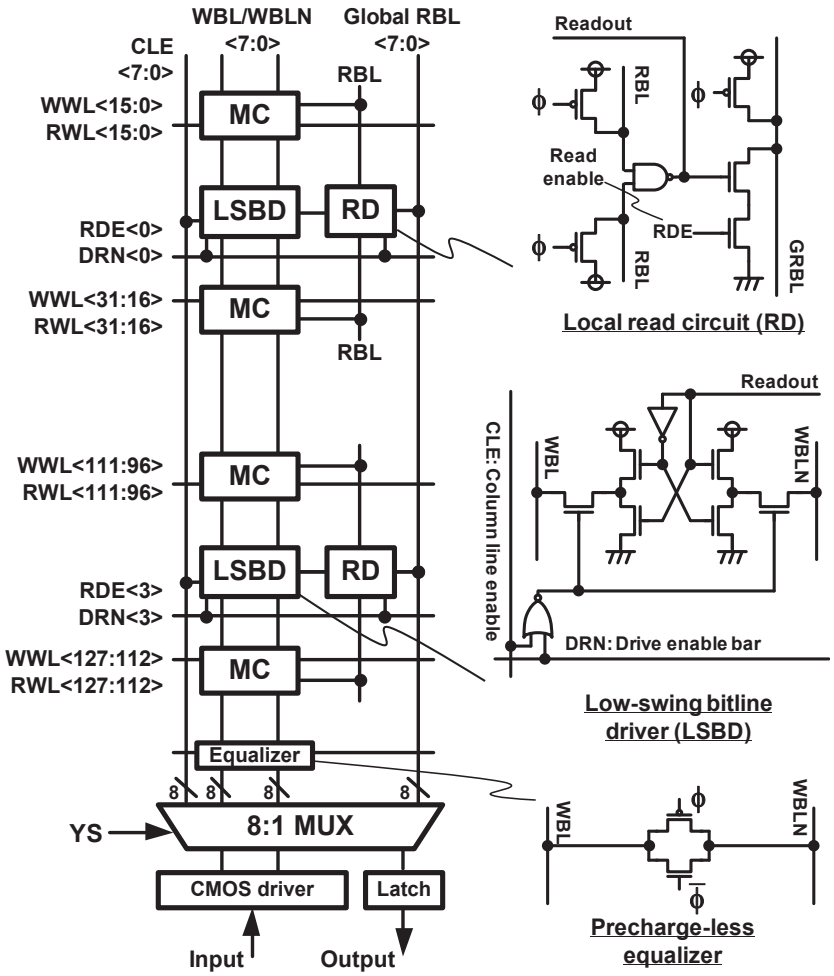
The write-back scheme has power overhead because the CMOS write drivers fully pull the write bitlines (WBL/WBLN) up or down at all half-selected columns. The WBLs are usually longer than read bitlines (RBL) to preserve array efficiency [24]. Consequently, the active energy in the half-selected columns degrades the energy efficiency.

3.2.2 Disturb Mitigation Scheme

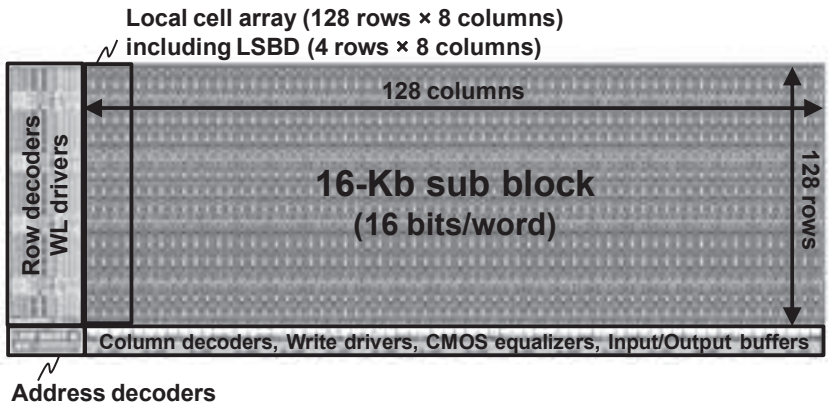
To reduce the extra energy for the half-select problem, we propose a disturb mitigation scheme that features the following: floating WBLs with a precharge-less equalizer (CMOS transmission gate) and the low-swing bitline driver (LSBD) with nMOS pull-up transistors for the WBLs, which limit the swing of the WBLs in the half-selected columns.

Figures 3.14(a) and 3.14(b) illustrate a local cell array (128 rows × 8 columns) and a 16-Kb sub-block (16 local cell arrays) configuration of the proposed SRAM. Figure 3.14(a) also shows circuitry of the local read circuit, the LSBD, and the precharge-less equalizer. The single-ended 8T cell is adopted in the SRAM. The proposed 8T SRAM employs a hierarchical read bitline (RBL) structure. The number of cells per RBL is 16 for stable read operation. In contrast, a WBL is shared by 128 cells to preserve the array efficiency. The WBLs are not precharged to a supply voltage, but floated because of the precharge-less equalizer. A local read circuit and an LSBD are shared by 32 cells. A CMOS write driver is shared by a local cell array.

Figure 3.15 illustrates operating waveforms of the proposed scheme. In a read cycle, a read enabling (RDE) signal is activated; then a global read bitline (GRBL) is discharged when an RBL is pulled down. In the write cycle, the dedicated read ports transport the data to the local read circuits. Column line enable (CLE) signals are high in the selected columns and the LSBDs are disabled as presented in Fig. 3.16. In the half-selected columns (CLE = “L”), the proposed LSBDs drive the WBLs according to the readout data when the driver enable (DRN) signal is grounded. The LSBD consists only of nMOSes. Thereby, the swing of WBLs is limited by the threshold voltage of the nMOSes. After the WBLs are pulled up or down by nMOS-based LSBDs, the write wordline (WWL) is activated. The selected cell is written by the CMOS write driver and the write margin is not degraded.



(a)



(b)

Fig. 3.14 (a) Local cell array and (b) 16-Kb sub-block with the proposed circuitry including a low-swing bitline driver (LSBD) and precharge-less equalizer. “MC” signifies “single-ended 8T memory cell”.

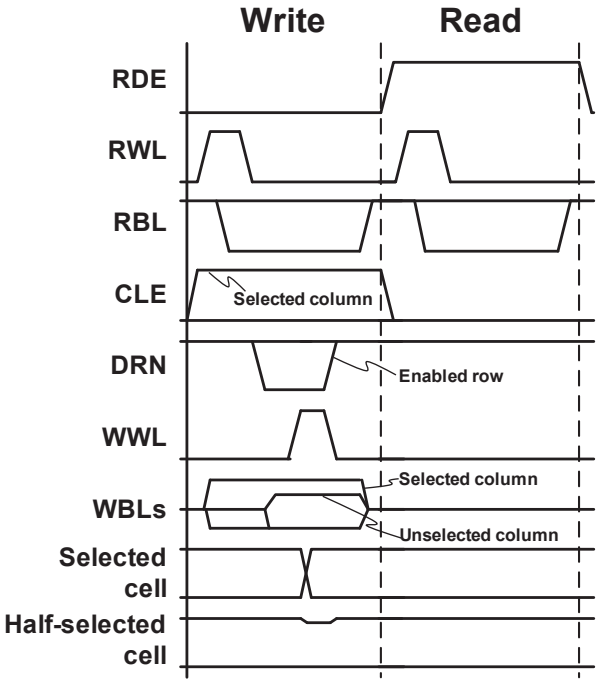


Fig. 3.15 Operating waveforms.

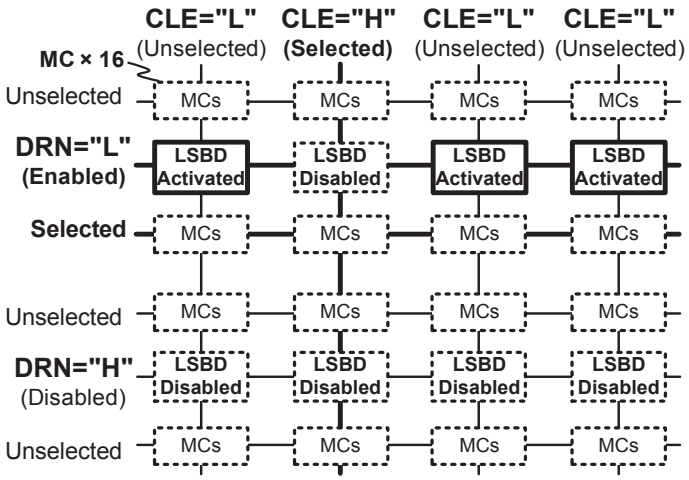
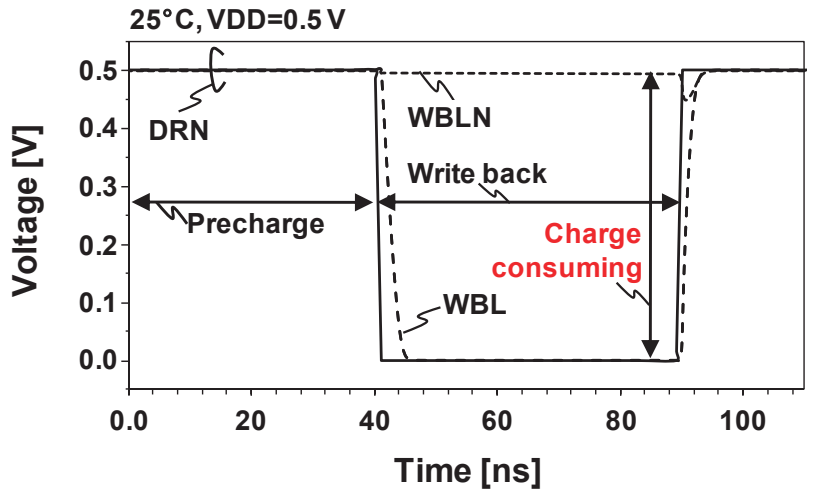


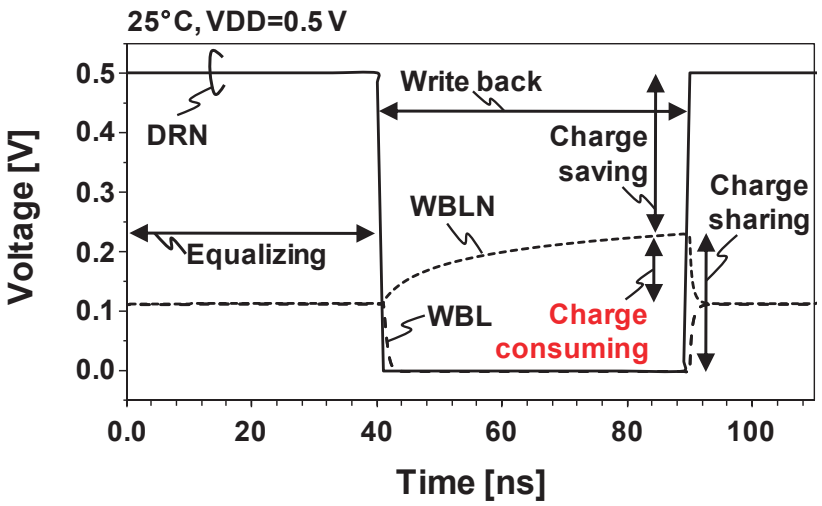
Fig. 3.16 Activated LSBDs exist on low-state CLE (column line enable) and low-state DRN (driver enable bar) signals.

Figures 3.17(a) and 3.17(b) respectively show waveforms of the write bitline pair (WBLs: WBL and WBLN) in the half-selected columns with the conventional write-back scheme and the proposed scheme. In the conventional write-back scheme, the WBLs are precharged to supply voltage until the DRN signal is pulled down. The

WBL is grounded and the WBLN is pulled up by the CMOS drivers. When the write operation is finished, the WBLs are precharged again. In contrast, the WBLs in the proposed scheme are floated until the DRN activation. When the WBL and WBLN are pulled down and up by the proposed LSBD, then the charging energy is saved because the rising write bitline voltage is saturated at an intermediate voltage by the threshold voltage of an nMOS in the LSBD. At the end of the write cycle, the write bitlines' voltages are again equalized with charge sharing. The floating WBLs reduce bitline leakage current because no precharge transistors are incorporated.



(a)



(b)

Fig. 3.17 Waveforms of the half-selected cells assisted by (a) the conventional write-back scheme and (b) the proposed scheme.

Figure 3.18 shows that a pulled-up WBL level depends on V_{tn}: if an nMOS is fast, then the V_{tn} drop is small, the disturb mitigating assist becomes effective. However, a slow nMOS can save power because its swing is small. The enlarged margin and saving power are a tradeoff. Figure 3.19 illustrates the active power reduction compared to the conventional write-back scheme at the write cycle. The active energy on the WBLs is reduced by 37%, 60%, and 79%, respectively at the FF, CC, and SS corners at 25°C.

We investigated the disturbance margins of the half-select cells with the proposed disturb mitigation scheme. Monte-Carlo analyses are executed at the five process corners and at three temperatures when VDD is 0.5 V. The simulation considers threshold voltage variation in the LSBD shared by 32 bitcells. The yield in Table 3.2 shows that the SS corner at -40 °C is the worst case and its yield is 3.27σ, in which the pull-up transistors in the LSBD is weakened. In the worst case, the voltage of the suppressed WBL, "VDD - V_{tn}" is decreased. The weak pull-up transistor and the more suppressed WBL causes more disturbing current flowing through the pass gate transistor of the SRAM cell. The tradeoff between the yield at the global corner and the saved energy must be considered in the SRAM design.

Figure 3.20 illustrates simulation results of the leakage power on the WBLs at the activated cycle in 8T bitcells. The leakage power in the worst corner is improved by 33% because of the low-swing feature of the LSBD.

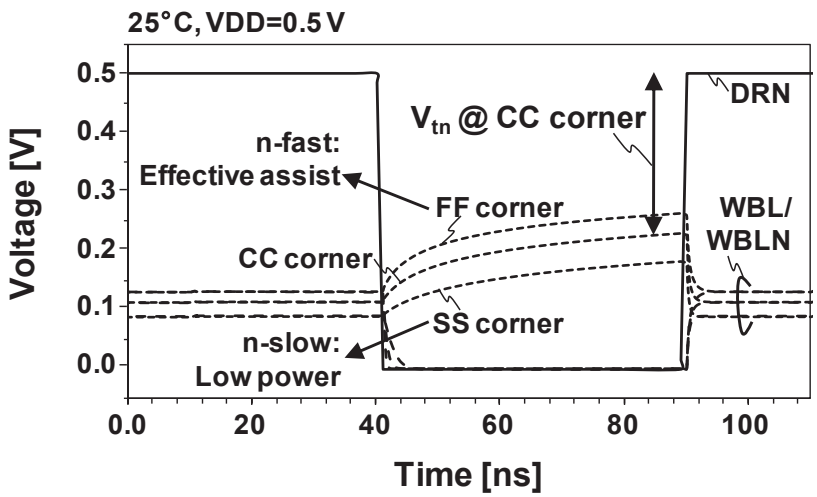


Fig. 3.18 Pulled-up WBL level dependence on the global corner.

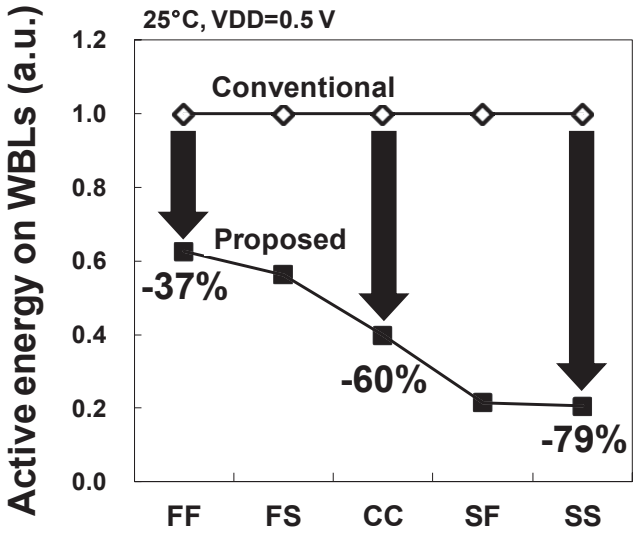


Fig. 3.19 Active energy reductions on WBLs at the five process corners (RT, room temperature; VDD = 0.5 V).

Table 3.2 Yields of half-selected cells in the proposed scheme.

Yield @ 0.5 V (based on Monte Carlo)		Temperature [°C]		
		-40	25 (RT)	125
Global corner	FF	5.39σ	> 7σ	> 7σ
	FS	4.79σ	5.59σ	> 7σ
	CC	4.31σ	5.49σ	> 7σ
	SF	4.04σ	5.45σ	> 7σ
	SS	3.27σ	4.47σ	6.85σ

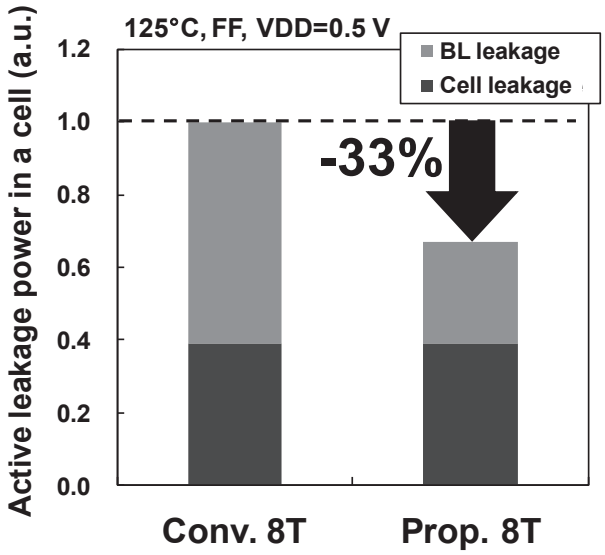


Fig. 3.20 Comparison of the active leakage power of the conventional and proposed schemes (FF corner, 125°C, VDD = 0.5 V).

3.2.3 Measurement Results

As presented in Fig. 3.21, we fabricated the proposed and conventional 512-Kb 8T SRAM macros using a 40-nm CMOS bulk process for comparison. The conventional macro incorporates a write bitline precharger connected to a supply voltage. Therefore, its write bitlines are fully charged and discharged in the write-back operation. The proposed 512-Kb macro consists of 32 × 16-Kb sub-blocks, as shown in Fig. 3.14(b). Table 3.3 shows specifications of the proposed SRAM test chip. The 8T bitcell area is 0.706 μm^2, which is 28% larger than a 6T cell with a β ratio of two. The transistor width of access gates is doubled to enhance a write margin while the other transistors are minimum sizing. The numbers of cells in a RBL and WBL are 16 and 128, respectively. The cell density is 701 Kb / mm^2.

Figure 3.22 presents a measured Shmoo plot of the proposed 8T SRAM macro. The access time is restricted by the read operation. The minimum operating voltage is 0.5 V at an access time of 160 ns at room temperature (RT). Figures 3.23 and 3.24 respectively show that the measured leakage power and active energy, which are improved by 26.0% and 59.4% at the supply voltage of 0.5 V. The active energy in the write cycle is 1.52 pJ (= μW/MHz). The total energy is 12.9 pJ when the read and write cycles are 50–50 at 0.5 V.

Table 3.3 Features of the test chip.

Technology	40-nm bulk CMOS
Macro size	0.723 mm × 1.010 mm
Macro configuration	512 Kb (16 Kb × 4 × 8), 16 bits/word
Cell size	0.706 μm^2 (logic rule)
# of cells / BL	16 (RBL), 128 (WBL)
Cell density	701 Kb/mm^2
Power supply	0.5–0.8 V
Write active energy	1.52 μW/MHz @ 0.5 V, 6.25MHz, RT
Total energy (R/W=50/50)	12.9 μW/MHz @ 0.5 V, 6.25MHz, RT
Access time	160 ns @ 0.5 V, 4.5 ns @ 0.8 V

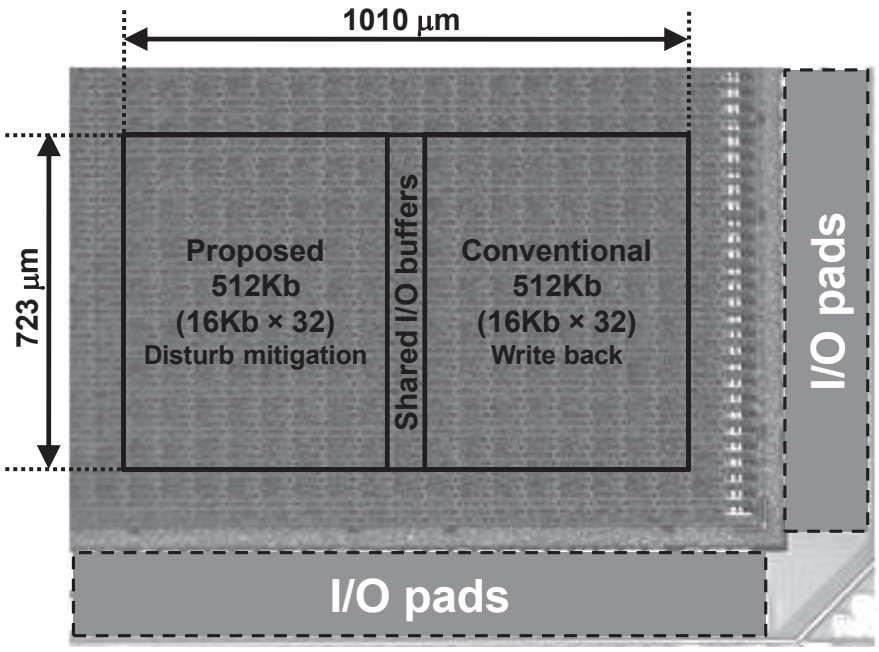


Fig. 3.21 Micrographs of the test chip: 1 Mb SRAMs include the proposed disturb mitigating scheme and the conventional write back scheme.

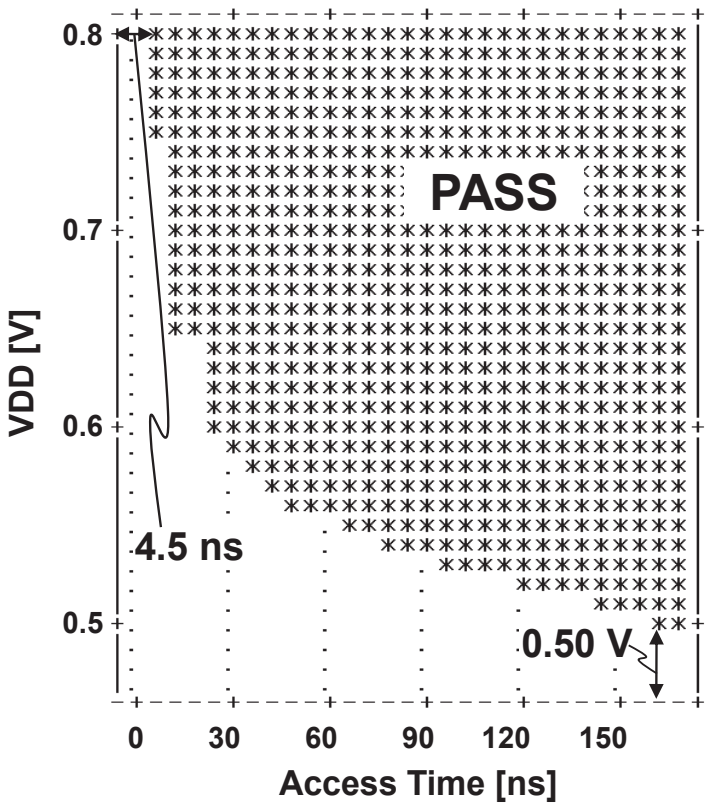


Fig. 3.22 Shmoo plot of the proposed 512-Kb SRAM macro.

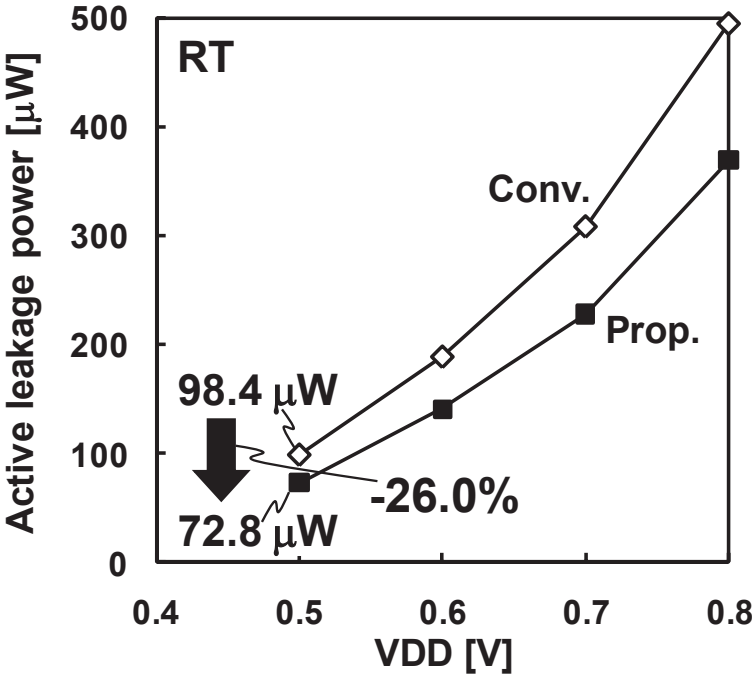


Fig. 3.23 Measured active leakage power at RT.

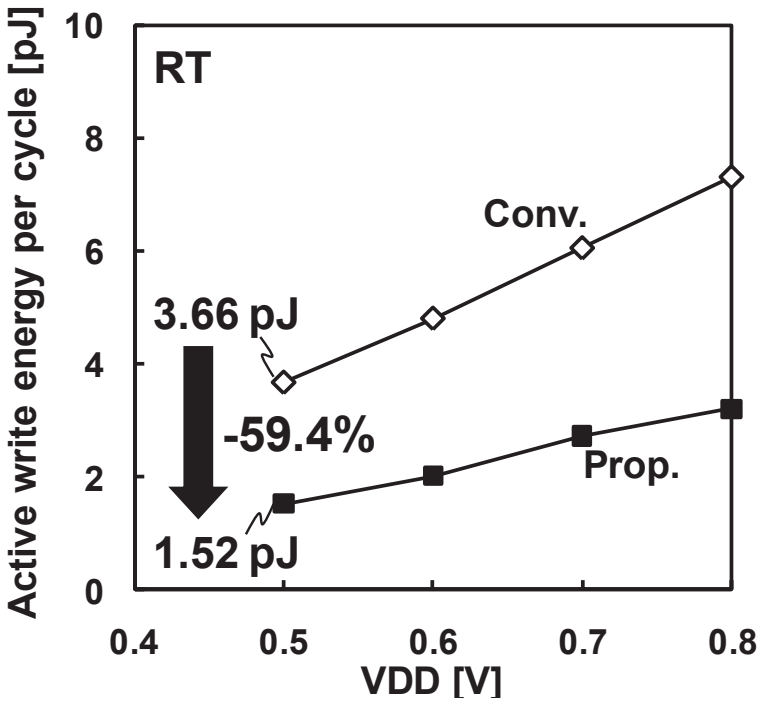


Fig. 3.24 Measured active energy per write cycle without leakage at RT.

3.3 Summary

In this section, we describe two half-select disturb tolerant SRAM designs: dual write wordline 8T (DW8T) SRAM and disturb mitigating 8T SRAM.

1) The DW8T SRAM with the sequential writing technique can mitigate the half-select problem. A half-VDD generator was designed to precharge WBLs for decreasing disturbing currents. The proposed sequential writing technique further eliminates one of the two disturb currents, which improves the half-select margin better. DW8T with sequential writing technique improves the half-select BERs by 71% at the disturb worst corner and 79% at the typical corner compared with the conventional 8T, respectively. We implemented the 256-Kb DW8T SRAM macro and the half-VDD generator on a single chip in a 40-nm CMOS process. The measured output voltage of the half-VDD generator shows good dependence on the VDD from 0.2 V to 1.1 V within an error of -45 mV to +35 mV. The VDDmin of the proposed 256-Kb DW8T SRAM is improved by 367 mV on average among seven sample chips. The best chip operates at a VDDmin of 600 mV. The proposed half-VDD precharging WBLs improves the leakage power by 25%, compared with the conventional 8T SRAM.
2) The disturb mitigation scheme achieves low-power and low-voltage operation for an 8T SRAM. The proposed scheme has a 3.27σ yield at 0.5 V at the SS corner and low temperature. The active energy is improved by 37%, 60%, and 79% at FF, CC, and SS corners, respectively at 25°C. The 512-Kb 8T SRAM test chips were implemented in a 40-nm bulk-CMOS process. The SRAM operates at a single 0.5-V supply voltage at room temperature and achieves 1.52-μW/MHz active energy in a write cycle and 72.8-μW leakage power, which are 59.4% and 26.0% better than the conventional write-back scheme. The total energy is 12.9 μW/MHz at 0.5 V in a 50%-read / 50%-write operation.

Chapter 4 Bitline Limiting Technique for Low-Power 8T SRAM

This chapter presents a description of two bitline limiting techniques to improve SRAM energy efficiency in nanometer CMOS process:

1) Read Bitline Amplitude Limiting (RBAL) Scheme
2) Selective Source Line Control (SSLC) Scheme

4.1 Read Bitline Amplitude Limiting (RBAL) 8T SRAM

4.1.1 Read Bitline Amplitude Limiting Scheme

Figure 4.1 illustrates an RBAL and novel DA scheme, which consist of only three NMOSes. The gate and drain of RBAL are connected respectively to RBL and virtual footer (VFT). In a 1-read operation, the RBLs are pulled down by the activated read ports. Figure 4.2 presents the waveforms of RBL with RBAL and without the DA scheme. Although the slowest cell is discharging the RBL, the other RBLs are pulled down faster. However, the discharge is stopped by the threshold voltage of RBAL. The decrease of average swing in RBL improves the dynamic energy. The single-ended 8T cell generally uses an inverter as a sense amp. Consequently, there is delay overhead when the RBL ranges under middle voltage. To prevent the delay degradation, the novel DA scheme is proposed. The DA terminals are connected to RBAL, VFT, output of sense-amp (= inverter) and enable signal (EN). When the output voltage is over the threshold voltage of the NMOS and the EN signal is activated, the RBL and the VFT are shorted by the two series of NMOSes. The DA scheme improves the read bitline delay presented in Fig. 4.3.

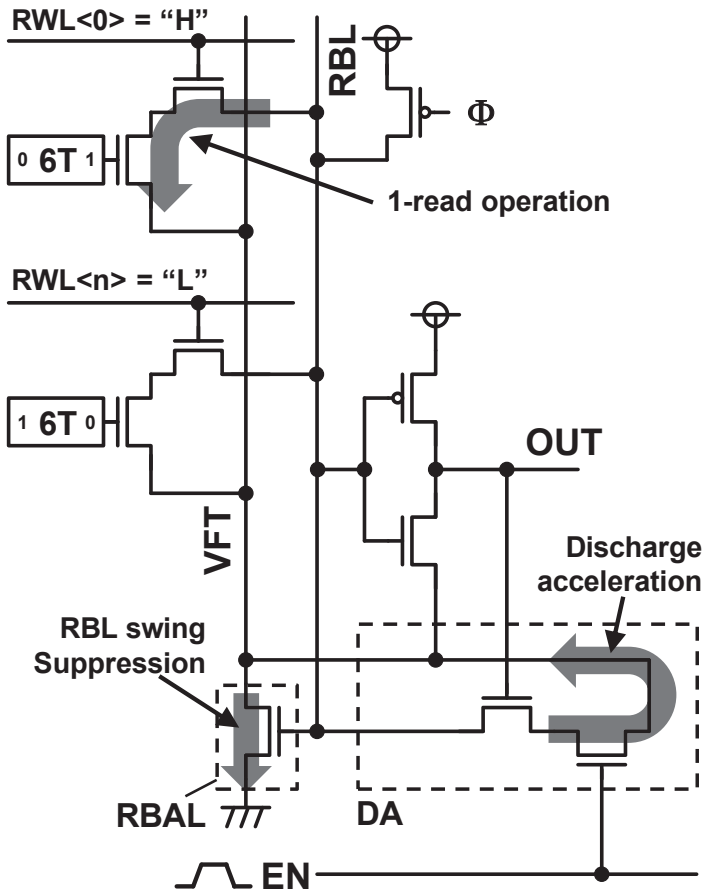


Fig. 4.1 Circuit diagram of RBAL and discharge acceleration (DA) scheme.

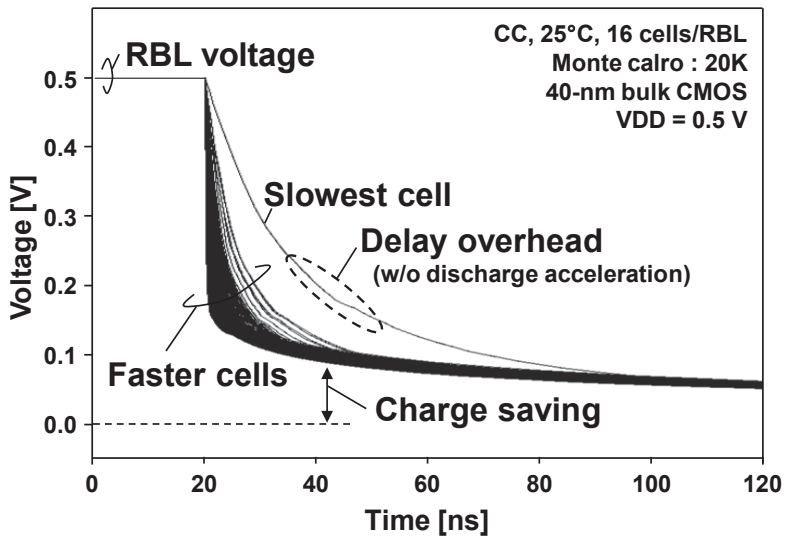


Fig. 4.2 Waveforms of read bitline in proposed 8T cell with read bitline limiter.

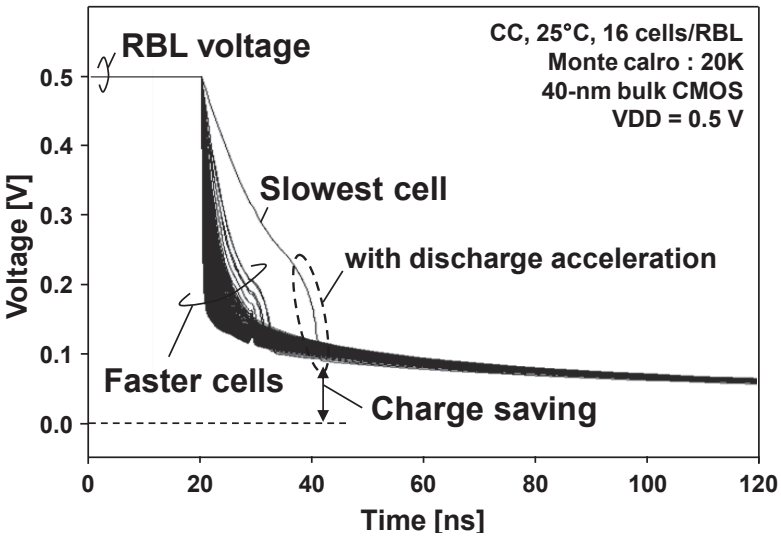


Fig. 4.3 Waveforms of read bitline in proposed 8T cell with read bitline limiter and assist circuit.

Figure 4.4 illustrates RBL delay versus width of the RBAL. Smaller RBAL increases the threshold variation. However, longer RBAL increases the capacitance of RBL. Herein, the width of RBAL is optimized by the RBL delay.

Figure 4.5 presents the minimum drain current (I_{on}) and maximum leakage current (Ioff) of the read port in the 8T cell. The number of 8T cells in a RBL is 16. The red line and blue line respectively indicate the minimum Ion and Ioff in a conventional 8T cell. The proposed scheme with RBAL and DA decreases the minimum Ion by 0.92% and increases the maximum I_{off} by 32%, however, the Ion is two orders of magnitude larger than I_{off}.

Figure 4.6 shows waveforms of the slowest cell in conventional, RBAL without DA and RBAL with DA when 20-K Monte-Carlo analyses are executed at CC, 25°C. In this paper, T_{delay} is defined by the time to which V(OUT) rises to 0.45 V at supply voltage of 0.5 V. The T_{delay} with only RBAL is increased by 12%. However, the T_{delay} with RBAL and DA is decreased by 3%. Table 4.1 shows T_{delay} and active energy (E_{active}) improvement at five process corners and temperatures of three kinds. T_{delay} at the FS corner are increased by 14%-32%, however, T_{delay} at SS corner are improved by 2%–5%. E_{active} are improved by 13%–27% at 0.5 V.

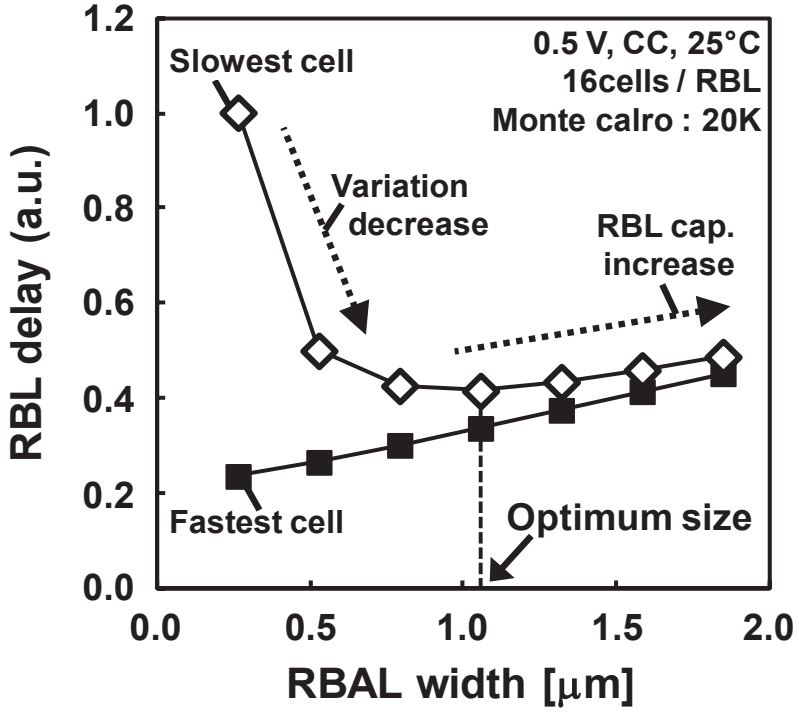


Fig. 4.4 Read bitline (RBL) delay versus the width of the limiter transistor.

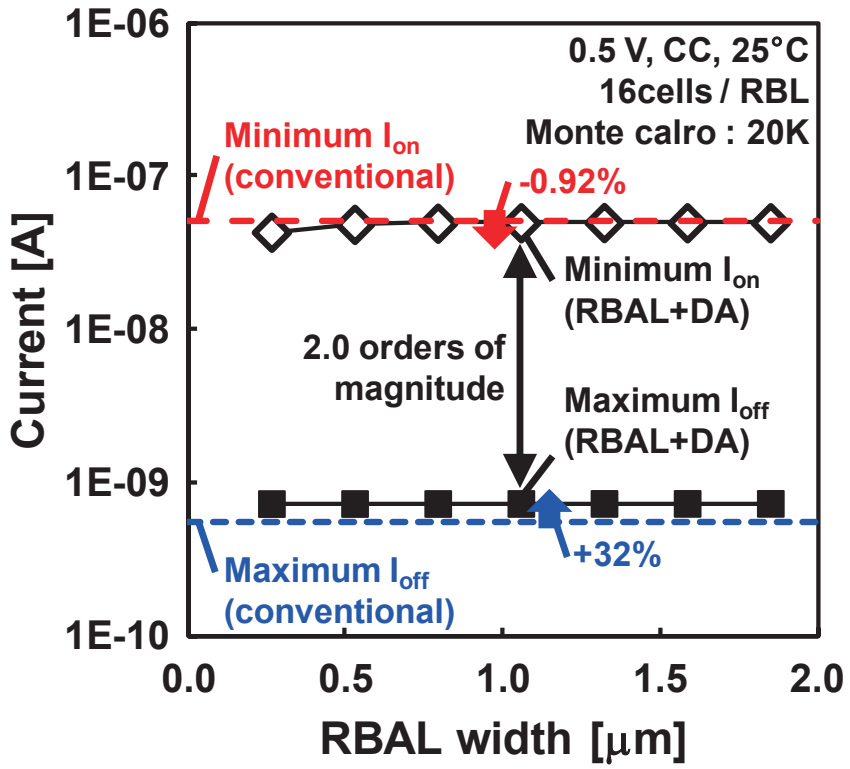


Fig. 4.5 Current margin.

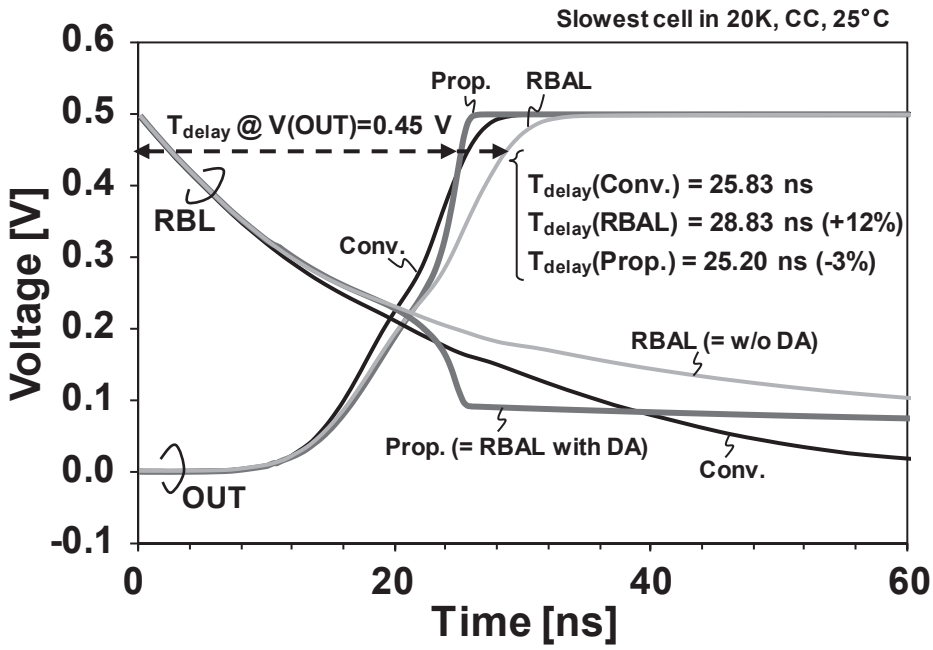


Fig. 4.6 Waveforms of the slowest cell.

Table 4.1 T_{delay} and E_{active} comparison.

		T_{delay} @ V(OUT) = 0.45 V [ns]			T_{delay} ratio	E_{active} in a RBL [fJ]			E_{active} ratio
		Conv.	RBAL	Prop.	Prop./Conv.	Conv.	RBAL	Prop.	Prop./Conv.
SS	-40	1761.30	2008.00	1700.30	0.97	3.1320	2.3595	2.3398	0.75
	25	145.62	161.31	138.97	0.95	3.1536	2.4799	2.4507	0.78
	125	15.12	16.40	14.75	0.98	3.2174	2.6706	2.6024	0.81
SF	-40	518.29	547.16	457.84	0.88	3.1482	2.3205	2.2916	0.73
	25	55.01	58.33	49.26	0.90	3.1997	2.4681	2.4204	0.76
	125	7.28	7.74	7.74	1.06	3.2968	2.6722	2.6722	0.81
CC	-40	175.97	205.83	173.40	0.99	3.1439	2.3748	2.3439	0.75
	25	25.83	28.83	25.20	0.98	3.1822	2.5260	2.4716	0.78
	125	4.52	4.91	4.91	1.09	3.2884	2.7589	2.7589	0.84
FS	-40	53.41	86.61	70.62	1.32	3.1525	2.4406	2.4035	0.76
	25	11.35	14.54	13.61	1.20	3.2028	2.6159	2.5188	0.79
	125	2.69	3.07	3.07	1.14	3.4060	2.9409	2.9409	0.86
FF	-40	16.04	18.91	16.78	1.05	3.1970	2.4570	2.3821	0.75
	25	4.51	5.02	5.02	1.11	3.2668	2.6497	2.6497	0.81
	125	1.36	1.47	1.47	1.08	3.4509	2.9605	2.9605	0.86

4.1.2 Chip Implementation and Measrement Results

We designed and fabricated a 256-Kb SRAM macro in a 40-nm bulk CMOS process, as presented in Fig. 4.7. Table 4.2 shows the test chip configuration: The macro size is 0.566 mm × 0.976 mm, the 256-Kb SRAM macro consists of 128 rows × 128 columns × 16 banks, the 8T cell size is 0.706 μm^2 based on logic rule, and the cell density is 463 Kb / mm^2. Figure 4.8 illustrates 16-Kb sub block with the proposed circuit: RBAL and DA. The sub block consists of 16 local cell array (8 columns × 128 rows). Figure 4.9 illustrates a local cell array, which includes the local read circuit, RBAL, DA and low-swing bitline driver (LSBD) which achieves low-power write-back function. At a write cycle, a RWL is activated and an LSBD drives a pair of WBL/WBLN in a half-selected column according to the readout data. Figure 4.10 illustrates the circuit details. The global RBL (GRBL) is not activated during the write cycle to suppress the energy dissipation. The RBAL and DA transfer the readout datum to the LSBD at the write cycle and to GRBL at the read cycle. The LSBDs are activated only in half-selected columns according to the column line enable (CLE) and drive enable bar (DRN). In write target columns, CMOS write drivers activate the write bitlines so the write margin is not degraded. Figure 4.11 shows the measured energy dissipation per cycle (R:W = 50:50) in the minimum operation voltage (VDD_{min}) of 10 MHz, 20 MHz and 100 MHz at room temperature (RT). The measurement results are investigated using 16 sample chips. Consequently, the energy consumption is less than 10 pJ / access at 0.5–0.7 V.

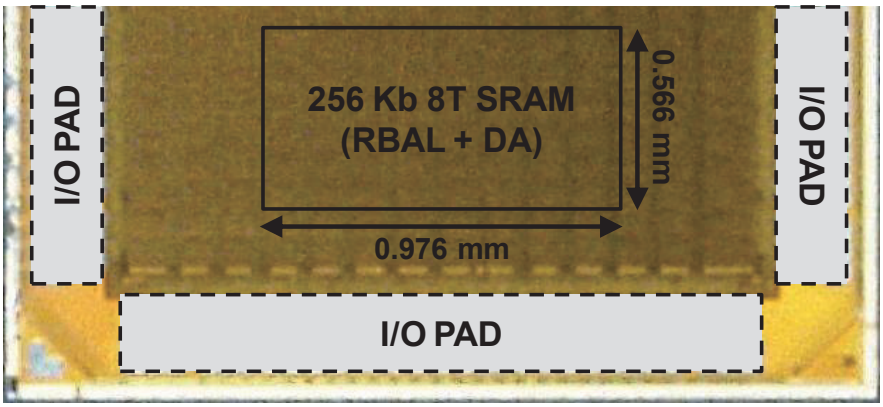


Fig. 4.7 Die photograph of the test chip.

Table 4.2 Test chip configuration.

Technology	40 nm bulk CMOS
Macro size	0.566 mm x 0.976 mm
Macro configuration	256 Kb (16Kb x 2 x 8), 16 bits/word
Cell size	0.706 μm^2 (logic rule)
# of cells/BL	16 (RBL), 128 (WBL)
Density	463 Kb/mm^2

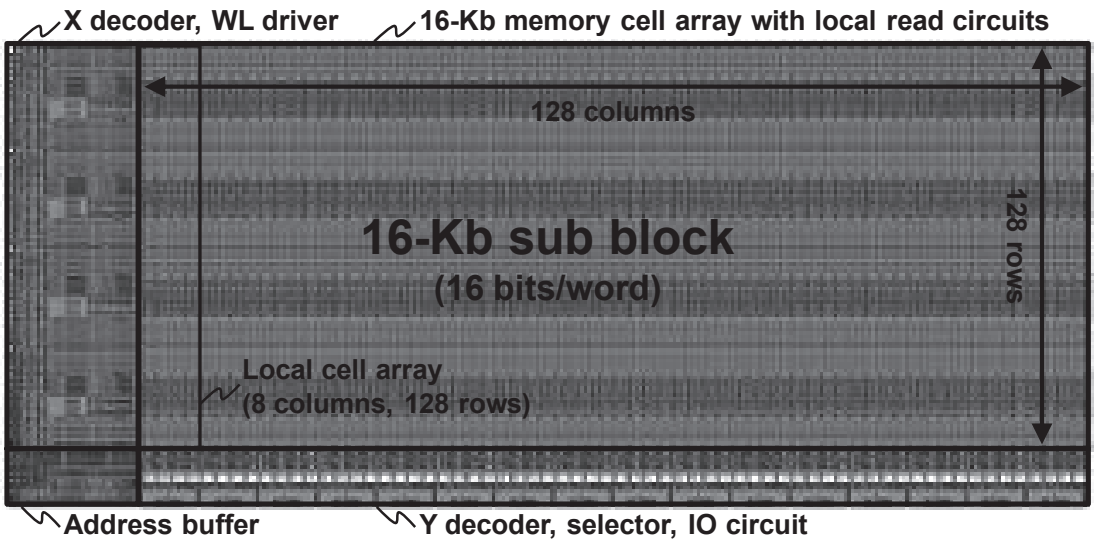


Fig. 4.8 16-Kb sub block with the proposed circuitry.

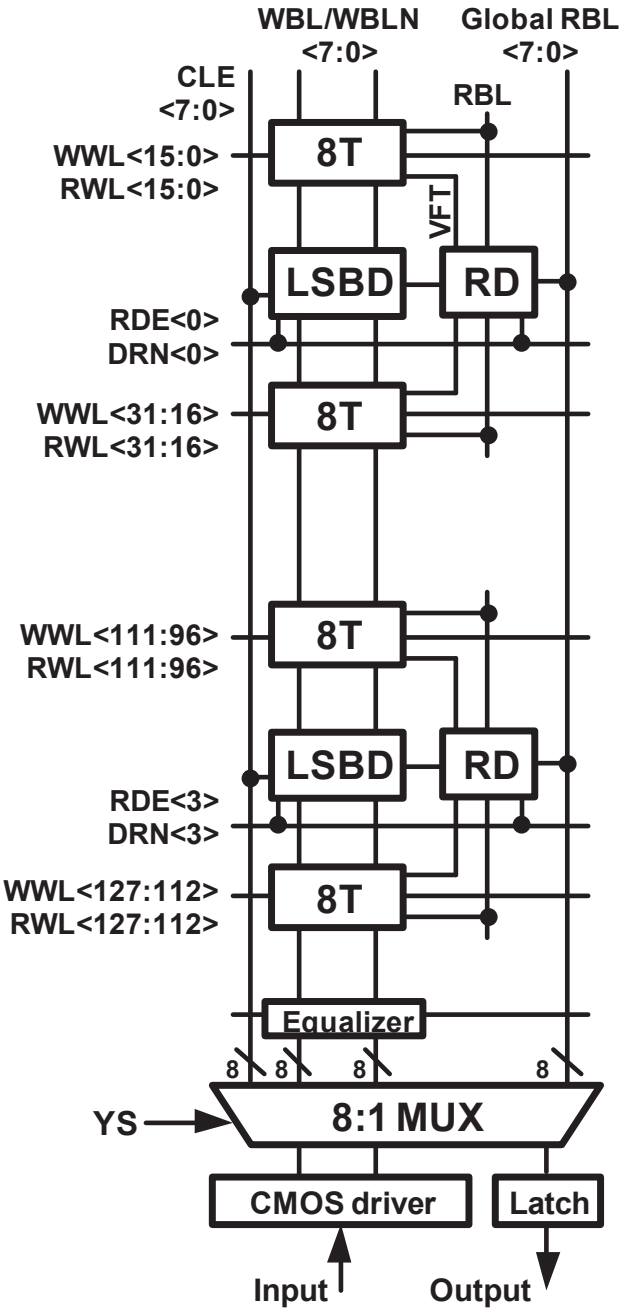


Fig. 4.9 Diagram of local cell array.

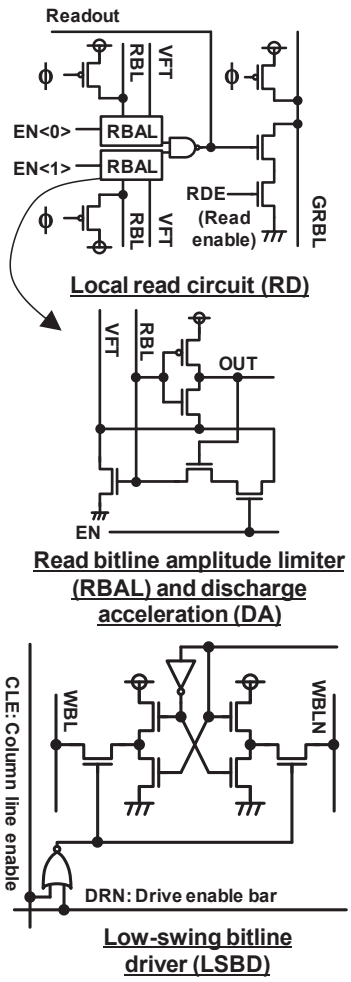


Fig. 4.10 Diagram of the proposed circuits and low-swing bitline driver (LSBD) to prevent the half-select problem.

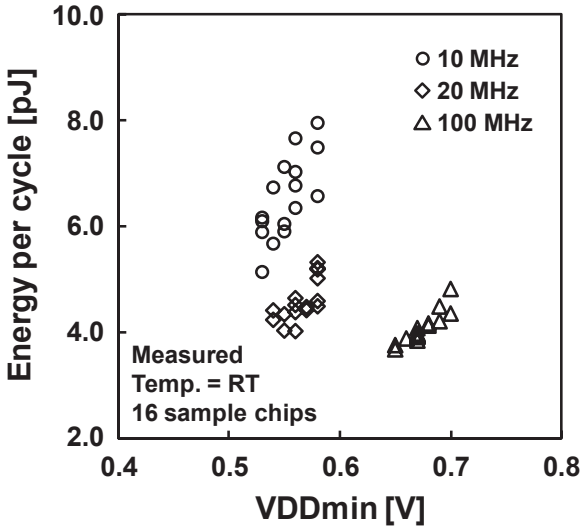


Fig. 4.11 Measured energy dissipation per cycle (R:W = 50:50) at the minimum operation voltage (VDDmin) at room temperature (RT).

4.2 Selective Source Line Control of Read Bitlines and Address Preset Structure

4.2.1 Successive Read Operation

Instead of the conventional 6T SRAM, a single-ended 8T SRAM is also widely used even as a single-port memory leveraging disturb-free dedicated read ports [36]. Another advantage of the 8T SRAM is that a "1" readout consumes no dynamic power because a read bitline maintains a precharging voltage [37].

In this section, a partially discharging 8T SRAM with a selective source line control (SSLC) scheme is proposed. The proposed scheme cuts off SLs of the dedicated read ports selectively according to a column address. The proposed SSLC improves energy efficiency in a successive read operation of an instruction cache or video processing. In the incremental address access, only a row address (= less significant address bits) is frequently changed, as presented in Fig. 4.12, where a column address is changed only slightly. Our proposed work improves the energy efficiency of successive read operations.

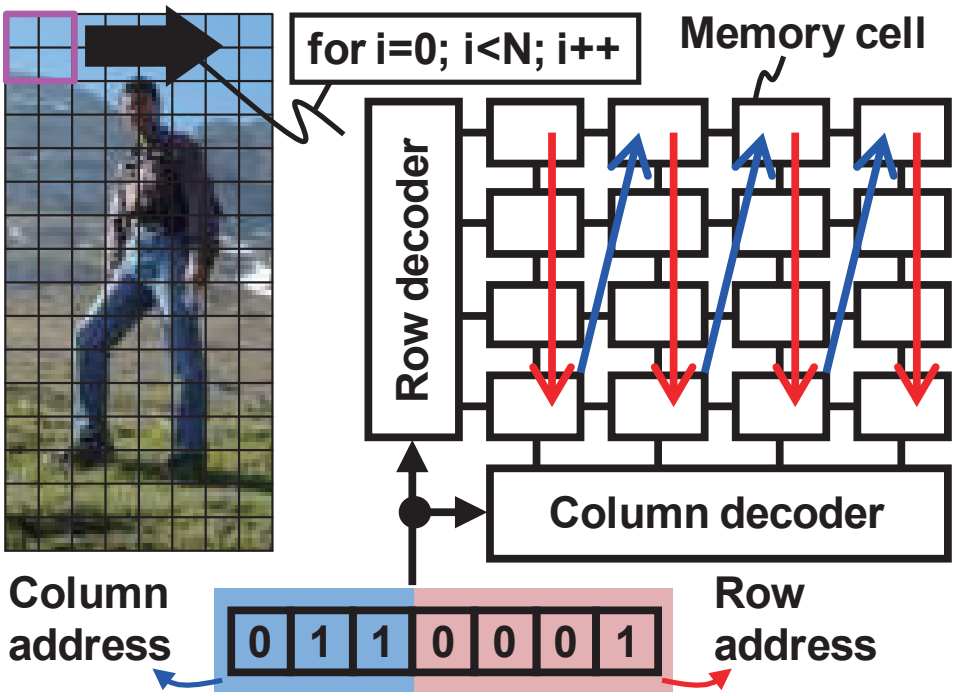


Fig. 4.12 Successive memory access in video processing.

4.2.2 Selective Source Line Control (SSLC) scheme

Figure 4.13 illustrates an array of the 8T cells with a commonly used interleaving structure. The SLs of the dedicated read port are always grounded in the conventional structure. Although a selected local read bitline (RBL) is merely connected to a global RBL by a multiplexer, the other local RBLs in the unselected columns are discharged, which is not necessary for the read operation.

Figure 4.14 illustrates the concept of the proposed SSLC scheme. The SL is a shared virtual ground line of the dedicated read ports in a single column of the 8T SRAM array. An NMOS switch and an OR gate are inserted in every column. The switch is turned on selectively or is kept off according to a column address. In a standby mode, the SLs are grounded to prepare upcoming random access; the SL might, however, be floated if one-clock wakeup is not needed. In the write operation, the SLs are grounded because the 8T SRAM employs a disturb mitigation scheme with write back to eliminate a half-select problem [14]. For that reason, the OR gate has a write enable (WE) input. Although the SSLC circuit must be implemented in every column, the area overhead is 0.7% in our design. Figures 4.15(a)–4.15(c) respectively show schematic, FEOL, and BEOL layouts of the proposed 8T cell with an SL. In the conventional 8T cell, a ground line of the dedicated read port can be shared with an adjacent cell. However, in the proposed 8T cell, the SL must be separated. In contrast, no area overhead exists in adding the SL. In our design, the cell size is 1.01 μm^2 in a logic rule, which is slightly larger than the conventional one because the transistor length is relaxed for low-leakage operation.

Figure 4.16 shows operating waveforms of wordline, RBL, and SL of a selected and unselected columns, in which cells have all “0” data. In the selected columns, the bitlines are pulled down and discharged. They are then precharged for subsequent operations. In unselected columns, the bitline is not fully discharged. Its swing is suppressed because the SL is floated by the SSLC.

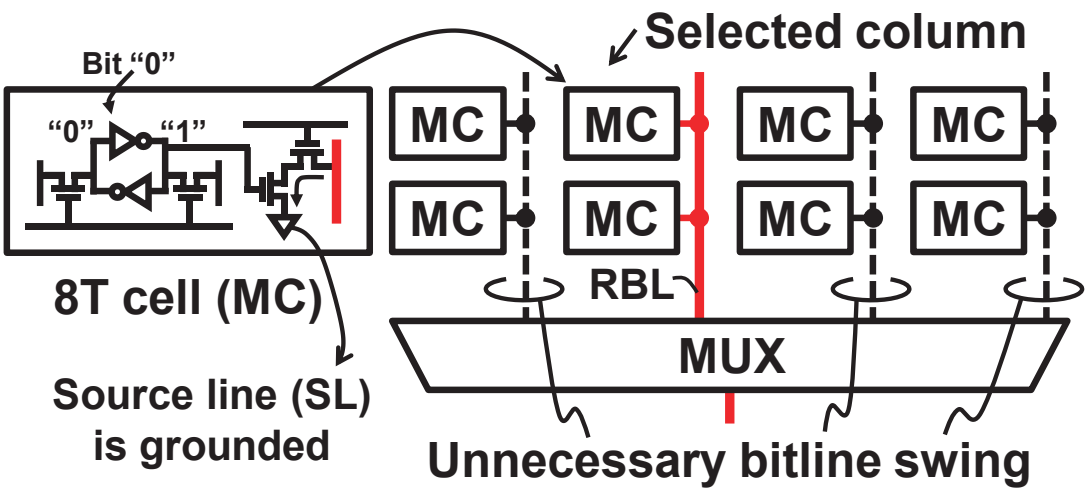
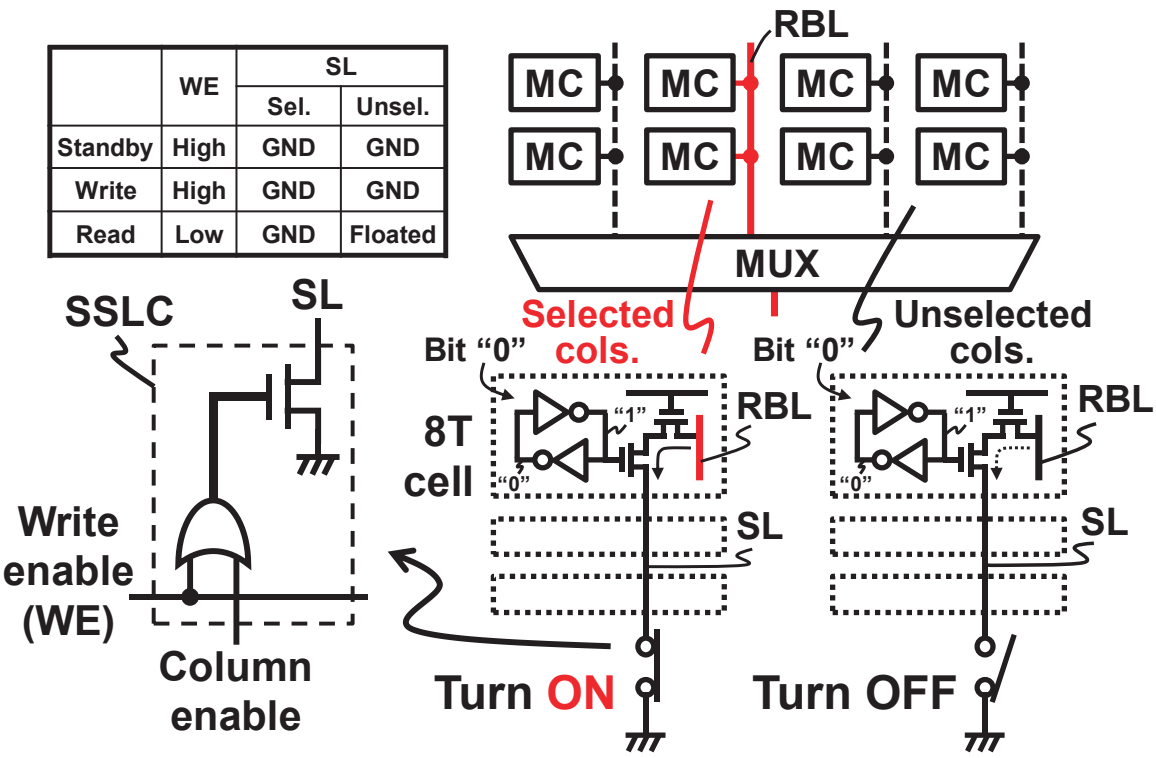


Fig. 4.13 Conventional 8T memory cell array. Bit "0" discharges a read bitline (RBL).



	WE	SL	
		Sel.	Unsel.
Standby	High	GND	GND
Write	High	GND	GND
Read	Low	GND	Floated

Fig. 4.14 Conceptual diagrams showing the proposed partially discharging 8T SRAM with the selective source line control (SSLC) scheme in read operation.

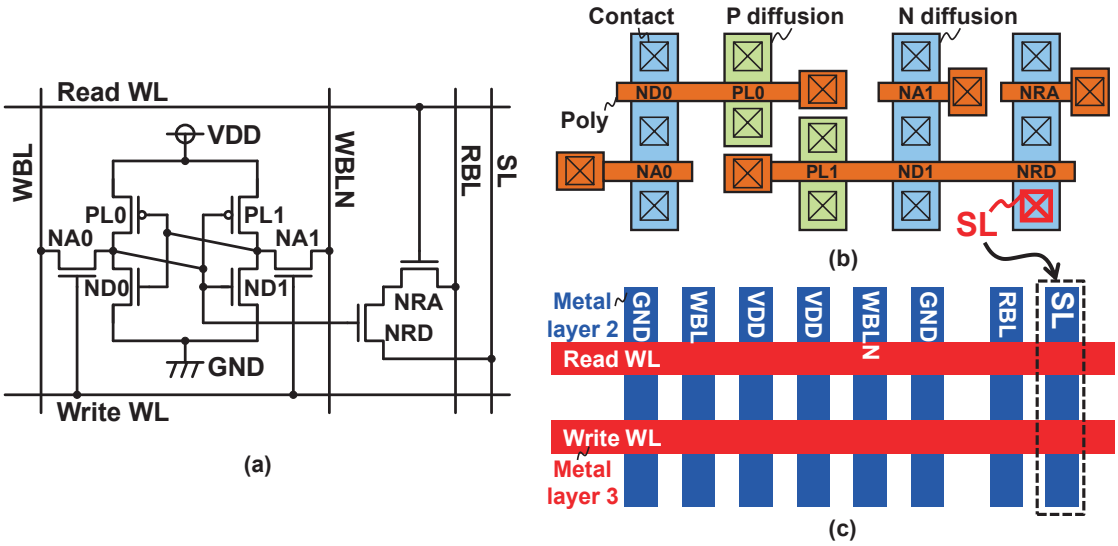


Fig. 4.15 (a) Schematic, (b) FEOL, and (c) BEOL layouts of the proposed 8T cell with a separated source line (SL).

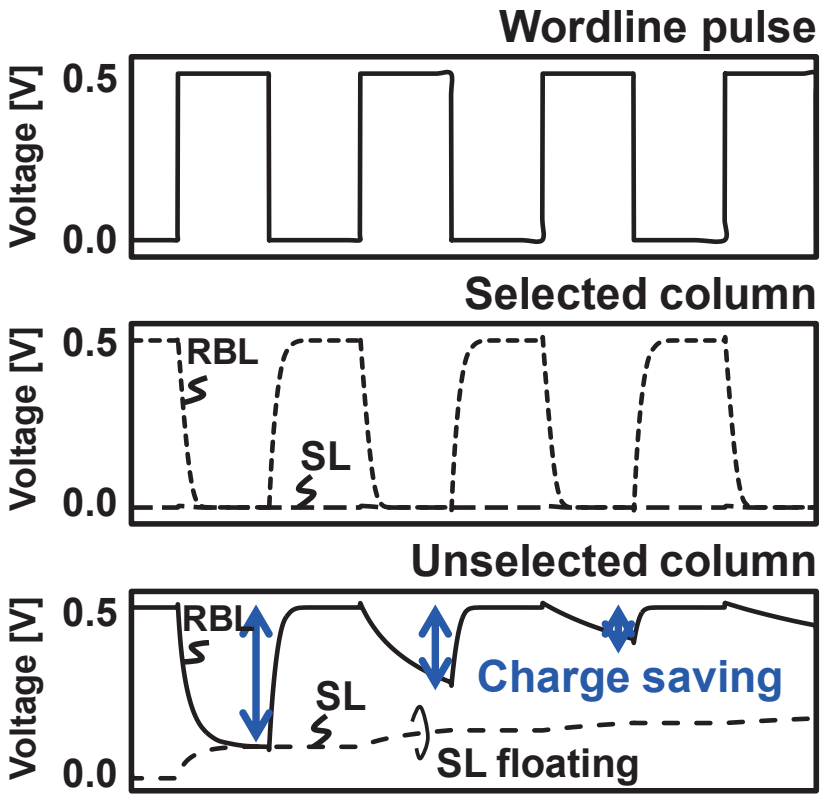


Fig. 4.16 Waveforms of wordline, read bitline (RBL), and source line (SL) of selected and unselected columns in consecutive “0” read operations.

4.2.3 Address Preset Structure

Figure 4.17 shows an important shortcoming of the SSLC scheme: the access time penalty. Before read operations, the SL must be grounded in the selected column. This SL activation demands extra access time. In this subsection, an address preset structure is presented to eliminate the access time penalty caused by SL activation. The proposed structure leverages an access address (= an address accessed at the present cycle: ADD_{acc}) and a preset address (= an address accessed at the next cycle: ADD_{pre}) as shown in Figs. 4.18(a) and 4.18(b). In particular in a video memory or a memory shared by many cores, an address accessed in the next cycle can be preset because the memory access is algorithmic or is stored in a queue. In such a case, the ADD_{pre} can be fed in a negative edge of the clock and the SL in the column accessed at the next cycle can be grounded preliminarily to prepare for the next positive edge. The address preset structure eliminates the access time penalty in the SSLC mode when the address accessed at the next cycle can be preset. The area overhead of the address preset structure is less than 1% in the SRAM macro.

In Fig. 4.18(a), the ADD_{acc}, which is the present address, receives an ADD_n on the first positive edge. It can then preset an ADD_{n+1} for the next cycle because it is fixed on the negative edge of the clock. The SL is always grounded before access in the successive read operation. Consequently, the SSLC with the address preset structure improves the energy efficiency with no access time penalty.

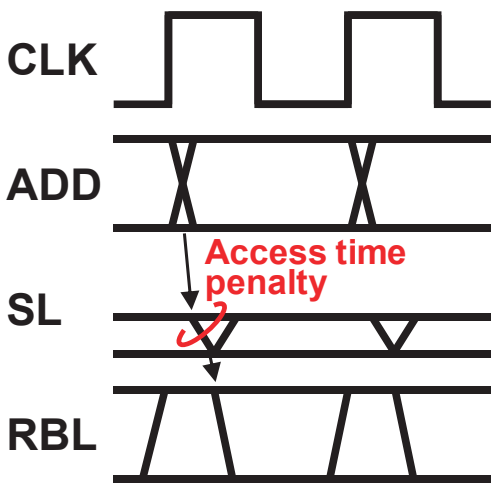


Fig. 4.17 Access time penalty in the SSLC scheme.

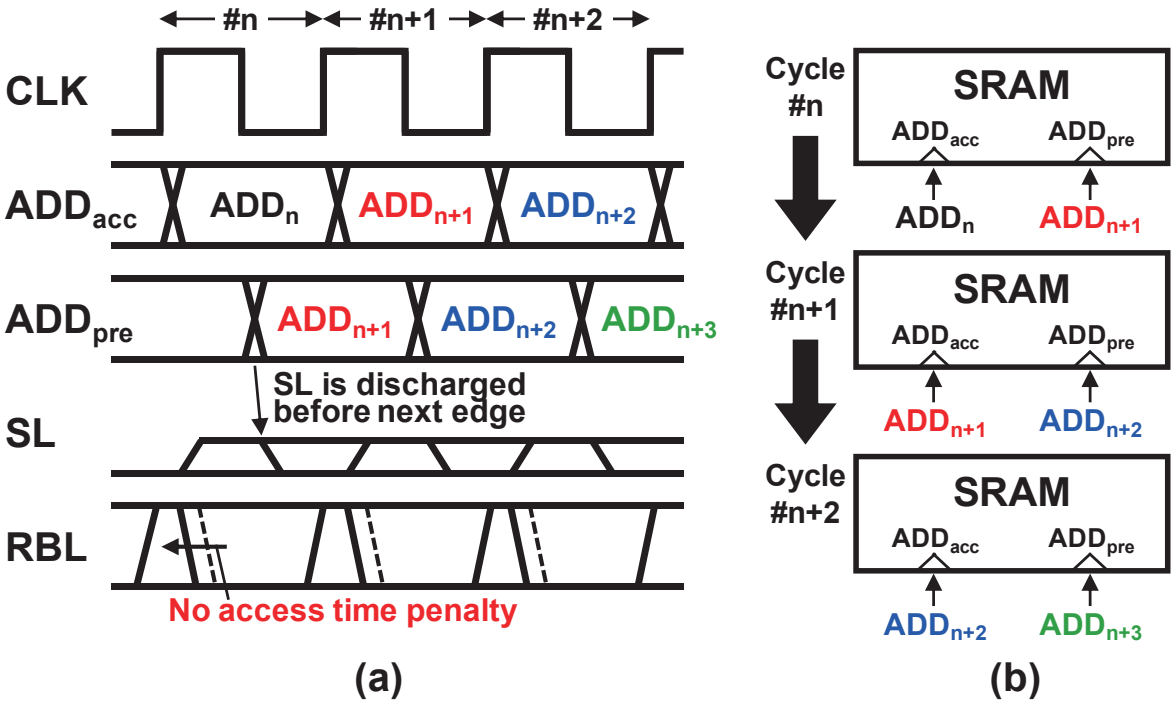


Fig. 4.18 (a) Waveforms and (b) timing behavior of the SSLC scheme with the address preset structure.

4.2.4 Chip Implementation and Measurement Results

We implemented a 16-Kb 8T SRAM test chip using a 40-nm CMOS process as presented in Fig. 4.19. The macro size is 128 μm × 280 μm. The 8T SRAM consists of 16 bits / word × 1 K words (128 rows × 128 columns). An SRAM sub-array (128 rows × 8 columns) has a multiplexer that selects a column for an input or output datum. Figure 4.20 presents a schematic of the proposed 8T SRAM with the SSLC and the low-energy disturbance mitigation scheme [14]. A pair of write bitlines (WBL/WBLN) and an SL are shared by 128 cells in a column. A local RBL is shared by 16 cells and a NAND gate transports the readout datum to a global RBL driver. In the write operation, the write-back driver drives the WBL pair as to the original readout data to prevent the half-select issue. In a write cycle, all SLs are grounded for the write-back operation, as described in the previous section.

Figures 4.21 and 4.22 respectively present access patterns in the measurements and measurement results in the successive read operation. The gray and the black bars in Fig. 4.22 respectively show active and leakage energies per cycle. In the measurements, four

data and access patterns are used.

- In the all-zero (ALL0) data with a fixed address pattern, only selected RBLs are merely discharged because an access address is fixed. The other RBLs remain floating because they are always unselected. In this case, the proposed SSLC effectively reduces the read energy by 57.2%.
- The RBL remains "1" in the all-one (ALL1) data pattern. One fixed address is accessed continuously. In this case, the SSLC does not work because all the RBLs keep the precharged voltage. Therefore, the power reduction is 0.0%.
- The checkerboard pattern using incremental row address (CKB X+) has 50% "0" data. The measurement result demonstrates the SSLC decreases the read energy by 45.0% in this case.
- In the CKB using incremental column address (CKB Y+), the column address is changed at every cycle. The SLs cannot be floated for a long time; the power reduction is less effective than ALL0 and CKB X+ patterns. The reduction is 28.5% in the pattern.

On average of the four patterns, the proposed SSLC reduces the energy consumption by 38.1% in the successive read operation. Table 4.3 presents the test chip characteristics.

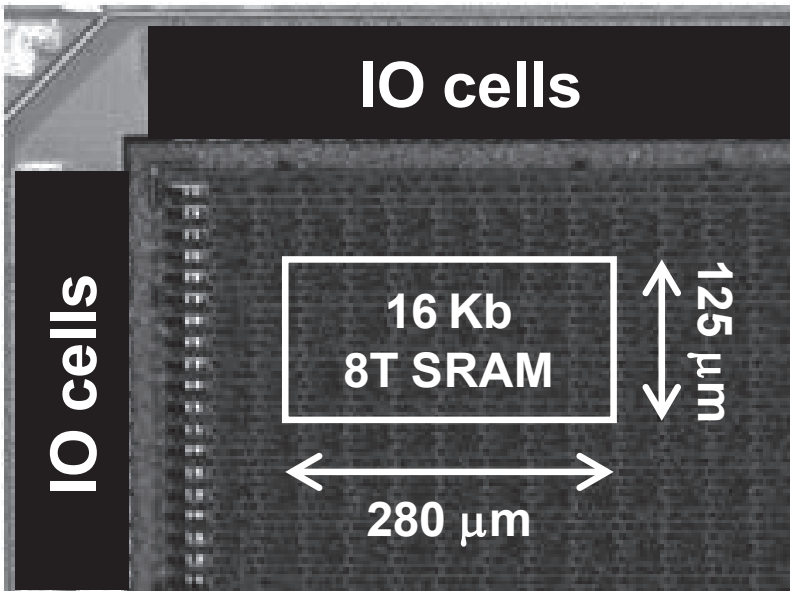


Fig. 4.19 16-Kb 8T SRAM test chip.

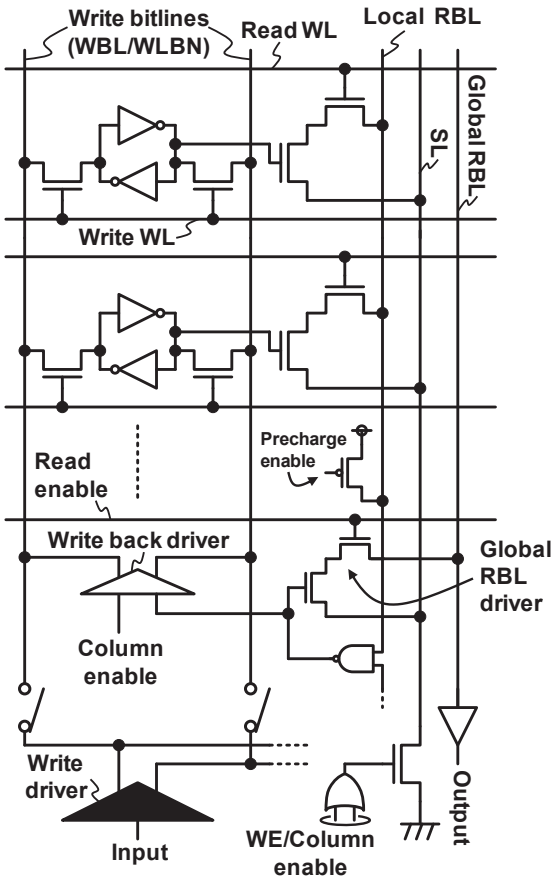


Fig. 4.20 Schematic of the proposed 8T SRAM with the SSLC and the disturbance mitigation scheme.

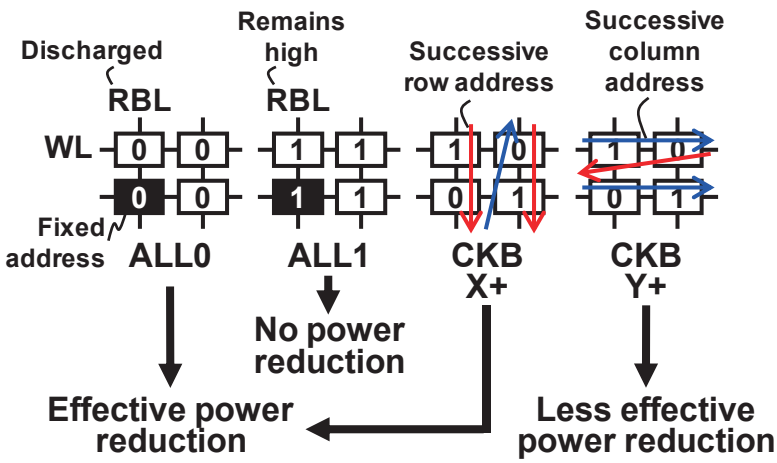


Fig. 4.21 Access patterns in the energy measurement. The proposed SSLC is effective in the all-zero (ALL0) and the checkerboard X address increment (CKB X+) patterns than the other two patterns.

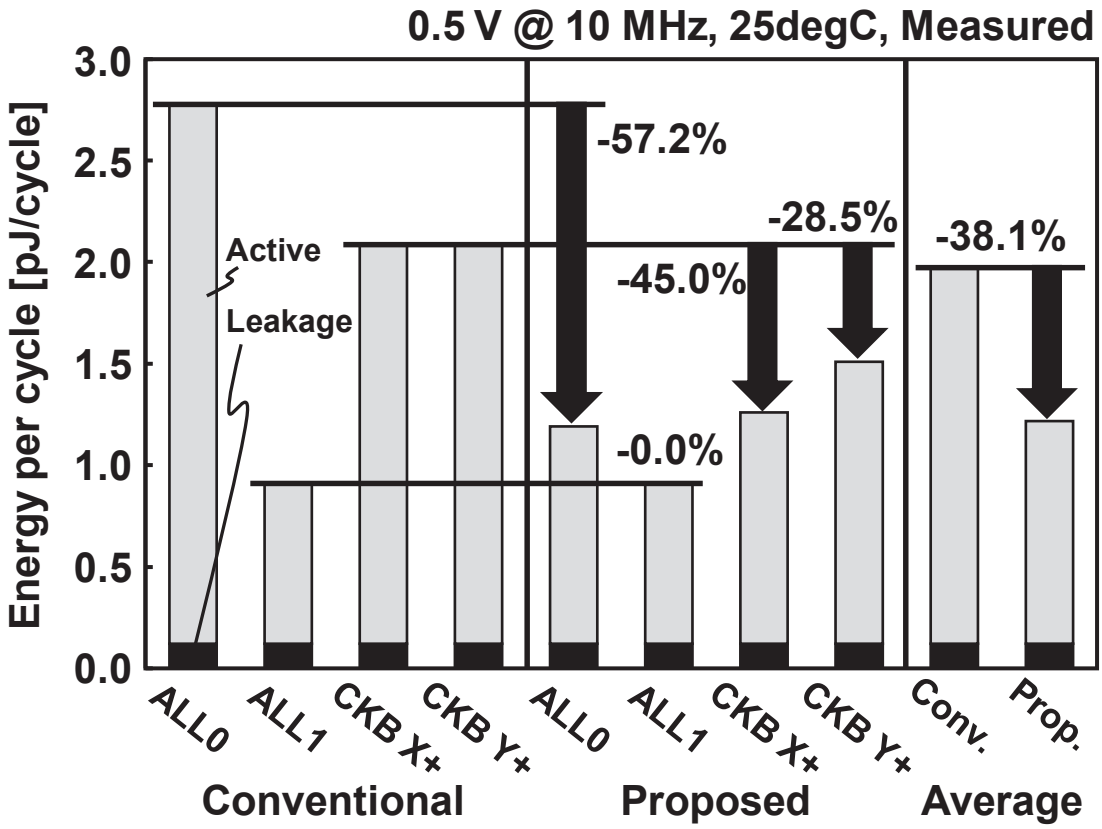


Fig. 4.22 Measurement results of the implemented test chip in read operation.

Table 4.3 Features of a test chip.

Technology	40 nm bulk CMOS
Macro size	125 μm × 280 μm
Macro configuration	16 Kb (16 bits/word, 1 K words)
Cell size	1.01 μm^2 (logic rule)
# of cells / BL, SL	16 (RBL), 128 (WBL), 128 (SL)
Density	457 Kb/mm^2
Write active energy (CKB)	2.18 pJ @ 0.5 V, 10 MHz, RT
Read active energy (CKB)	1.14 pJ @ 0.5 V, 10 MHz, RT
Leakage energy (CKB)	0.12 pJ @ 0.5 V, 10 MHz, RT

4.3 Summary

As described in this chapter, we proposed two bitline limiting techniques: 1) read bitline amplitude limiter and 2) selective source line control scheme.

1) First, we proposed a read bitline amplitude limiter (RBAL) and discharge acceleration (DA) scheme. The RBAL reduces the active energy dissipation 13%–27% at 0.5 V. The RBAL increases the read delay. However, the DA scheme improves the delay overhead without power penalty. Although the delay overhead with RBAL and DA is 32% at worst case (FS, -40°C), the delay is decreased by 2%–5% at the SS corner. Circuits were implemented to 256-Kb SRAM macros by 40-nm process. The energy dissipation in a cycle is less than 10 pJ / access at 0.5–0.7 V.
2) Second, we presented the selective source line control (SSLC) scheme for an 8T SRAM. The RBL swing is suppressed in an unselected column because the SSLC disconnects the source line (SL) of the dedicated read ports and therefore does not fully discharge the unselected read bitlines (RBL). In addition to the SSLC, the address preset structure is introduced to address the access time penalty, which best matches with the SSLC. The 16-Kb 8T SRAM test chip implemented in a 40-nm bulk CMOS technology demonstrates that the SSLC with the address preset structure reduces read energy consumption by 57.2%, 0.0%, 45.0%, and 28.5% in ALL0, ALL1, and CKB0 row address increments, and the CKB0 column address increment, respectively. On average, the proposed scheme exhibits a 38.1% energy reduction in successive addresses accessed, compared with a conventional 8T SRAM.

Chapter 5 Margin Enhancement Techniques for Bit-Error and Soft-Error Tolerant SRAM

This chapter presents a description of two margin enhancement techniques to improve bit-error and soft-error rates of SRAM in nanometer CMOS process:

1) Bit-error and soft-error tolerant 7T/14T dependable SRAM
2) Soft-error resilient 8T SRAM bitcell layout with a divided wordline structure

5.1 Bit-Error and Soft-Error Tolerant 7T/14T Dependable SRAM

5.1.1 7T/14T Dependable SRAM

We have proposed a 7T/14T (7-transistor / 14-transistor) SRAM with a dependable mode for low-voltage operation [38]. Figure 5.1 illustrates the 7T/14T SRAM structure. As well as the conventional 6T cell, the normal mode allocates one bit in a 7T cell while the dependable mode does so in a 14T cell by enabling a CTRL signal (CP0 and CP1 are activated). In the 14T dependable mode, either wordline, WLA or WLB, is asserted, which enlarges an SNM because a β ratio (a ratio of the driver transistor's size to the access transistor's size) is doubled. Thus, the reliability of the proposed cell can be dynamically changed depending on an operating condition. For instance, the 7T/14T SRAM is able to be implemented as on-chip cache memory on a processor with dynamic voltage and frequency scaling (DVFS) [39].

In this section, with 150-nm FD-SOI 7T/14T SRAM test chips, we present not only a BER improvement but also mitigating alpha- and neutron-induced SER. We will show experimental results that the 14T dependable mode is superior to ECC and TMR in terms of BER. The respective alpha- and neutron-induced SERs in the 14T dependable mode are suppressed by 80.0% and 34.4% over the 7T normal mode because Q_{crit} in the 14T mode is increased by 70%, at a supply voltage of 0.3 V. Namely, the proposed 7T/14T SRAM is a dynamically hardenable device. This paper reports measurement results of a specific 150-nm FD-SOI memory; however, they will be useful for FD-SOI designers.

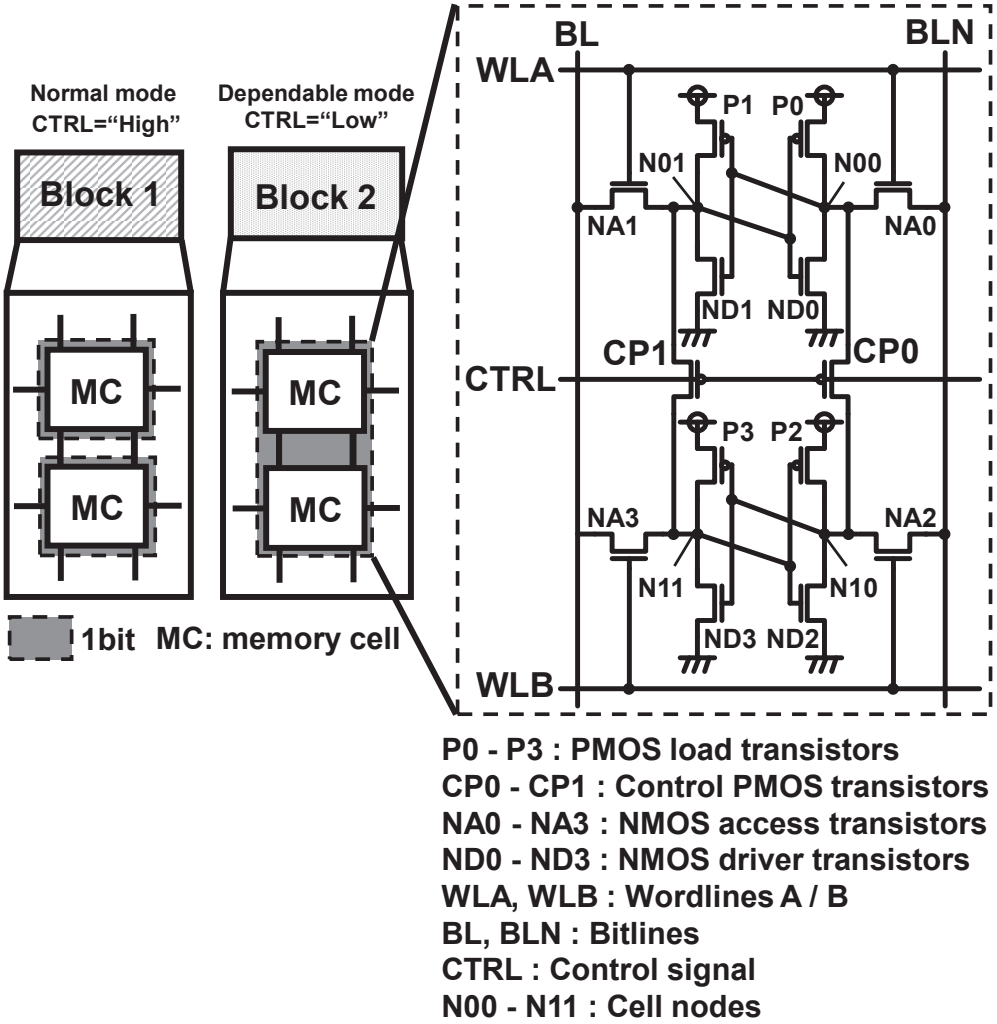


Fig. 5.1 Structure of 7T/14T SRAM cell [38].

5.1.2 SRAM structure

We designed and fabricated a 576-Kb SRAM macro (512 rows × 128 columns × 9 banks) with a nominal supply voltage of 1.5 V in a 150-nm FD-SOI process. Figures 5.2(a)–5.2(c) illustrate the implemented chip micrograph, a block diagram of a 64-Kb bank, and 7T/14T SRAM cell layout, respectively. The SRAM adopts bit-interleaving technique for preventing multiple-cell upset (MCU) [40]. The 7T/14T cells are accessed by bitlines (BL/BLN), wordlines (WLA/WLB), and control signal (CTRL). Since the SRAM cell is inter connected by layer-1 metal, the bitlines vertically tracks with layer-2

metals; then the wordlines and control signal are horizontally connected using layer-3 metals. The layout is based on a logic rule; the area overheads are 9.5% and 119% in the 7T and 14T cells, respectively, over the 6T cell. In contrast, the power of the 14T cell is reduced by 40% because its minimum operating voltage is lower than that of the 6T cell. The double area overhead of the 14T cell might affect manufacturing defects; however, in this paper, we will focus on the investigations of the BER and SER.

Figure 5.3 shows operating waveforms of the 7T/14T SRAM in the write, read, and standby cycles. When the CTRL signal is disabled (CTRL is "high"), the SRAM acts as the 7T normal mode. In this case, the SNM and Q_{crit} are quite similar to those in the conventional 6T cell. In the 14T dependable mode, the both wordline, WLA and WLB, are simultaneously activated in the write cycle, and a single wordline, WLA, is enabled in the read cycle; thus, the write margin and SNM are enlarged, compared to the 7T mode. The CTRL signal is kept active (= "low") during a standby state in the 14T dependable mode, which improves a retention margin.

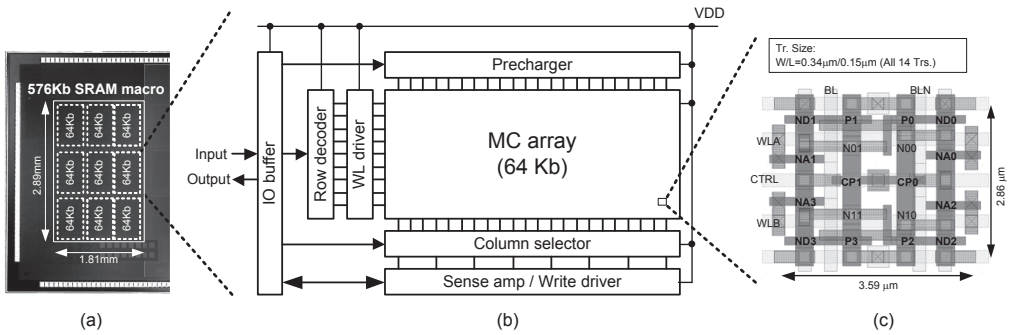


Fig. 5.2 (a) Chip micrograph, (b) block diagram of 64-Kb bank, and (c) 7T/14T SRAM cell layout (based on logic rule).

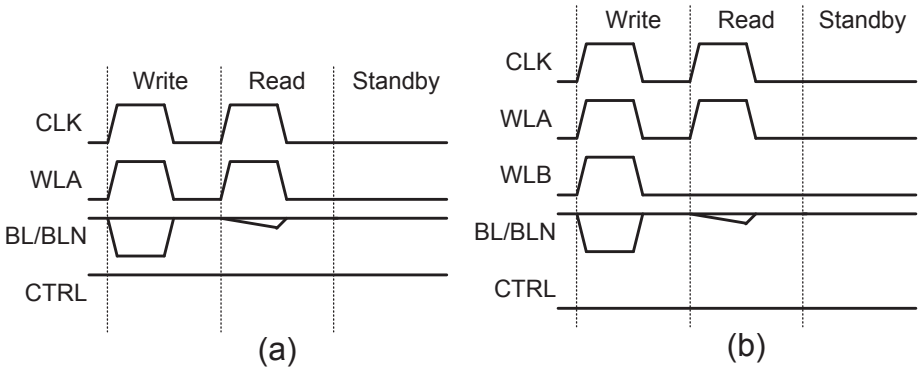


Fig. 5.3 Operating waveformes of (a) 7T normal mode and (b) 14T dependable mode.

5.1.3 Device Simulation Results

In this section, we will present mixed-mode simulation results that the 14T dependable mode is superior to the 7T normal mode at SEU tolerance. Figure 5.4(a) illustrates a Synopsys TCAD model [41] of ND1. The other transistors in SRAM latches (P0, P1, P2, P3, ND0, ND2, ND3, CP0, and CP1) are based on FD-SOI SPICE models as presented in Fig. 5.4(b). In other words, the simulation runs in the mixed mode (TCAD model plus SPICE models). It is well known that an nMOS driver transistor connected to an "H" internal node is the most sensitive one to an SEU [42]. In this simulation, ND1 corresponds to it when N01 is "H", on which the TCAD simulation should be carried out to evaluate its nucleus reaction and secondary-ion particle transportation. The device profile and the SPICE models are provided by a foundry.

We simulate that an alpha particle whose LET is 0.1 pC/um perpendicularly strikes the channel center of ND1. Figure 5.5 shows waveforms of internal nodes (N00 and N01) in the 7T/14T SRAM cell. When N01 (N00) is high (low), the ND1 transistor that has the N01 node is the most sensitive to the SEU; it is pulled down to the ground if a heavy ion strikes the ND1 transistor. The datum in the 7T cell (7T per bit) is possibly flipped by this disturb current. However, that in the 14T dependable cell can be sustained by compensating current flowing through the connecting pMOS, CP1.

We investigated the LET threshold (LET_{th}) and Q_{crit}; they were calculated by the following equations:

$$LET_{th} = \min(LET\,|_{SEU\ happens})$$

$$Qcrit = \min(Deposited\ charge(LET)\,|_{SEU\ happens})$$

$$Depositedcharge\ (LET) = \int_0^{10e-9} id(t, LET)dt$$

$$LET = 10k\,[fC/um]\ (1 \le k \le 15, k \subset N)$$

LET_{th} is a minimum LET in which a SRAM cell is flipped. Q_{crit} is defined as a deposited charge which is an integral of the disturb current.

We simulate the SEU effect over a LET range of 10-150 fC/μm. Figures 5.6 and 5.7 illustrate the simulated LET_{th} and Q_{crit} under 0.3-1.5 V operating voltages (VDD). The LET_{th} is improved by 10-50% and the Q_{crit} is increased by 10-70%. Because an alpha and neutron SERs are logarithmically proportional to Q_{crit} when Q_{crit} is small [43], the SERs is expected to be rapidly decreased on that condition.

In reality, the 14T cell is twice larger than the 7T cell; thus, in the 14T cell, the probability of crossing particles to the nodes turns out double. In the next section, we will compare total SERs between the 7T and 14T cells by experiment.

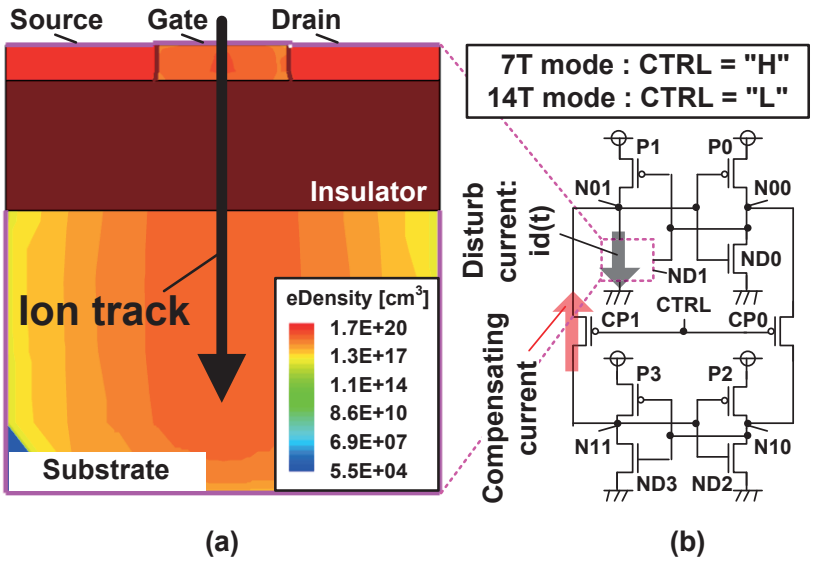


Fig. 5.4 (a) Cross section of nMOS (ND1) TCAD model, and (b) 7T/14T SRAM cell circuit for mixed-mode simulation using tool suite of Synopsys Sentaurus package.

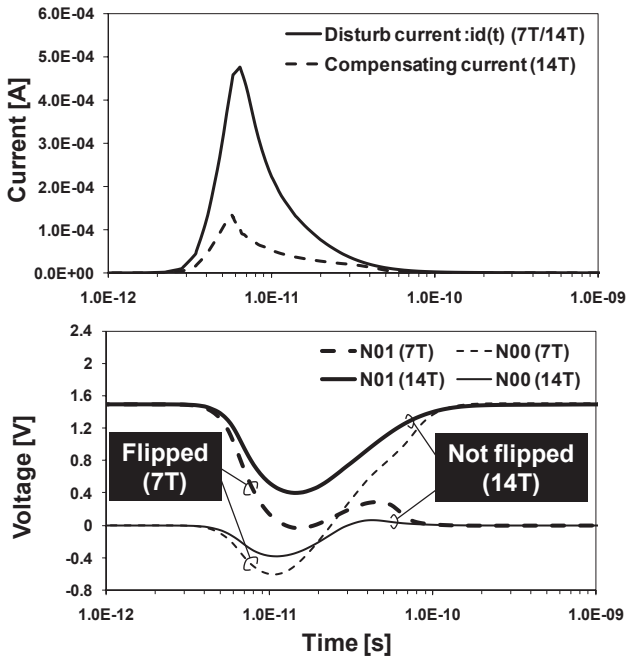


Fig. 5.5 Mixed-mode simultion results on the structure presented in Fig. 5.4. The 14T dependable cell is not flipped due to compensating current flowing through CP1. The heavy ion's LET is 0.1 pC/μm.

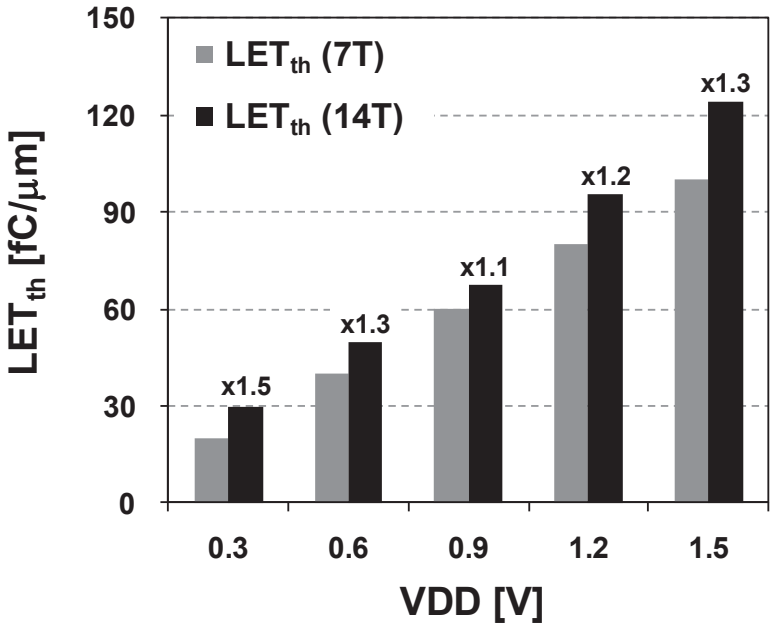


Fig. 5.6 Simulated LET_{th} when VDD is varied. LET_{th} in the14T dependable mode is improved by 10-50% over the 7T normal mode.

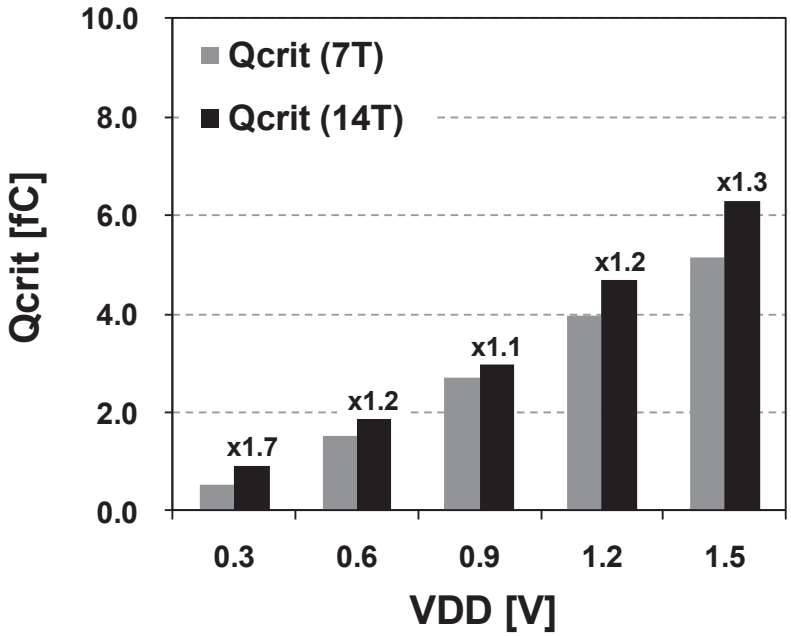


Fig. 5.7 Simulated Q_{crit} when VDD is varied. Q_{crit} in the14T dependable mode is improved by 10-70% over the 7T normal mode.

5.1.4 Bit-Error Rate Measurement Results

Figure 5.8 illustrates the measured BERs in the 7T normal and 14T dependable modes. We took three steps: 1) normal write operation at 1.5 V, 2) dummy read operation for disturbance to SNM at low voltage (VDD < 1.5 V), and 3) read operation at 1.5 V. We confirmed that the BERs in the write and retention modes have much margins than that in the read disturb. So, the read operation is critical. The curves of the 7T with ECC and 7T with TMR can be calculated below:

$$\mathrm{BER}_{\mathrm{ECC}} = \mathrm{BER}_{7\mathrm{T}} \times \left[1 - \left(1 - \mathrm{BER}_{7\mathrm{T}}\right)^{37}\right]$$

$$\mathrm{BER}_{\mathrm{TMR}} = 3 \times \left(\mathrm{BER}_{7\mathrm{T}}\right)^{2} - 2 \times \left(\mathrm{BER}_{7\mathrm{T}}\right)^{3}$$

The minimum operating voltages are 0.66 V, 0.60 V, 0.58 V, and 0.52 V in the 7T normal, 7T with ECC, 7T with TMR, and 14T dependable modes, respectively. The 14T dependable mode reduces the minimum operating voltage by 0.14 V, compared to the 7T normal mode.

Figure 5.9 illustrates overviews of 1-bit correct ECC and TMR configurations when a word width is 32 bits. The ECC includes a syndrome generator, decoder, and error correction, which needs 158% speed penalty and 18% area overhead [44]. Because the TMR simply decides its outputs by majority voting, the speed penalty is less than that in ECC. However, the area overhead is 200% due to the triple redundancy. Note that the proposed 7T/14T SRAM can also adopt these classic methods. The combination with the proposed 14T dependable mode will realize higher reliability.

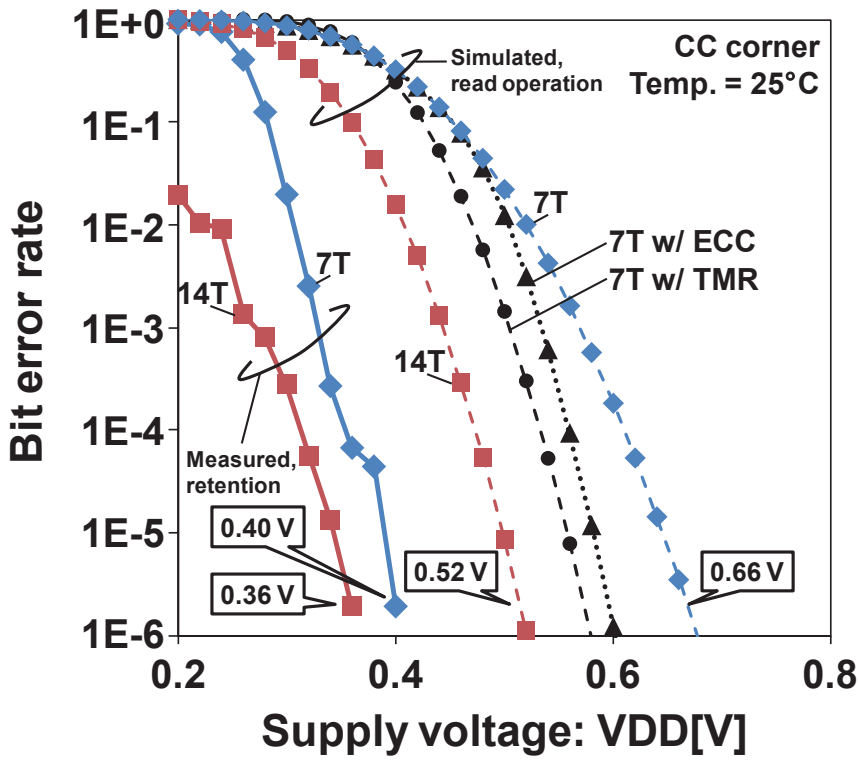


Fig. 5.8 BER curves: The 14T dependable mode has the smallest BER.

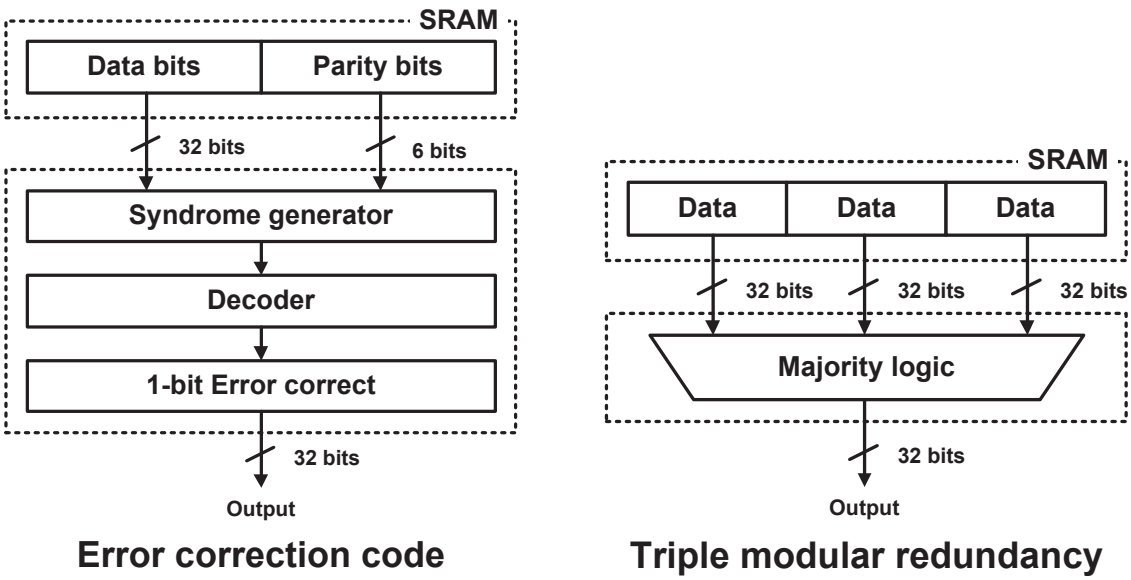


Fig. 5.9 Error correction code (ECC) and triple modular redundancy (TMR).

5.1.5 Soft-Error Rate Measurement Results

Figures 5.10 and 5.11 show diagrams of the alpha and neutron accelerated tests. For an alpha particle source, Am-241 foil was used; its flux was 9 × 109 $cm^{-2}h^{-1}$. The foil was placed above the package [45]. A neutron irradiation experiment for SER verification was conducted at the Research Center for Nuclear Physics (RCNP), Osaka University. A neutron white beam generated by a 400-MeV proton beam irradiates a measurement board for six hours, on which three sample chips were placed (Figure 5.12). The neutron flux was normalized to 3.6×10^{-3} $N/cm^2/s$ at the ground level in New York City.

Figures 5.13 and 5.14 illustrate the alpha and neutron SERs, respectively. In these experiments, any MCU did not occur. The supply voltage was fixed to 1.5 V according to the specification of the measurement board. The alpha-induced SER is improved by 80% although the 14T cell has two sensitive nodes per cell. This is because Q_{crit} is increased in the 14T dependable mode. The average neutron SERs in the three samples are 131 FIT/Mb and 86 FIT/Mb in the 7T normal and 14T dependable modes, respectively (34.4% reduction). The standard deviation is decreased from 9.06 FIT/Mb to 5.87 FIT/Mb. The 14T dependable mode has a double area but achieves a less SER than to the 7T normal mode.

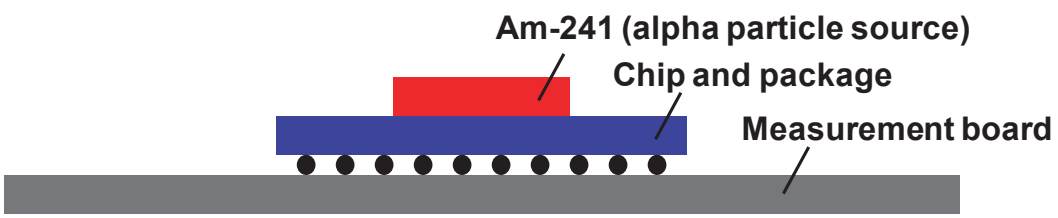


Fig. 5.10 Experiment diagram of alpha accelerated test.

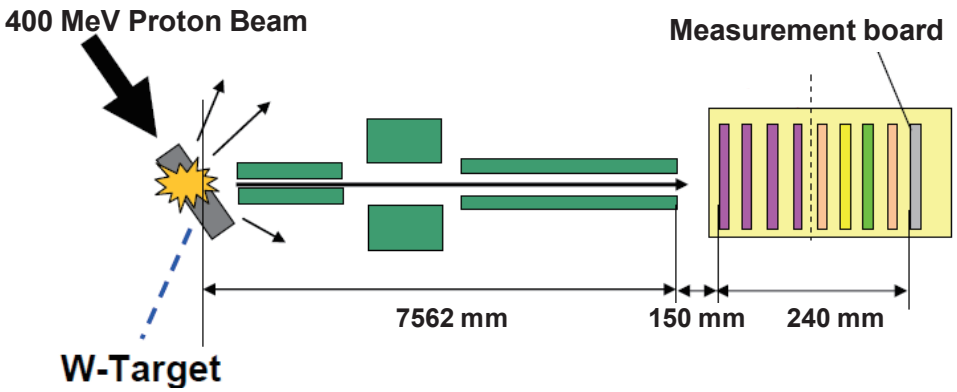


Fig. 5.11 Experiment diagram of neutron accelerated test.

Fig. 5.12 Photograph of neutron accelerated test.

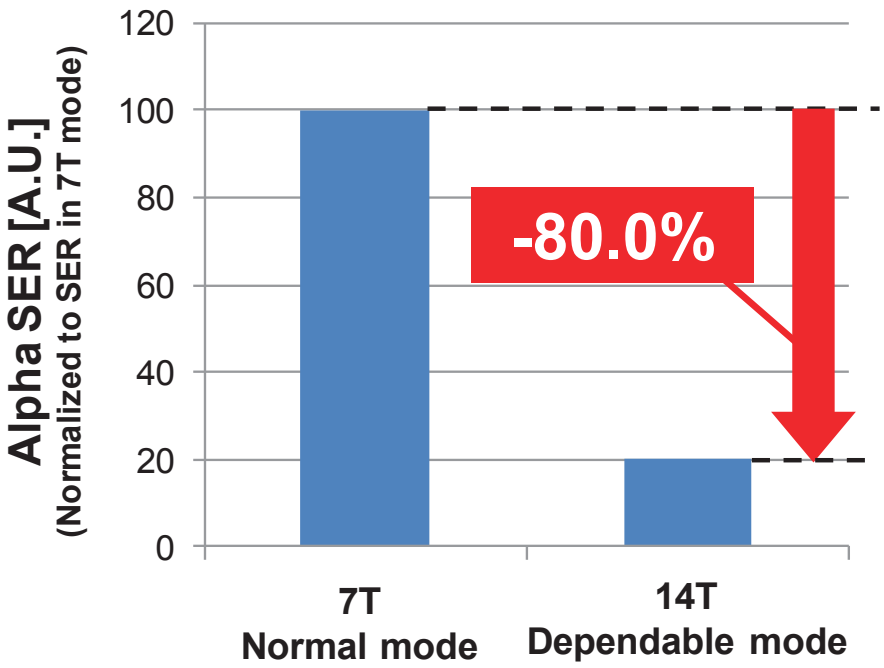


Fig. 5.13 Measured alpha-induced SERs in the 7T/14T SRAM.

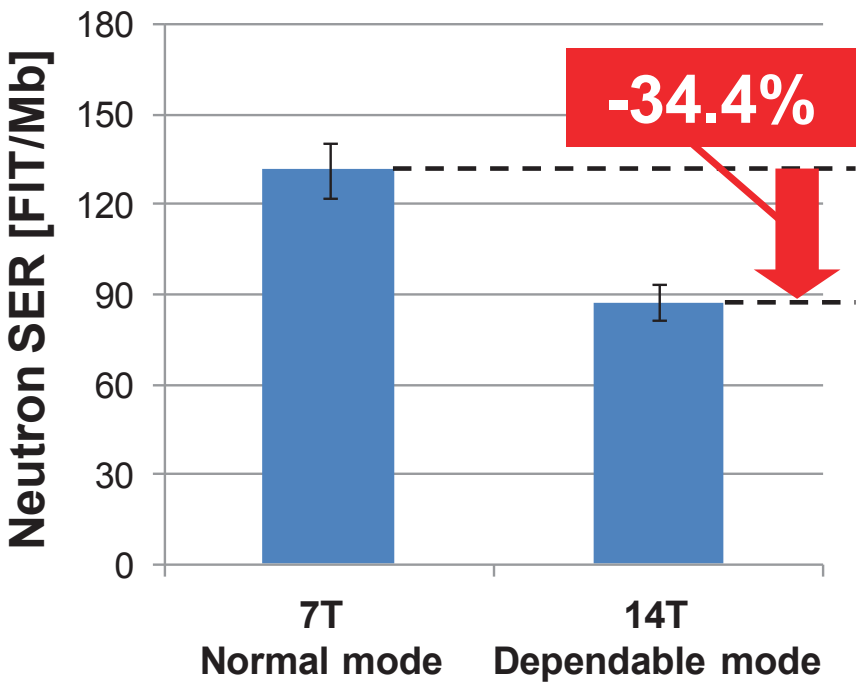


Fig. 5.14 Measured neutron-induced SERs in the 7T/14T SRAM.

5.2 Multiple-Bit-Upset Tolerant 8T SRAM Layout in Divided Wordline Structure

5.2.1 Multiple-Bit-Upset Tolerant 8T SRAM Layout

The 8T SRAM cell presented in Fig. 5.15 was proposed to eliminate read failures caused by the dedicated read port (comprising NRA and NRD). Figures 5.16(a) and 5.16(b) illustrate a general bit-interleaving SRAM structure and a divided wordline structure [21]. In the write operation in the general structure, all access gates (NA0 and NA1 in Fig. 5.15) in one end's cell to the other are activated. Then selected BLs are discharged or charged by write drivers. Consequently, the other BLs, which are unselected, incur the half-select problem and consume large amounts of active power. The general structure has drawbacks related to low-power and low-voltage operation.

The divided wordline structure separates one word from others, and a large multiplexer (MUX) outputs a selected word. The BLs in the selected columns are only discharged, which can avoid the half-select problem and achieve low power. However, a conventional 8T SRAM with a divided wordline structure still holds the MBU problem in a word. Figure 5.16(c) presents the conventional 8T cell layout and alignment pattern. Because the conventional bilaterally symmetric allocation produces two adjacent latches (Latch-0 and Latch-1), two-bit upset in the horizontal direction can easily occur by a heavy-ion strike. In addition, the two adjoining nodes (n00 and n10) are n-diffusions, whose critical linear energy transfer (LET) is a quarter or less than that of p-diffusion [40]; it is difficult to avoid the MBU in a word in the conventional 8T cell.

As described in this paper, we propose a novel MBU-tolerant 8T cell layout and its alignment pattern. As presented in Fig. 5.17, a pMOS (PL0), nMOSes (ND0, NA0, ND1, NA1), pMOS (PL1) and nMOSes (NRA and NRD) form p-n-p-n diffusions. The internal latches are separated and not adjoining. The sensitive nMOSes (ND0 and ND1) are adjacent in a single cell, by which enhancing a SER tolerance can be expected using a common-mode effect [46]. Therefore, the proposed 8T cell layout achieves MBU tolerance, even in the divided wordline structure.

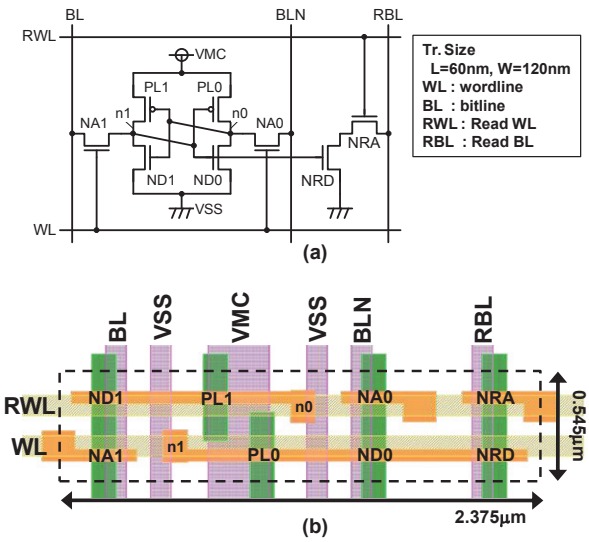


Fig. 5.15 (a) Schematic and (b) layout of conventional 8T cell in 65-nm CMOS process (logic rule basis).

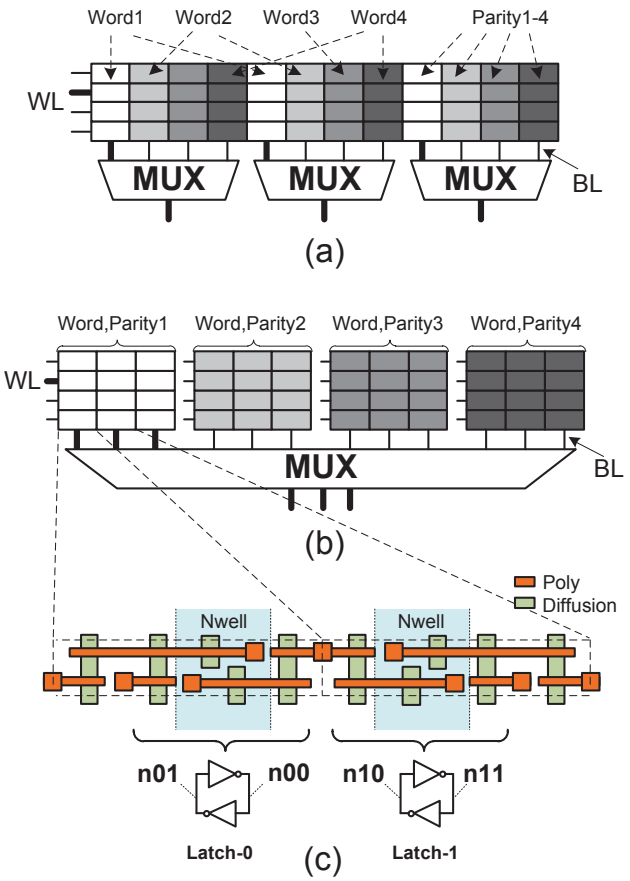


Fig. 5.16 (a) General structure, (b) divided wordline structure, and (c) conventional 8T SRAM cell layout pattern. ECC requires extra parity bits.

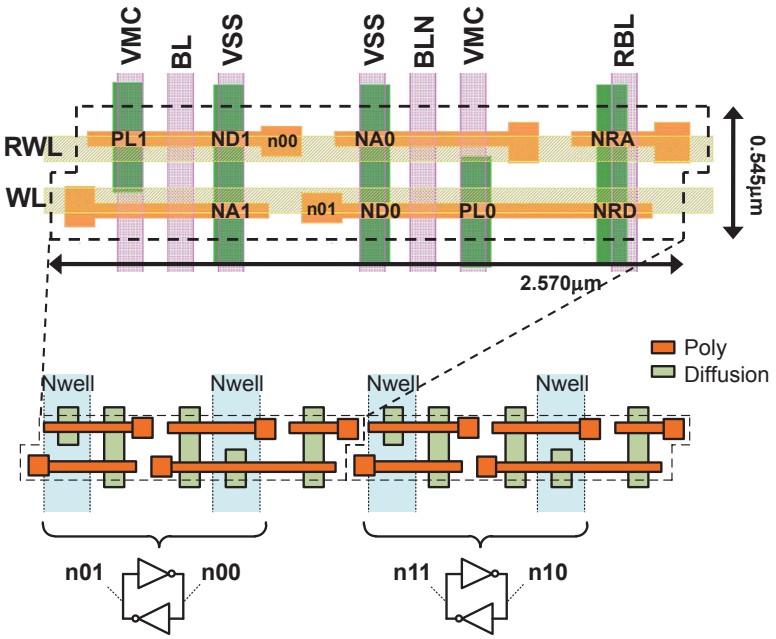


Fig. 5.17 Proposed 8T cell layout and alignment pattern.

5.2.2 Soft-Error Simulation Results

iRoC TFIT is a tool for simulating soft errors caused by heavy ions and neutrons on semiconductor devices [47]. Figure 5.18 presents the TFIT simulation flow diagram. In reality, TFIT has a database of disturb currents and soft-error behaviors extracted from the Synopsys TCAD simulator, which is fitted to measurement data. In the TFIT simulation flow, we used a 65-nm generic CMOS database and a 65-nm predictive technology model (PTM) model for SPICE simulations [48].

Figures 5.19 and 5.20 present SEU cross sections of nMOSes (ND1 = ND2 = ND and NA1 = NA2 = NA) and pMOSes (PL1 = PL2 = PL) in a latch, respectively. The cross section is defined by an area in which a heavy ion strikes and a cell is flipped. The LET of a heavy ion was varied from 10 to 90 fC / μm. The cross section area was set from the center of the drain diffusion. We observed that the cross sections at 0.9 V are 72–79% larger than at 1.3 V in the nMOSes. In the pMOSes, their cross sections at 0.9 V are 41–49% larger than at 1.3 V. For examples, at an LET of 90 fC / μm, the factors are 72% and 41% in the nMOSes and pMOSes, respectively. As a result, the SEU cross section ratio of nMOS to pMOS is increased in the lower-voltage region; Figure 5.21

presents that it is 3.5 at 1.3 V but goes up to 4.5 at 0.9 V. Because the proposed cell layout has nMOSes in the middle and the sensitive n-diffusions are separated in two adjoining cells, it can decrease the horizontal MBUs.

We also investigated neutron-induced MBU SER considering both horizontal and vertical directions, and compared the conventional and proposed 8T layout patterns. The TFIT has neutron-induced SER database fitted to sea level in New York. The SRAM data pattern was set to random and the memory capacity was assumed as 1 M bits. Figure 5.22 illustrates the MBU FIT and the error pattern examples in the conventional 8T SRAM at 0.9 V. The MBUs in the vertical direction can be corrected by ECC, but the two-bit or more upsets in the horizontal direction are not, which might cause important problems such as system failure. In the conventional 8T SRAM, the rates of the MBUs in the same words are 22.84% (2-bit MBU), 7.57% (3-bit MBU), 2.27% (4-bit MBU), and 0.56% (5-bit MBU) at 0.9 V; the total rate comes to 33.24% (= 22.84% + 7.57% + 2.27% + 0.56%).

Figure 5.23 shows that, in the divided wordline structure with the conventional 8T cell, the MBU SER reduction rate by ECC is 66.76% (= 100.00% – 33.24%) at 0.9 V as mentioned above. On the other hand, the MBU SER is decreased by 96.27% in the proposed 8T cell because the internal latches are separated by the n-well and p-substrate; the MBU in the same word is improved by 90.70% using the proposed layout.

In the proposed 8T SRAM, the total rate of the MBU in the same word is 3.73%, which is broken down into 0.00% (2-bit MBU), 2.72% (3-bit MBU), 0.81% (4-bit MBU), and 0.20% (5-bit MBU). The MBU SER is calculated as 3.46 FIT in ECC (FIT: failure in time). TABLE 5.1 presents neutron simulation results at 0.9–1.3 V; The MBU SERs are reduced by 66.76–69.02% with ECC in the conventional 8T cell while those in the proposed 8T cell correspond to 96.24–96.81%. This demonstrates that the proposed 8T cell suppresses the MBU SER in the same word effectively.

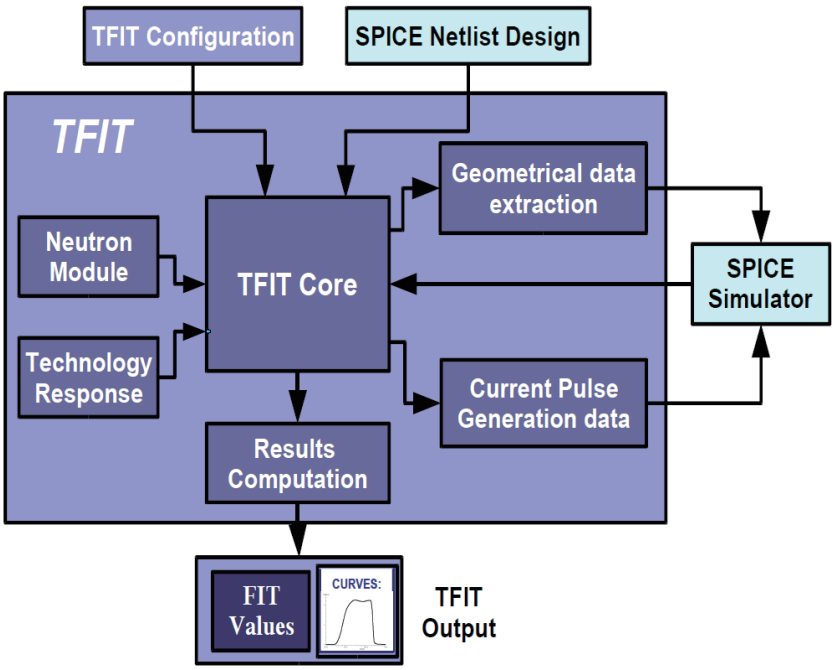


Fig. 5.18 TFIT simulation flow diagram [47].

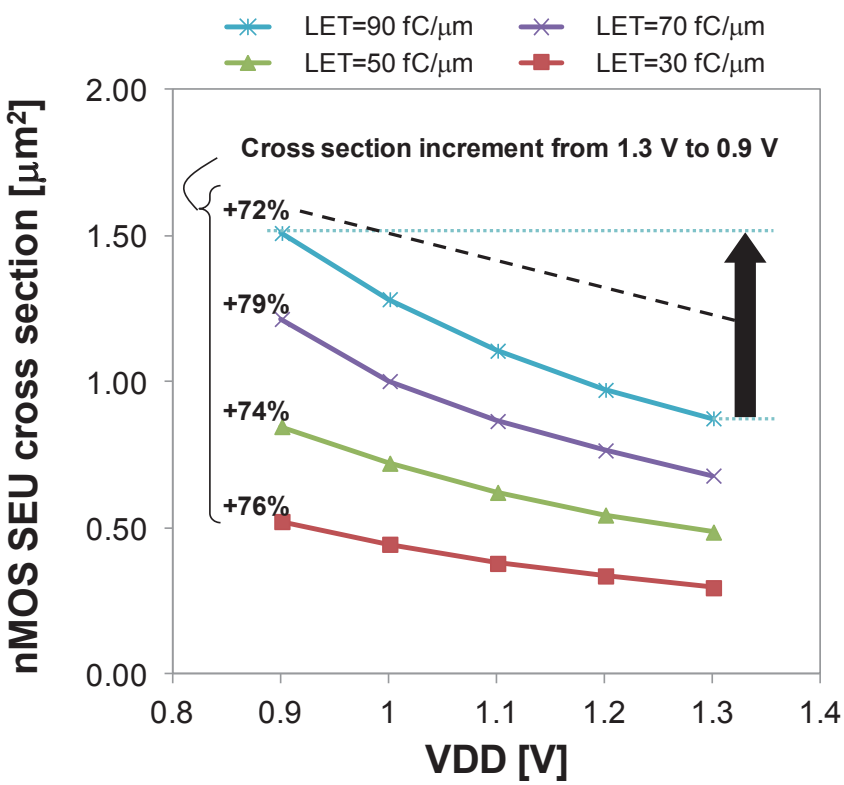


Fig. 5.19 SEU cross section in nMOSes (shared drain diffusion of ND and NA).

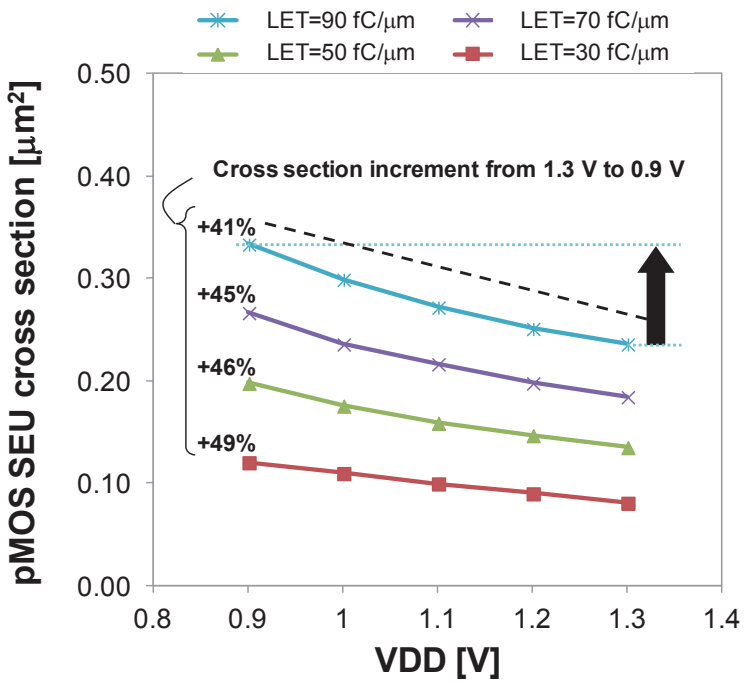


Fig. 5.20 SEU cross section in pMOSes (drain diffusion of PL).

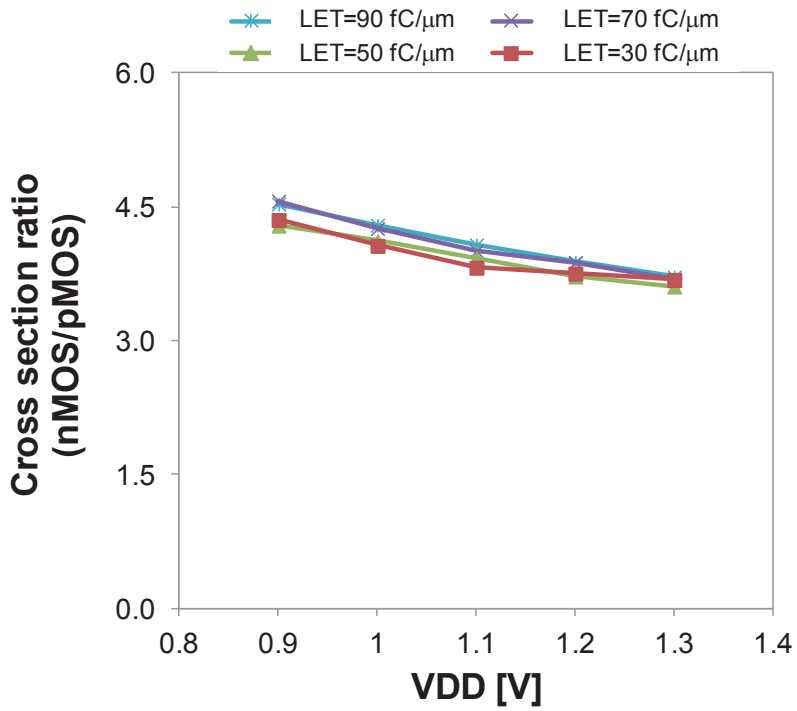


Fig. 5.21 Cross section ratio of nMOS to pMOS.

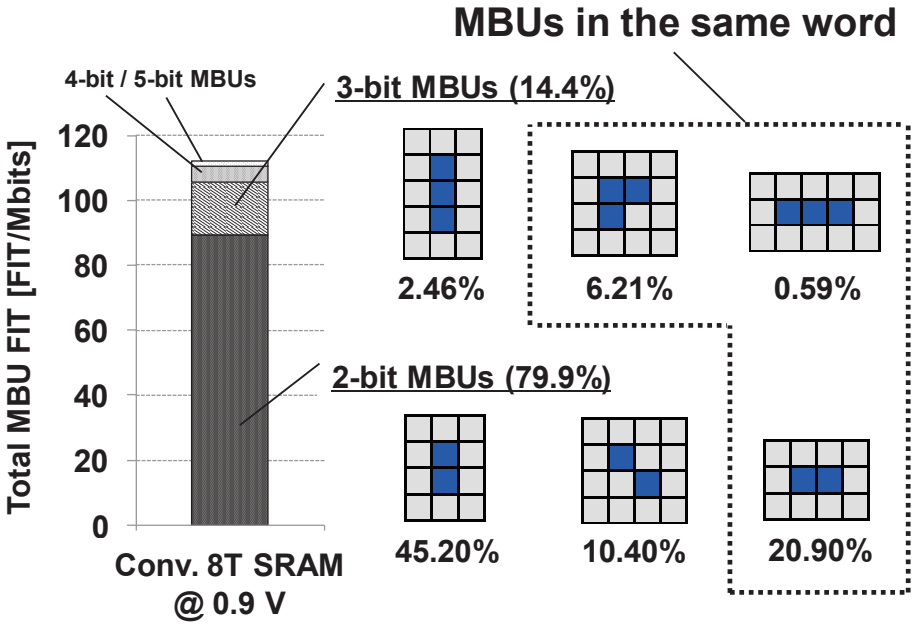


Fig. 5.22 MBU pattern examples in conventional 8T SRAM at 0.9 V. Note that they are examples; there are other patterns to be considered.

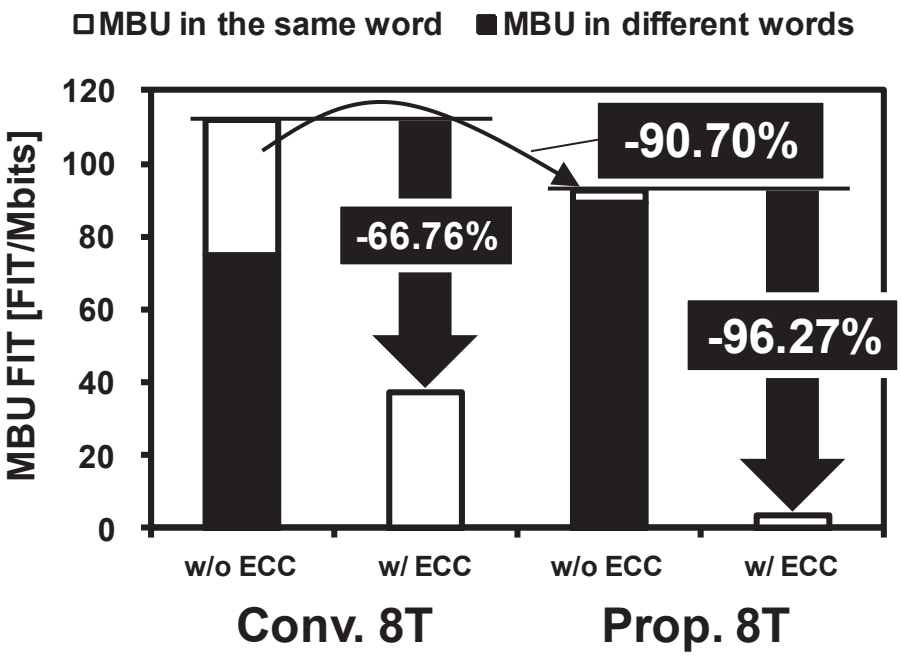


Fig. 5.23 Neutron-induced MBU improvement at 0.9 V in divided wordline structure: conventional and proposed 8T SRAMs.

Table 5.1 MBU Reduction Rate.

Type	VDD [V]	MBU SER w/o ECC [FIT]	MBU SER w/ ECC [FIT]	MBU SER reduction rate
Conv. 8T	0.9	111.92	37.20	-66.76%
	1.0	85.87	27.85	-67.56%
	1.1	64.68	20.77	-67.89%
	1.2	43.79	13.60	-68.95%
	1.3	37.12	11.50	-69.02%
Prop. 8T	0.9	92.78	3.46	-96.27%
	1.0	68.49	2.57	-96.24%
	1.1	50.04	1.82	-96.36%
	1.2	32.68	1.06	-96.74%
	1.3	26.79	0.85	-96.81%

5.2.3 3-D TCAD Simulation

We investigated an SEU tolerance in the proposed 8T SRAM layout using Synopsys 3-D TCAD simulation. The proposed 8T cell has two internal nodes (N1 and N0) of nMOSes (ND and NA) in the middle. The distance between the nodes is 0.46 μm. When a heavy ion strikes an area around them, these nodes are pulled down; in this case, the SEU tolerance is expected to be improved because of the common-mode effect. However, the conventional 8T cell is separated nMOSes by n-well and has no common-mode effect. In this simulation, two nMOSes (ND0 and ND1) in the proposed 8T cell and one nMOS (ND1) in the conventional 8T cell were made with 65-nm 3-D device models. The other transistors were based on the PTM 65-nm SPICE model. The gate length and width of the nMOS were set respectively to 60 nm and 120 nm.

Figure 5.24 illustrates a cross section and an ion strike point of an nMOS: Figure 5.24(a) shows the case of the conventional 8T cell, and Fig. 5.24(b) shows the proposed 8T cell case. The heavy ion strikes at 0.23 μm, which is far away from the edge of the drain node.

Figures 5.25(a) and 5.25(b) show internal waveforms in the conventional and proposed 8T cells. The conventional 8T cell was flipped by the impact. In contrast, the proposed 8T cell is not flipped, which best explains the phenomenon of the common-mode effect. Figure 5.26 shows an LET threshold (LET_{th}) improvement at 0.9 V in the proposed 8T cell. In this 3D TCAD simulation, the common-mode effect enhances the LET_{th} from 1.360 MeV to 2.264 MeV (+66%). In reality, note that the improvement depends on the position and LET of the ion strike; however, the total effect in the proposed 8T cell is confirmed in the previous subsection.

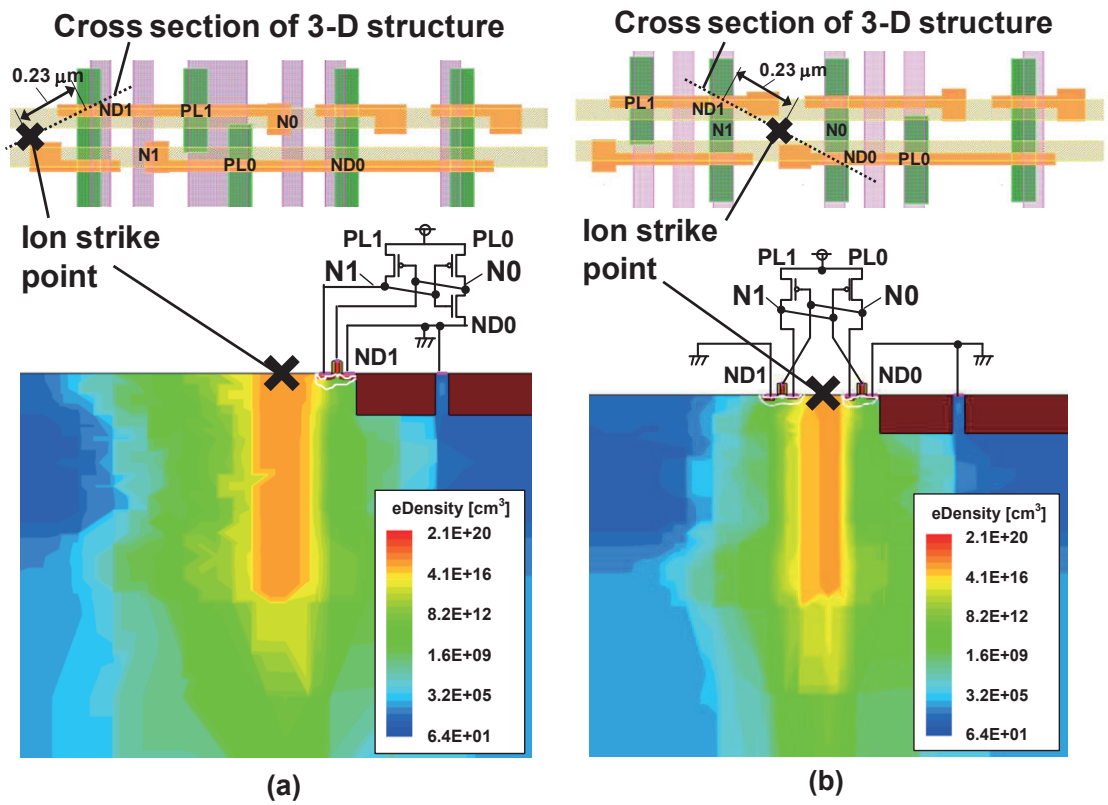


Fig. 5.24 Cross sections and ion strike points of nMOSes in (a) conventional 8T cell layout pattern (same as Fig. 5.15) and (b) proposed 8T cell layout pattern (same as Fig. 5.17). LET of heavy ion is 5.49 MeV.

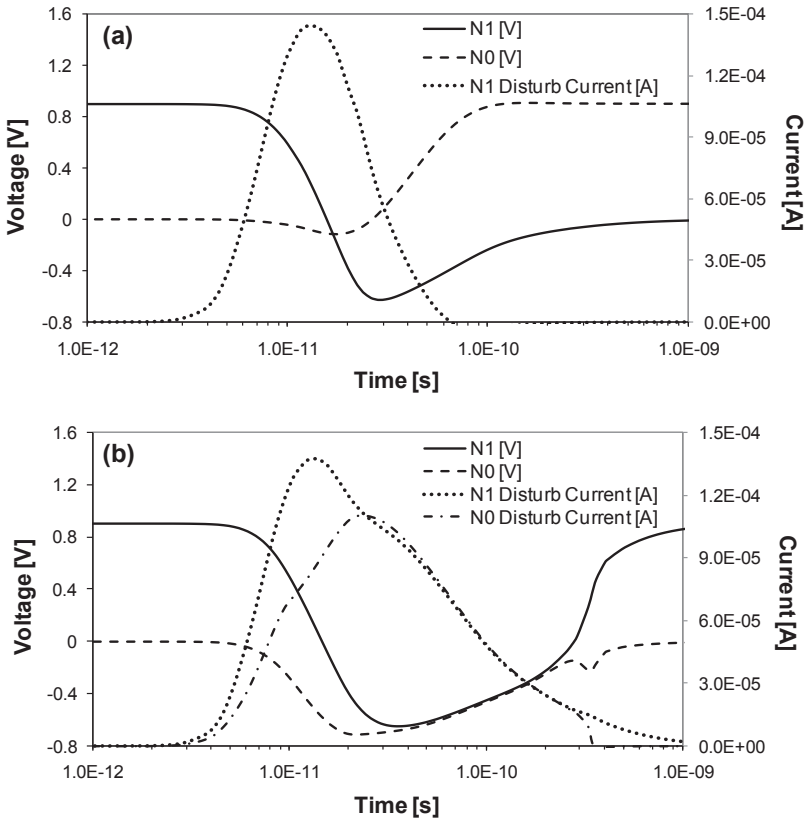


Fig. 5.25 Waveforms of internal nodes' (N1 and N0) voltages and their disturb currents in (a) conventional and (b) proposed 8T cells.

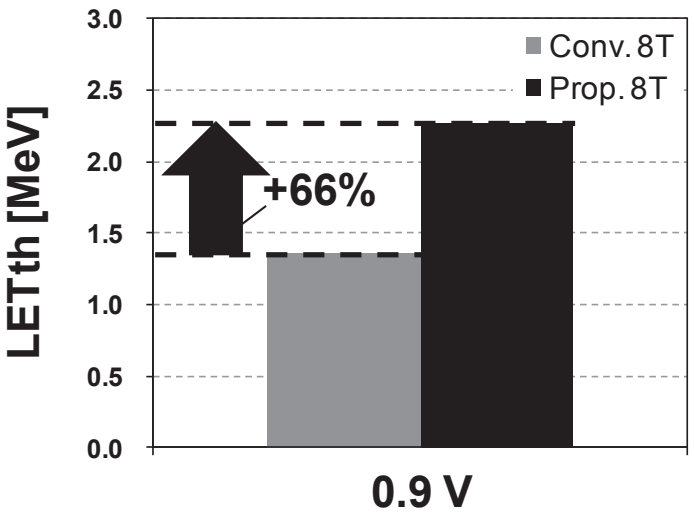


Fig. 5.26 LET_{th} improvement at supply voltage of 0.9 V.

5.2.4 Area and Power Comparison

The proposed 8T SRAM layout has an area overhead due to its p-n-p-n diffusion. In addition, the divided wordline structure requires an extra AND gate for each word. In this subsection, we mention the overheads in the proposed layout.

Table 5.2 shows a cell area comparison (the conventional 6T cell, the conventional 8T cell, and the proposed 8T cell). The three kinds of cells are all designed in a 65-nm CMOS logic rule, as illustrated in Figs. 5.15, 5.16, and 5.17. The cell area overhead in the conventional and the proposed 8T cell is 33% and 44% over the conventional 6T cell, respectively.

Figure 5.27 shows area overheads on an SRAM macro level when a bits / word (B in Table 5.2) is varied. The conventional 6T SRAM macro has the bit-interleaving structure and the conventional and proposed 8T SRAM macros have the divided wordline structure. The cell arrays consist of eight words / row and 256 cells / bitline. The SRAM macros are equipped with 1-bit correcting ECC. As the word width (B) is increased, the array area overheads are decreased. The proposed 8T SRAM is 48% larger than the conventional 6T SRAM when using 64 bits / word.

Table 5.2 SRAM array features.

	Conv. 6T SRAM	Conv. 8T SRAM	Prop. 8T SRAM
Cell area [um^2] (ratio to 6T)	0.9701 / cell (× 1.00)	1.294 / cell (× 1.33)	1.401 / cell (× 1.44)
Array style	Bit interleaving	Divided WL	Divided WL
Configuration	B bits/word × 8 words/row × 256 cells/bitlines		
ECC	1-bit correction		

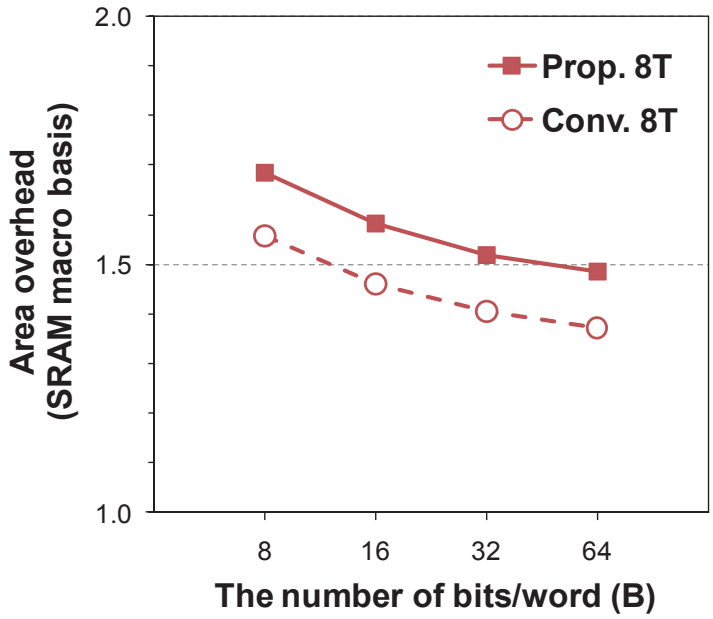


Fig. 5.27 Area overheads on an SRAM array level when the number of bits/word (B in Table 5.2) is varied.

The proposed 8T SRAM layout has the drawbacks in the area overhead; however, it improves a minimum operating voltage as well as the conventional 8T SRAM.

Figure 5.28 illustrates bit error rates (BERs) in the proposed and conventional 8T SRAMs and the 6T SRAM on the worst-case condition (FS corner and 125°C). A static noise margin (SNM) is used as a metric to evaluate the BERs. Note that the proposed 8T SRAM has the same BER curve as the conventional one because their transistor sizes are identical. Since the 8T SRAMs can eliminate the half-select problem, the minimum operating voltage is reduced from 0.88 V to 0.43 V (0.45-V improvement). The minimum operation voltage is defined at a BER of 10^{-6}.

Figure 5.29 shows operating power including peripheral circuits in the proposed and conventional 8T SRAMs and the 6T SRAM (when read / write = 50 / 50 and the power worst corner: FF corner and 125°C). The memory capacity is 1 M bits, and the clock cycle is set to 10 MHz. The proposed 8T cell has slightly longer wordlines and thus larger wordline metal capacitance than the conventional 8T cell; however, the power in the proposed SRAM consumes the same power as the conventional one because the power overhead in the proposed SRAM is negligible in the total power when the peripheral circuits are considered. Although the 8T SRAMs consume an extra power

due to its single-ended read port, the operating voltage can be decreased and thus the power is improved by 77.2%. Consequently, the proposed 8T SRAM achieves a low-voltage and low-power operation as well as the conventional 8T SRAM.

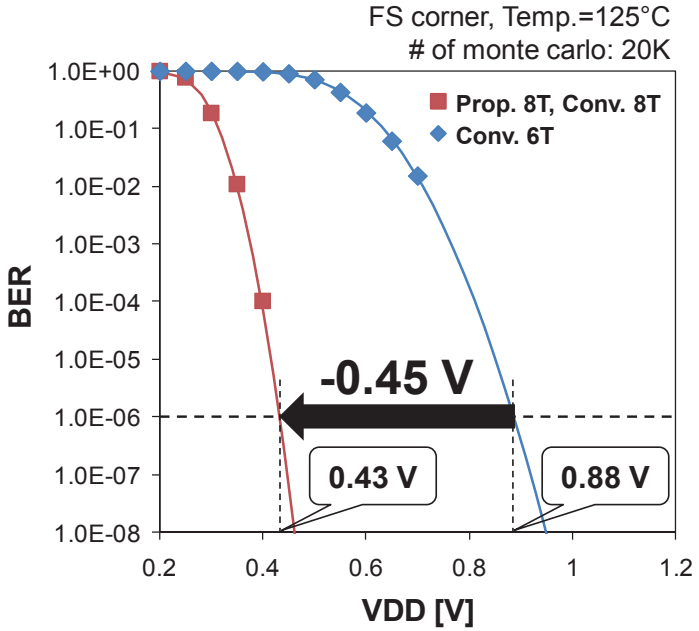


Fig. 5.28 Bit error rates (BERs) in the proposed and conventional 8T SRAMs and the conventional 6T SRAM. The minimum operation voltage is defined at a BER of 10^{-6}.

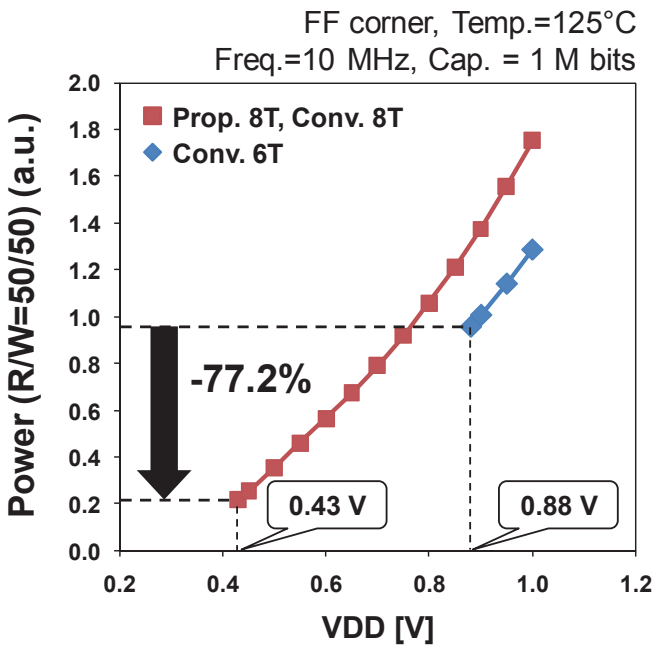


Fig. 5.29 Operating powers in the proposed and conventional 8T SRAMs and the conventional 6T SRAM.

5.3 Summary

As described in this chapter, we proposed two margin enhancement techniques for bit-error and soft-error resilient SRAM design:

1) We measured BERs and alpha-particle / neutron accelerated SERs using a 150-nm 576-Kb 7T/14T FD-SOI SRAM. We confirmed that the 14T dependable mode improves the minimum operating voltage to 0.52 V from 0.66 V in the 7T normal mode. The BER in the 14T dependable mode is superior to those in the TMR and ECC. The respective alpha- and neutron-induced SERs in the 14T dependable mode are 80.0% and 34.4% less than that in the 7T normal mode. We observed 10-70% increase of the 14T mode's Q_{crit} in a range of 0.3-1.5 V, by using Synopsys TCAD tool. The proposed 7T cell has the intrinsic area overhead of 9.5% over the 6T cell. Users can, however, boost the BER and SER reliability if paying more area overhead (14T cell = 119%). This feature demonstrates that the proposed 7T/14T SRAM can dynamically change its BER and SER; the users can take a tradeoff between the reliability and area (cost), which is useful and effective to various applications.
2) We proposed an MBU-tolerant 8T SRAM cell layout with the divided wordline structure. The proposed layout improves MBU in the divided wordline by 90.70%, and the MBU SER is decreased to 3.46 FIT at a supply voltage of 0.9 V. TCAD simulation of results indicated that the proposed 8T cell layout improves the LET_{th} by 66% due to the common-mode effect. The proposed 8T SRAM array has a 48% area overhead over the conventional 6T SRAM; however, the minimum operation voltage can be improved by 0.45 V and thus the operation power is decreased by 77.2%. Consequently, it can be said that the proposed 8T cell layout enhances soft-error reliability in the divided wordline structure and can achieve low-power and low-voltage operation.

Chapter 6 Neutron-Induced Soft-Error Simulator and Soft-Error Resilient Layout Design

In this chapter, a neutron-induced soft-error simulator and two soft-error tolerant designs for 6T SRAM:

1) Neutron-Induced Soft-Error Simulator Using PHITS
2) nMOS-Centered 6T SRAM Bitcell Layout
3) nMOS-pMOS Reversed 6T SRAM Cell Layout

6.1 Neutron-Induced Soft-Error Simulator Using PHITS

6.1.1 Simulation Flow

Figure 6.1 illustrates a flow chart of our simulation tool using the PHITS [10]. The simulation flow proceeds in the following sequence.

- The cosmic-ray neutron spectrum is predicted using an Excel-based Program for calculating Atmospheric Cosmic-ray Spectrum (EXPACS) [46, 47] as shown in Fig. 6.2. Neutron flux is normalized to ground level in New York City. The neutron energy is 1 MeV – 40 GeV as the input data.
- The device structure is constructed as presented in Fig. 6.3. The structure consists of a reaction and sensitive volumes in the memory cell array. The cell pitch, cell size, and sensitive volume size are based on 65-nm 6T SRAM cell layout design (logic rule basis) and a data pattern (ALL0). The sensitive volumes correspond to a high level (H) node of an NMOS transistor and a low level (L) node of a PMOS transistor. Actually, an NMOS node is known to have less critical charge than a PMOS node. The alignment of the sensitive volumes depends on the cell topology.
- The PHITS code has some nucleus reaction models: The intra-nuclear cascade (INC) model [51], the quantum molecular dynamics (QMD) model [52], and the generalized evaporation model (GEM) [53].
- Additionally, the PHITS includes an option called an event generator mode

(e-mode) [54] that describes low-energy neutron reaction below 20 MeV with evaluated nuclear data libraries. The models are chosen according to a tradeoff between the simulation time and the accuracy. In this work, the PHITS uses INC + GEM + e-mode with JENDL-4.0 [55].

- The PHITS simulates the nucleus reaction and particle transportation. During the simulation, dump files can be exported, which include the secondary ion particle states: atomic weight, nucleus reaction point (X, Y, Z), velocity vector (dX, dY, dZ), and energy per nucleon. If a particle crosses the surface of the sensitive volume, then the state of the particle at the cross point is also exported to the dump file.
- The secondary particle affects memory cells if crossing its sensitive volumes. The deposit energy is calculated with the dump files in respect to NMOS and PMOS nodes. In this work, the critical charge (Q_{crit}) to cause the memory cell upset can be set respectively to NMOS and PMOS nodes.
- The particles which cause at least one memory cell upset are extracted to a single-event-upset (SEU) particle list; we assume that an upset occurs if the energy deposited to the sensitive NMOS or PMOS node exceeds its critical charge.
- Some high-energy particles can upset several memory cells. In this simulation, an MCU particle list is extracted from the SEU particle list. We investigate horizontal and vertical MCU patterns. Consequently, the SEU and MCU SERs are calculated as a failure in time per 1-Mb SRAM (FIT / Mb).

In the following subsections, we introduce details of the simulation tool flow: device structure, dump files, SEU / MCU list extractions, and SEU / MCU SER calculations.

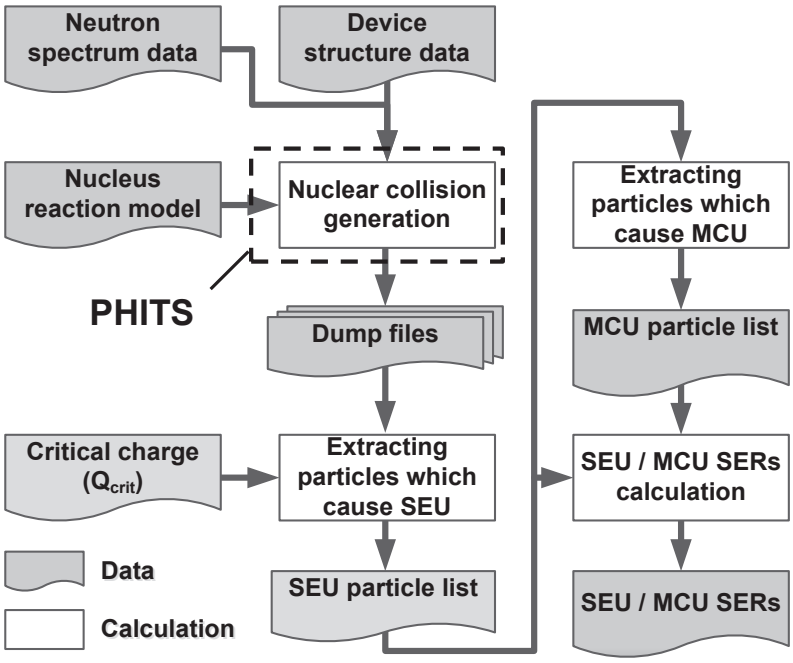


Fig. 6.1 Flow chart of the proposed SER simulation tool using PHITS [10].

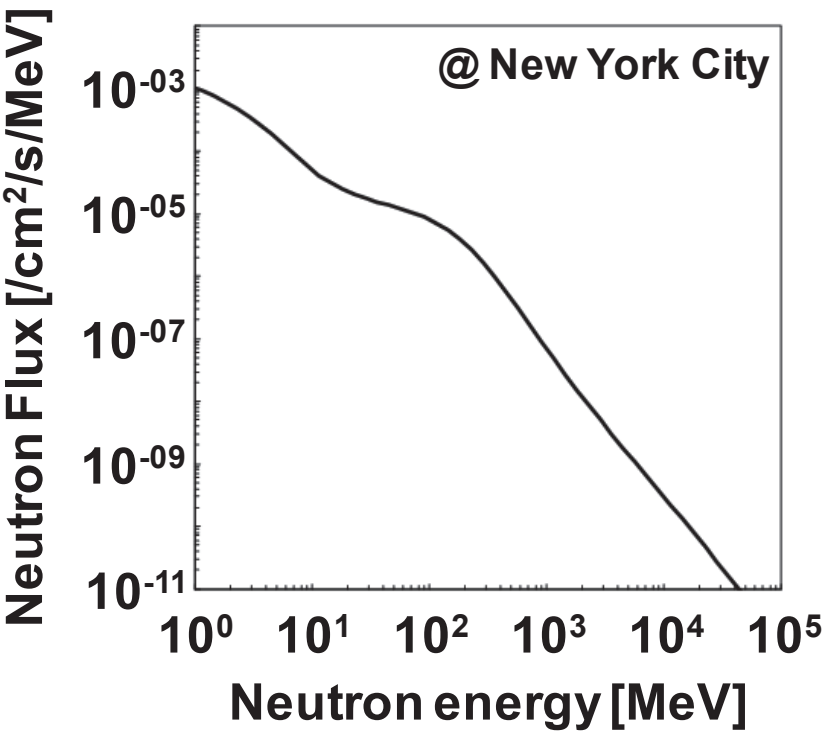


Fig. 6.2 Cosmic-ray neutron flux normalized to ground level in New York City calculated by EXPACS [46, 47].

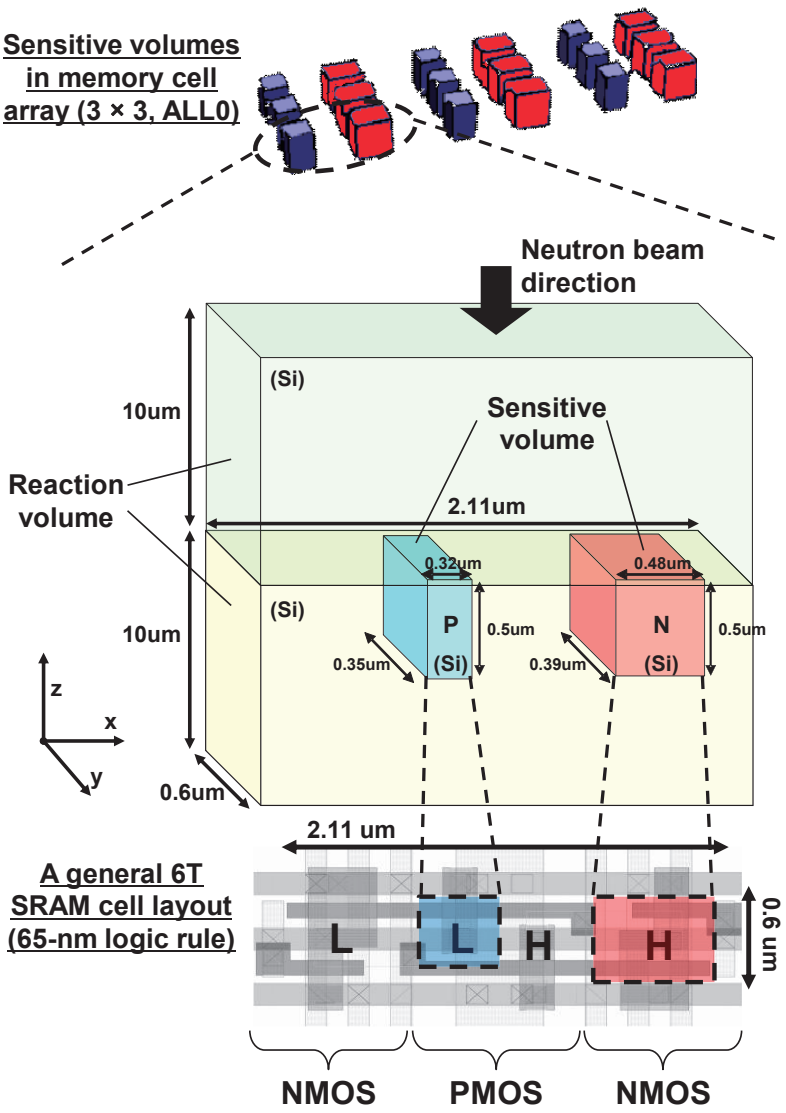


Fig. 6.3 Device structure based on a 65-nm general 6T SRAM cell layout (logic rule basis).

6.1.2 Soft-Error Rate Calculation

The PHITS can export secondary particle dump files presented in Fig. 6.4. The product dump files and the cross dump files respectively include particle data at nucleus reaction points and at crossing points from / to the sensitive area. In our simulation, the dump files are generated in respect to NMOS and PMOS sensitive volumes in an SRAM cell. The dump file includes nucleus reaction IDs (event numbers), atomic weight, geometry points (X, Y, Z), velocity vectors (dX, dY, dZ), and energy in the point (E). The deposit energy (E_{deposit}) corresponds to the particle's lost energy. The E_{deposit} in

Fig. 6.4(a) – 6.4(d) are calculated respectively. The deposit charge ($Q_{deposit}$) is calculated using the following equation.

$$Q_{deposit}[\mathrm{C}] = \frac{e}{3.6} \times E_{deposit}[\mathrm{eV}]$$

The SEU and MCU SERs are calculated with the particle lists. The SEU SER (SER_{SEU}) is calculated as follows:

$$SER_{SEU} = 3.6 \times A_{neutron} \times N_{SEU} / N_{neutron} \times Flux \times 10^{10} [\mathrm{FIT/Mb}]$$

Figures 6.5(a) and 6.5(b) show MCU error patterns: (a) $MCU_{BL=1}$ shows vertical fails in a column; and (b) $MCU_{BL>1}$ shows horizontal fails in several columns. In this work, the $MCU_{BL=1}$ SER and $MCU_{BL>1}$ SER are investigated using the proposed tool according to the data pattern and the layout topology. The MCU SER, SER_{MCU}, is calculated using the equation (2-3). In the equation, $A_{neutron}$ is the neutron irradiation area (μm^2), N_{MCU} is the number of MCUs, $N_{neutron}$ is the number of neutron irradiations and *Flux* is a frequency of the neutron particle ($1/cm^2/s$) calculated with Fig. 6.2.

$$SER_{MCU} = 3.6 \times A_{neutron} \times N_{MCU} / N_{neutron} \times Flux \times 10^{10} [\mathrm{FIT/Mb}]$$

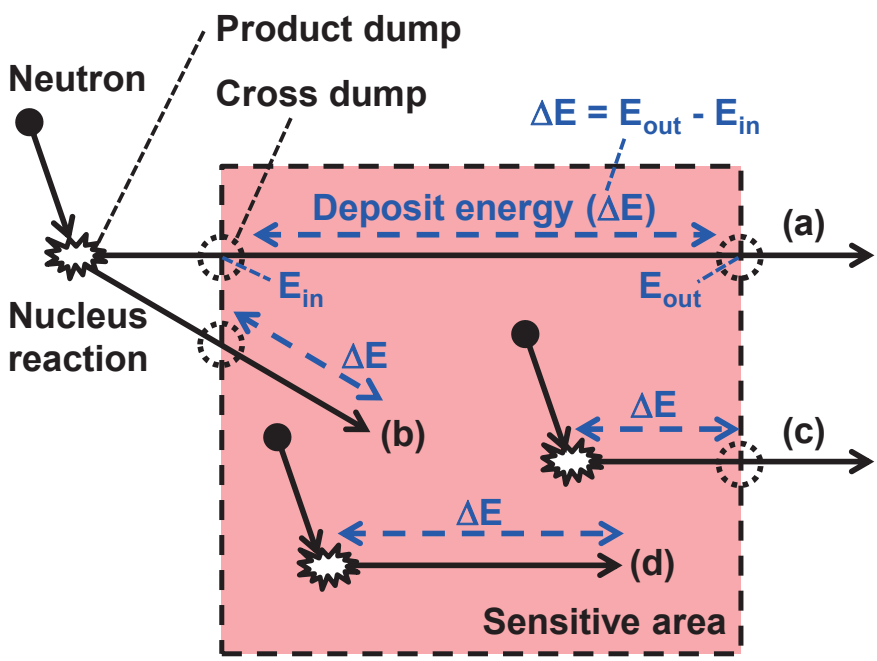


Fig. 6.4 Product-dump and cross-dump data related to secondary ions: (a) crossing the sensitive area, (b) entering the area, (c) leaving the area, and (d) remaining in the area.

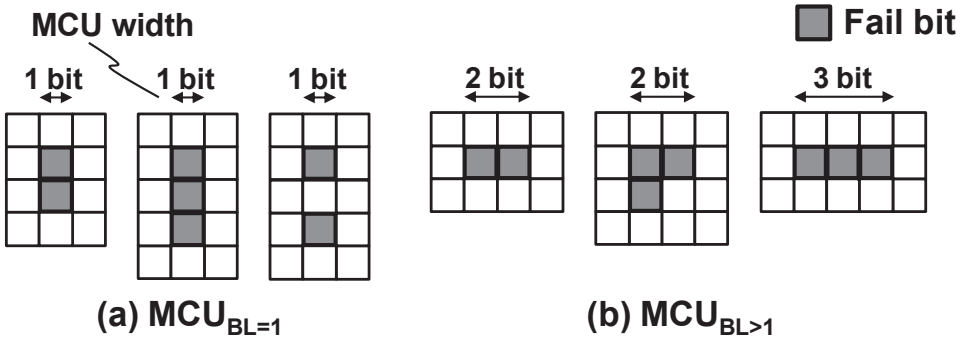


Fig. 6.5 MCU error patterns: (a) $MCU_{BL=1}$ shows vertical fails in a column and (b) $MCU_{BL>1}$ shows horizontal fails in several columns.

6.2 NMOS-Centered 6T SRAM Bitcell Layout

6.2.1 Conventional and Proposed 6T SRAM Cell Layouts

Respective Figs. 6.6(a) and 6.6(b) show a schematic and a layout of a general 6T SRAM cell with a 65-nm CMOS logic rule. In the design, the sizes of the transistors are relaxed to suppress threshold voltage variation so that the cell area is about twice as large as a commercial 65-nm 6T cell. The 6T cell consists of PMOS load transistors (PL0, PL1), NMOS driver transistors (ND0, ND1) and access transistors (NA0, NA1). A wordline (WL) and two bitlines (BL, BLN) are horizontally and vertically connected among cells, respectively. In the layout of the general 6T cell, the PMOS transistors are centered in the memory cell; this structure is called an NMOS-PMOS-NMOS (NPN) layout in this paper.

Figure 6.7 shows sensitive nodes in the general 6T cell layout: a low-state ("L") PMOS diffusion and a high-state ("H") NMOS diffusion. We have observed that the NMOS has a four-times larger SEU cross section than a PMOS for a wide range of supply voltages (see Fig. 6.8). The simulation results come from an iRoC TFIT soft-error simulator using database of a generic 65-nm bulk CMOS process. Figure 6.9 shows an SRAM cell array using the general NPN 6T layout. In the conventional 6T SRAM, the sensitive NMOS nodes are in a same P-well in the horizontal direction; horizontal upsets can be easily incurred.

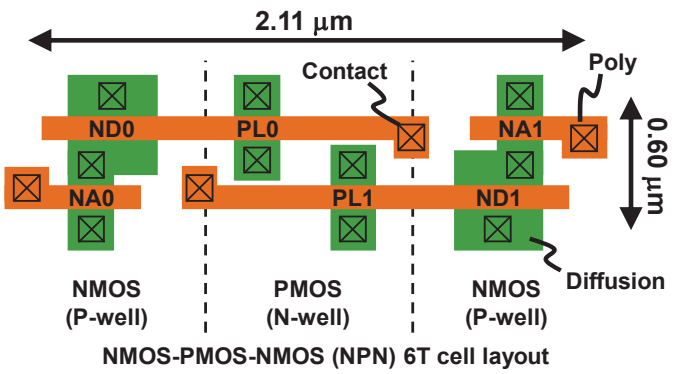


Fig. 6.6 (a) Schematic and (b) NMOS-PMOS-NMOS (NPN) layout of a general 6T SRAM cell.

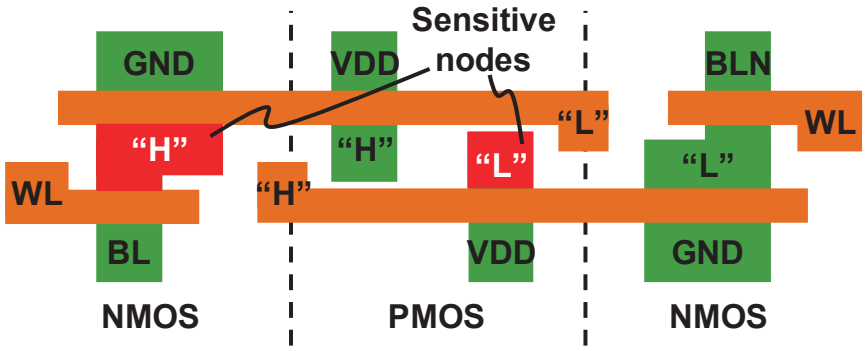


Fig. 6.7 Sensitive nodes in a general NPN 6T SRAM cell.

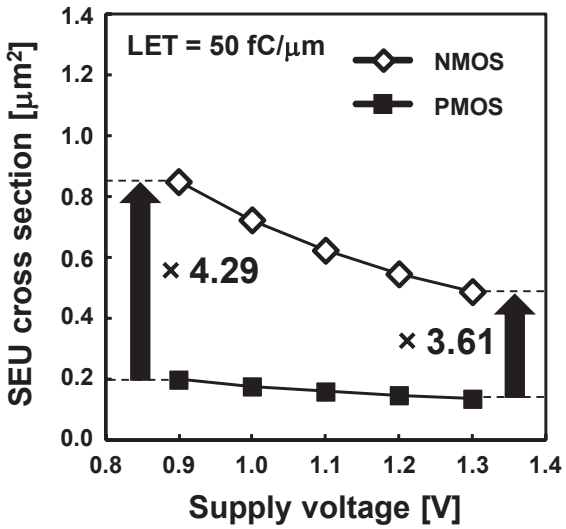


Fig. 6.8 SEU cross sections of NMOS and PMOS with a twin-well 65-nm process calculated using the iRoC TFIT simulator.

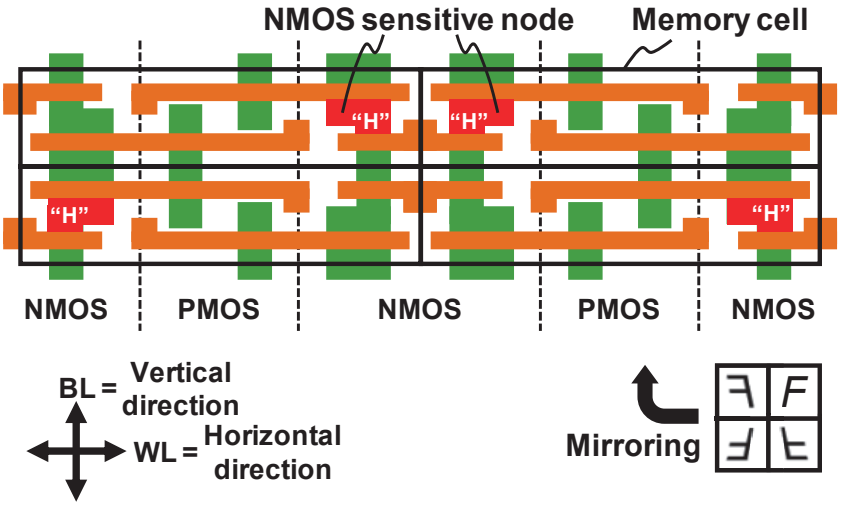


Fig. 6.9 SRAM cell array using the general NPN 6T cell layout.

The proposed 6T cell is designed as a PMOS-NMOS-PMOS (PNP) layout in Fig. 6.10. The NMOS-centered 6T layout has the same transistors as the general one. The WL and the BLs are respectively assigned in horizontal and vertical direction. The PNP 6T cell can lower a horizontal MCU rate because the NMOS-centered layout can separate the horizontally adjacent NMOS sensitive nodes with the N-well as shown in Fig. 6.11. The proposed layout has the same schematics and the cell area on the 65-nm logic rule basis, so that the proposed design can be implemented only by replacing its cell layout. Note that shared contacts, which are commonly used in an industrial SRAM rule, cannot be applied to the proposed 6T cell layout. This drawback incurs a certain area overhead in the SRAM rule basis design.

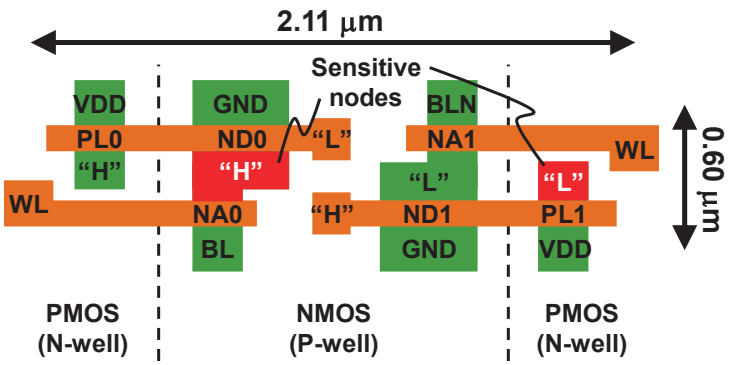


Fig. 6.10 Layout of a proposed PMOS-NMOS-PMOS (PNP) 6T cell.

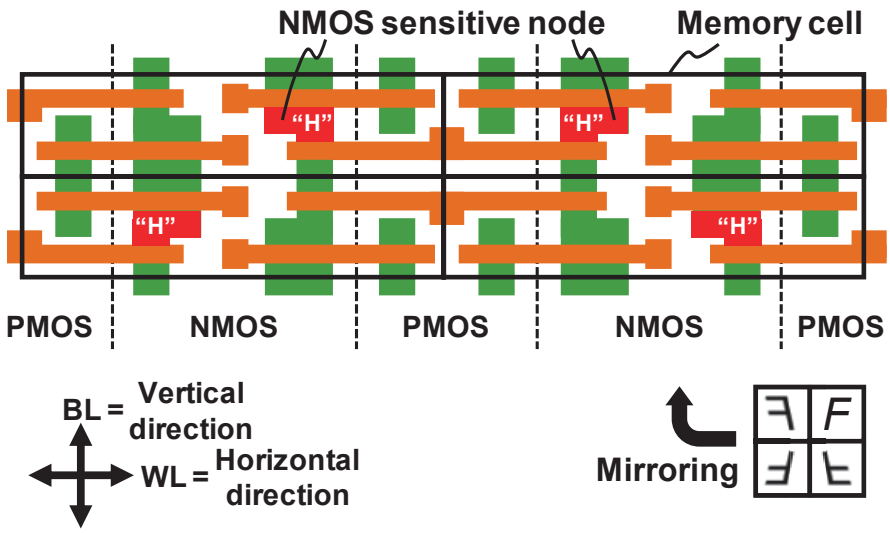


Fig. 6.11 SRAM cell arrays using the proposed PNP 6T cell layout.

6.2.2 SRAM Macro Design

We designed and fabricated an 1-Mb SRAM test chip consisting of 256-Kb macros of four types (NPN layout with twin well, PNP layout with twin well, NPN layout with triple well (Fig. 6.12), and PNP layout with triple well), as presented in Fig. 6.13(a). Additionally, Fig. 6.13(b) illustrates the block diagram of a 16-Kb block (128 columns × 128 rows: 16 bits / word × 1K words). The 16 bits in a same word are aligned in a bit-interleaving manner. The SRAM macros using the four-type 6T cells occupy same areas so that the SRAM macros share same peripheral circuits. In the two macros with the triple-well structures, the memory cells are merely fabricated in the triple well; the peripheral circuits are on the twin well. In the memory cells on the triple-well structure, the deep N-well narrows the depth of the P-well; thereby the parasitic bipolar effect increases the MCU SER. This paper also investigates the dependency on the well structuring.

Figure 6.14 presents a layout of the implemented SRAM cell arrays and well taps. The NPN and PNP 6T cells designed by the 65-nm logic rule have 2.11 × 0.60 μm^2 area (see Figs. 6.6(b) and Fig. 6.10; the gate length is relaxed to 80 nm to suppress variation). The well taps are inserted every 32 cells (= 19.2 μm) in the vertical direction; hence, a tap density is 1/32 of memory cells. Since the memory cell assigns the Metal-1 layer as internal connections, the vertical Metal-2 and horizontal Metal-3 layers are assigned as BLs and WLs.

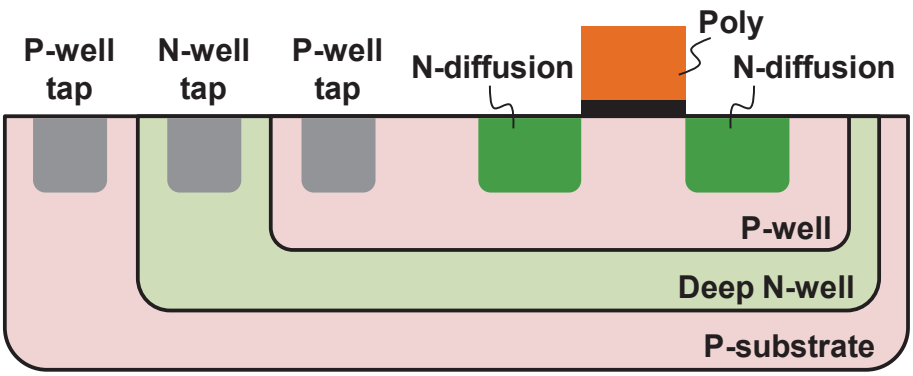


Fig. 6.12 Cross section of NMOS when using triple well.

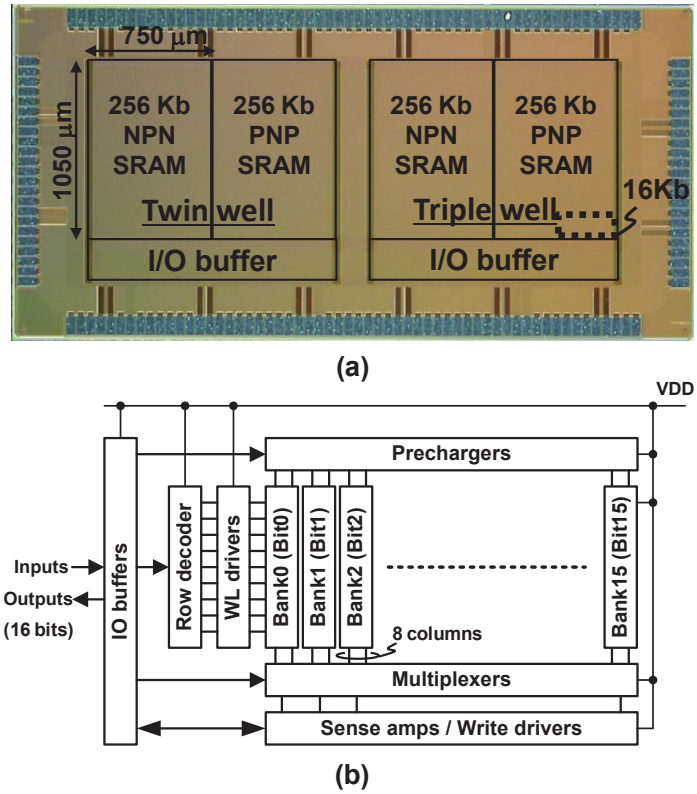


Fig. 6.13 (a) Micrograph of a 1-Mb SRAM test chip including NPN and PNP SRAMs with twin and triple wells. (b) Block diagram of a 16-Kb block.

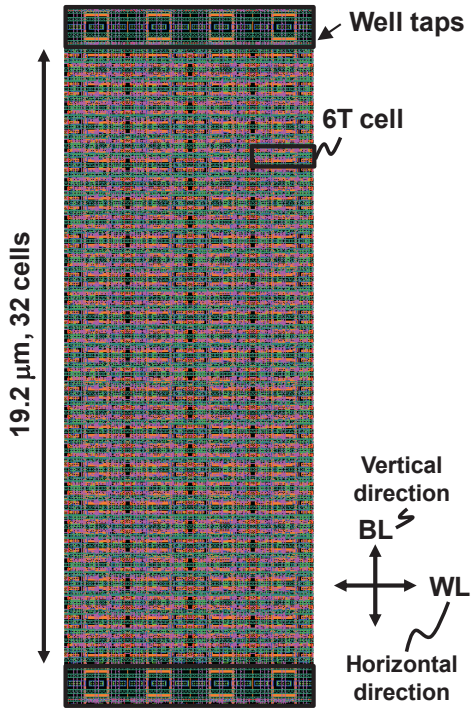


Fig. 6.14 Layout of memory cell array and well taps.

6.2.3 Experimental Results

The neutron irradiation experiment is conducted at The Research Center for Nuclear Physics (RCNP), Osaka University as presented in Fig. 5.12. Spallation neutron beam generated by the 400-MeV proton beam irradiates a board under test (BUT) 7892-mm far from a tungsten target, on which three sample chips are placed in a BUT, for 30 hrs. The neutron flux is normalized to 13 cph / cm^2 above 10 MeV at ground level in New York City [56], which incorporates scattering effect [57], attenuation effect [58], and board screening effect [59]. Figure 6.15 shows a timeline on the BUT. The FPGA automatically generates input data pattern to the SRAM macro before the irradiation and finally outputs addresses of the fail bits. The FPGA is placed apart from an irradiation area (10 cm diameter) so that the FPGA properly works even in this irradiation test.

Figures 6.16(a) and 6.16(b) illustrate measurement results of single-bit-upset (SBU) SERs when a checkerboard (CKB) pattern and all-zero (ALL0) pattern are used. The supply voltage is applied to the four macros from 0.6 V to 1.2 V to assess the dependence of the SERs on the supply voltage. Results show that the SBU SERs were ranging from 500 FIT / Mb to 1400 FIT / Mb depending on the supply voltage, but no apparent difference on the SBU SER is observed among the four types. The SBU SER of the CKB pattern is slightly larger than that of the ALL0 pattern. Figures 6.17(a) and 6.17(b) show NMOS sensitive nodes in the CKB and ALL0 patterns; they are aligned in the horizontal and vertical directions, respectively. The distance between the sensitive nodes in the CKB pattern is, however, longer than that in the ALL0 pattern (see Fig. 6.11); this feature possibly yields a more SBU SER in the CKB pattern even if a large-energy ion hits the sensitive nodes. On the other hand, MBUs tend to be incurred in the ALL0 patterns at the same ion energy.

In addition to the SBU SER, we measured MCU SER using four data patterns presented in Fig. 6.17: (a) CKB, (b) ALL0, (c) column stripe (CS), and (d) row stripe (RS), in which sensitive node patterns differ.

As presented in Fig. 6.5, an MCU SER in the vertical direction is called $MCU_{BL=1}$ in this paper, and an MCU SER in the horizontal direction is called $MCU_{BL>1}$. The $MCU_{BL>1}$ is more important for designers to adopt the interleaving and/or ECC strategy.

Figures 6.18(a)–6.18(d) illustrate measured MCU SER in the four data patterns at the

supply voltage of 1.2 V. When using the CKB, CS, and RS patterns, the $MCU_{BL>1}$ in the PNP 6T SRAM can be suppressed by 86–98% compared to the general NPN layout. The proposed PNP layout separates NMOSes from adjacent ones in the horizontal direction, which reduces the $MCU_{BL>1}$ SER. In the ALL0 pattern, the $MCU_{BL>1}$ even in the general NPN cells is low in nature because the sensitive nodes are not horizontally adjacent in a single bitline. As a result, only 67% improvement is observed in the MCU SER. The proposed PNP layout with the twin-well structure achieves $MCU_{BL>1}$ SERs of 5.78, 4.58, 9.48, and 4.70 FIT/Mb in the CKB, ALL0, CS and RS patterns and the PNP layout with the triple-well structure achieves $MCU_{BL>1}$ SERs of 5.78, 4.58, 18.96 and 3.13 FIT/Mb. Table 6.1 summarizes the data of the MCU SERs.

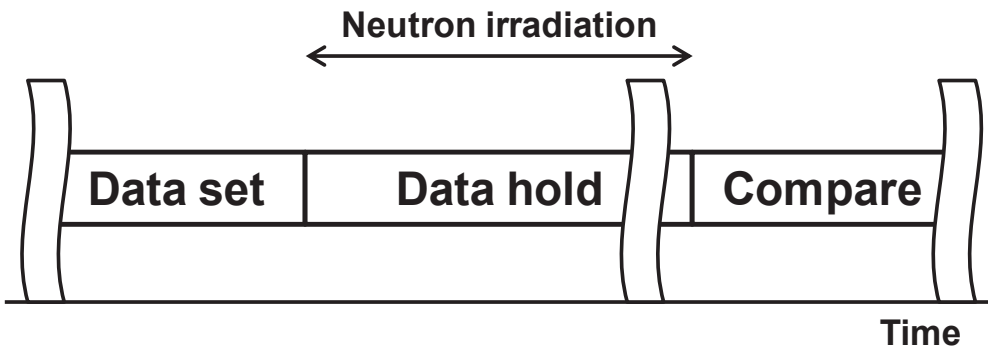


Fig. 6.15 Timeline in the neutron-accelerated test.

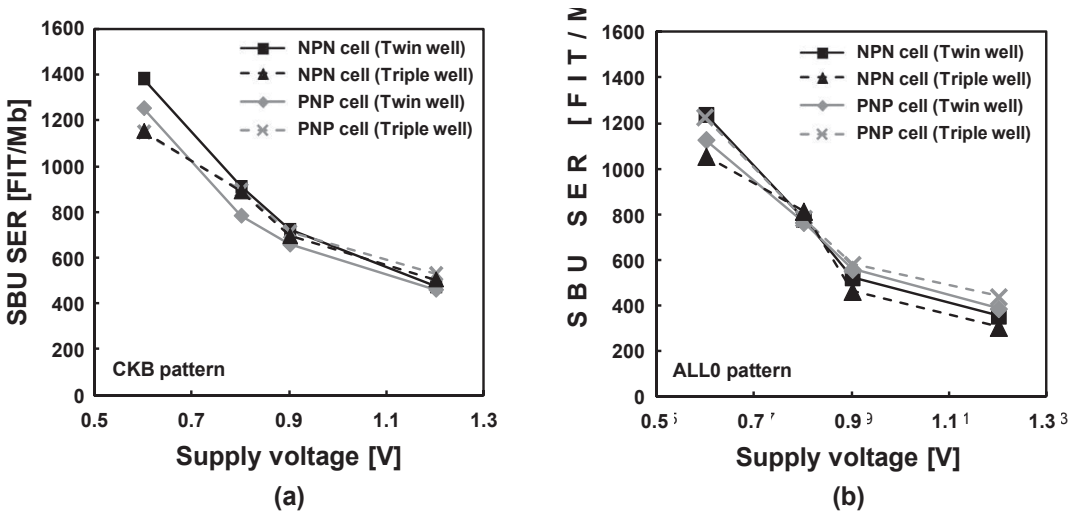


Fig. 6.16 Measured neutron-induced SBU SERs in the (a) CKB pattern and (b) ALL0 pattern at 0.6-1.2 V (four types).

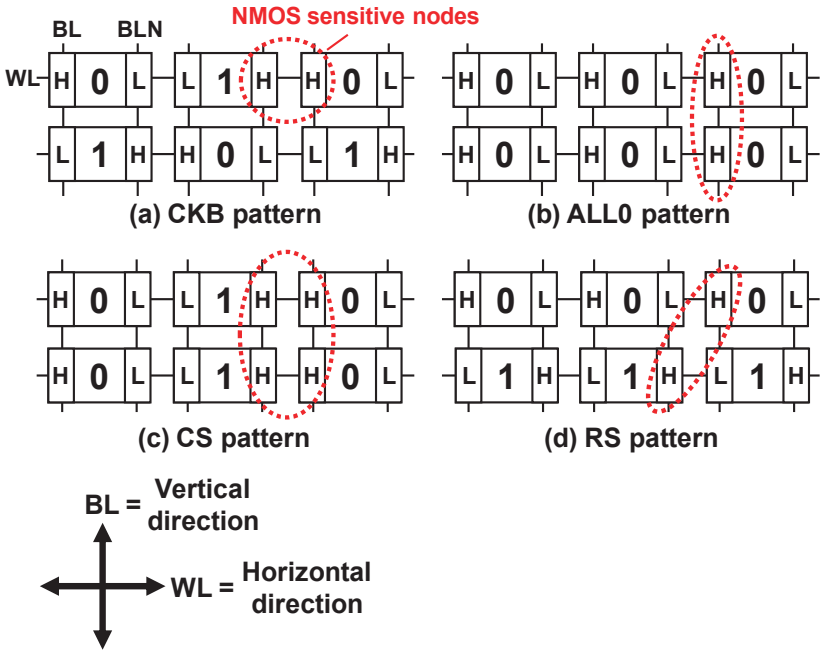


Fig. 6.17 Multiple-cell-upset patterns: (a) $MCU_{BL=1}$ and (b) $MCU_{BL>1}$ are defined respectively by vertical fail bits in a same column and by horizontal fail bits in two or more columns.

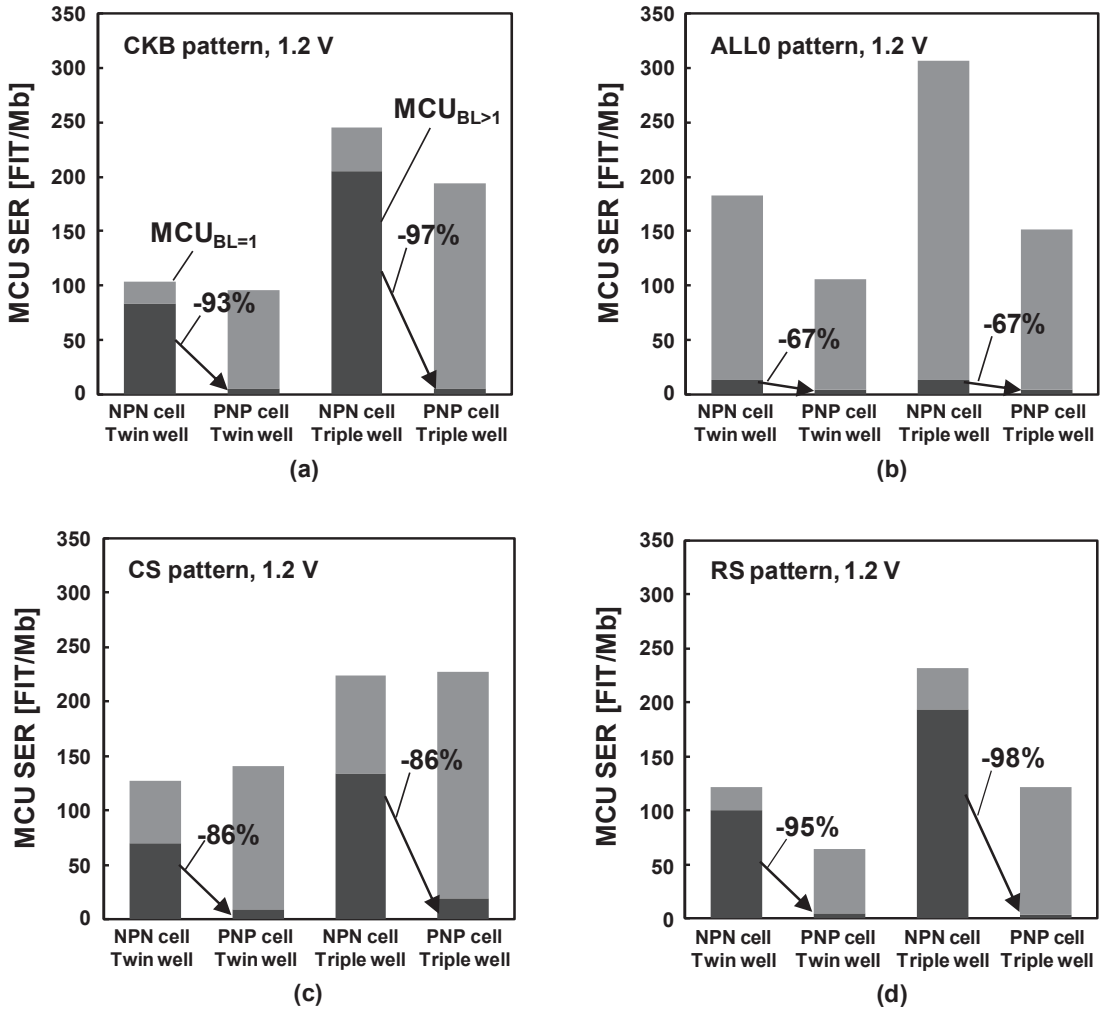


Fig. 6.18 Data patterns: (a) checker-board (CKB), (b) all zero (ALL0), (c) column stripe (CS), and (d) row stripe (RS).

Table 6.1 MCU Reduction Rate.

VDD [V]	Data pattern	Well type	Cell type	$MCU_{BL=1}$ SER [FIT/Mb]	$MCU_{BL>1}$ SER [FIT/Mb]	Total MCU SER [FIT/Mb]
1.2	CKB	Twin	NPN	20.23	83.83	104.06
			PNP	89.61	5.78	95.39
		Triple	NPN	40.47	205.23	245.70
			PNP	187.89	5.78	193.67
	ALL0	Twin	NPN	169.51	13.74	183.25
			PNP	100.79	4.58	105.37
		Triple	NPN	293.21	13.74	306.95
			PNP	146.60	4.58	151.19
	CS	Twin	NPN	56.89	69.93	126.82
			PNP	131.56	9.48	141.04
		Triple	NPN	90.08	133.93	224.01
			PNP	208.60	18.96	227.57
	RS	Twin	NPN	21.91	100.18	122.09
			PNP	59.48	4.70	64.18
		Triple	NPN	37.57	194.10	231.66
			PNP	118.96	3.13	122.09

6.3 NMOS-PMOS Reversed 6T SRAM Layout for Nanometer CMOS Technology

6.3.1 Process Scaling and Conventional 6T SRAM Cell

Process scaling continuously decreases an SRAM cell area by a factor of two in every technology generation, as presented in Fig. 6.19 [57, 58]. To scale CMOS transistors down to a 45-nm process or less, it is important to use compressive and tensile strain engineering for pMOS and nMOS, respectively, which increases the drain current [62]. Particularly, for a pMOS, embedded SiGe (eSiGe) in a source and drain boosts its saturation current (I_{satp}). The strain engineering is thereby more effective against I_{satp} than that in an nMOS (I_{satn}). Current enhancement using eSiGe strain for the pMOS increases more effective with the process scaling: +30% and +45% in a 45-nm and 22-nm processes [59, 60]. Figure 6.20 shows the trend of the saturation current ratio of an nMOS to a pMOS (= I_{satn} / I_{satp}) along with a process node [61, 62]. The ratio becomes unity because I_{satp} is comparable with Isatn at a 22-nm node. In addition, the pMOS has smaller threshold voltage variation (Vth variation) because of lesser dopant fluctuation [66]. Reportedly, the pMOS has less sensitivity to soft error effect than the nMOS. A standard deviation of the threshold voltage (σ_{Vth}) and a linear energy transfer threshold (LET_{th}) of the pMOS is 3/4 and 1/4 of those of the nMOS, respectively.

Figures 6.21(a) and 6.21(b) respectively show a schematic and a layout of the conventional six transistor (6T) SRAM cell. The conventional 6T cell consists of pMOS load transistors (PL0 and PL1), nMOS driver transistors (ND0 and ND1), and nMOS access transistors (NA0 and NA1). As described above, the conventional 6T cell suffers from the disadvantages of the large V_{th} variation and the soft-error vulnerability in the nMOS driver transistors. To cope with these nMOS problems and leverage the pMOS benefits, we propose the use of pMOS access and driver transistors instead: an n-p (nMOS-pMOS) reversed structure. A static noise margin, cell current, and soft-error tolerance are enhanced in the proposed n-p reversed 6T SRAM cell at the future 22-nm node or advanced ones.

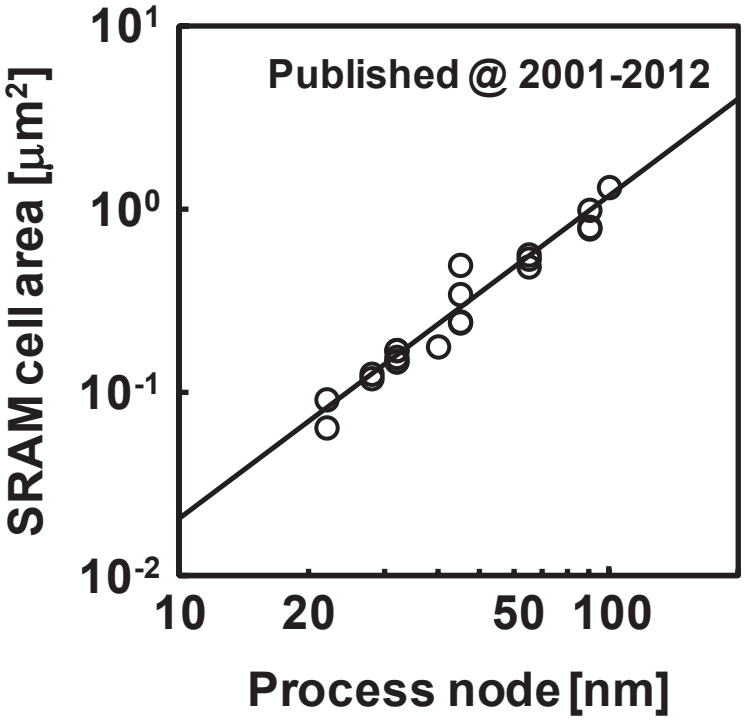


Fig. 6.19 Trend of 6T SRAM cell areas.

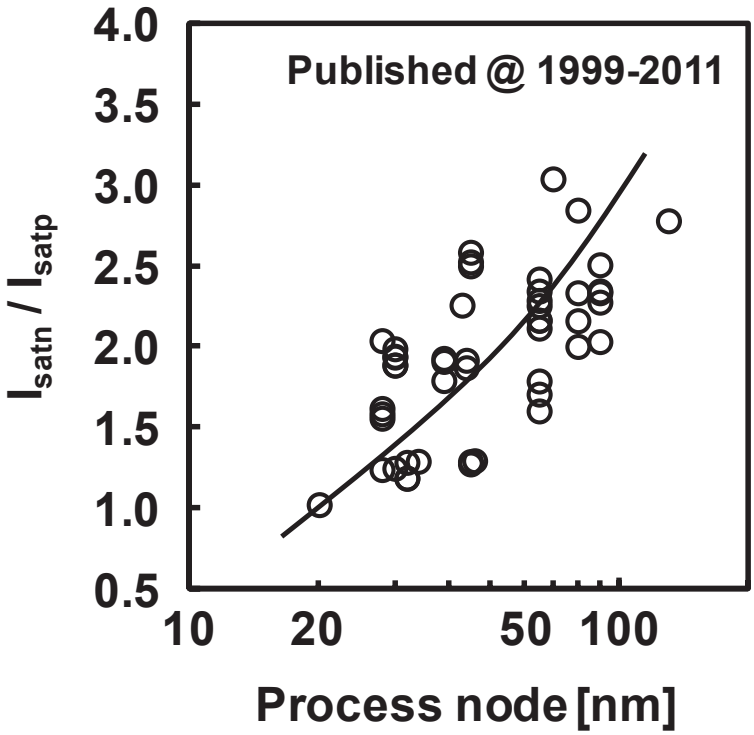


Fig. 6.20 Trend of saturation current ratios of I_{satn} to I_{satp}.

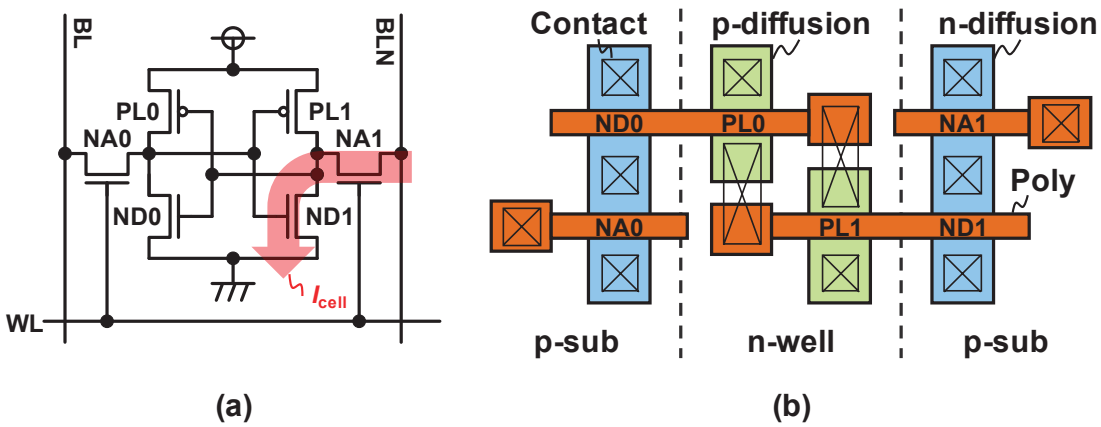


Fig. 6.21 (a) Schematic and (b) layout of a conventional 6T SRAM cell.

6.3.2 Proposed NMOS-PMOS Reversed 6T SRAM Cell

Figures 6.22(a), 6.22(b), and 6.22(c) respectively depict a schematic, a layout, and read waveforms of the proposed nMOS-pMOS (n-p) reversed 6T SRAM cell. The 6T cell consists of nMOS load transistors (NL0 and NL1), pMOS driver transistors (PD0 and PD1), and pMOS access transistors (PA0 and PA1). The number of transistors and the poly gate alignment are as shown in Fig. 6.22(b) although the n- and p-diffusions are swapped. The shared contacts are applicable for both 6T cells. Therefore, the proposed one has no area overhead. In a read operation, either bitline (BL or BLN in Fig. 6.22(a)) is pulled up by a cell current flowing through a pMOS access transistor. The proposed cell decreases a soft-error rate because it has a 33% smaller nMOS diffusion area than the conventional one and because the sensitive nMOS nodes share the same p-substrate.

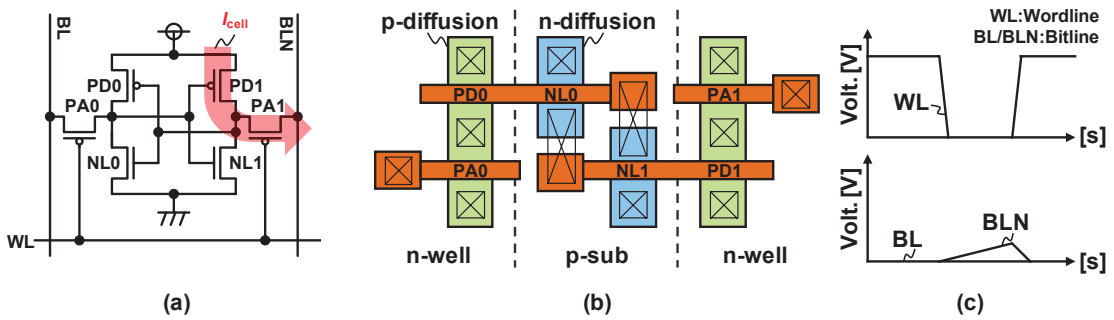


Fig. 6.22 (a) Schematic, (b) layout, and (c) read waveforms of the proposed n-p reversed 6T SRAM cell.

6.3.3 Simulation Setups

Table 6.2 presents a summary simulation parameters for the HSPICE circuit simulator and a particle transport code (PHITS). The supply voltage (VDD) and equivalent oxide thickness (EOT) for each process node are referred from the ITRS 2001–2011. The standard deviations of the threshold voltages for nMOS and pMOS (σ_{Vthn} and σ_{Vthp}) are normalized at the 65-nm node with the Stalk equation ($\sigma_{Vth} \propto$ EOT / √(channel area: width × length)). At the 65-nm node, σ_{Vthn} and σ_{Vthp} are 40 mV and 30 mV, respectively, for the minimum transistors, as derived from measurement results of test chips [66]. The respective saturation current ratio (I_{satn} / I_{satp}) and cell area are obtained using the fitting curves in Figs. 6.20 and 6.19. The critical charge is calculated with related works [27, 64] at each node.

Figure 6.23 shows the circuit setup for HSPICE to estimate static noise margins (SNMs) of the conventional and proposed cells. The SNM is defined as a minimum square in butterfly curves in Monte Carlo simulations (20 K trials). Furthermore, the cell current (I_{cell}) is taken from the minimum one by the SPICE Monte Carlo simulations, which reflects a readout speed.

Table 6.2 Simulation parameters.

Process node [nm]	VDD*1 [V]	EOT*1 [Å]	σ_{Vthn}*2 [mV]	σ_{Vthp}*2 [mV]	I_{sat} ratio*3 (I_{satn} / I_{satp})	Cell area*4 [μm^2]	Critical*5 charge [fC]
22	0.9	12	83.8	62.9	1.01	0.0813	0.224
32	1.0	15	64.6	48.5	1.40	0.1562	0.285
45	1.0	19	51.2	42.9	1.84	0.2830	0.430
65	1.1	21	40.0	30.0	2.26	0.5369	0.793
90	1.2	24	32.3	24.2	2.70	0.9465	1.700
130	1.2	27	25.7	19.3	3.08	1.7960	3.300

*1ITRS2001-2011, *2[20, 63], *3Fitting in Fig. 6.20, *4Fitting in Fig. 6.19, *5[27, 64]

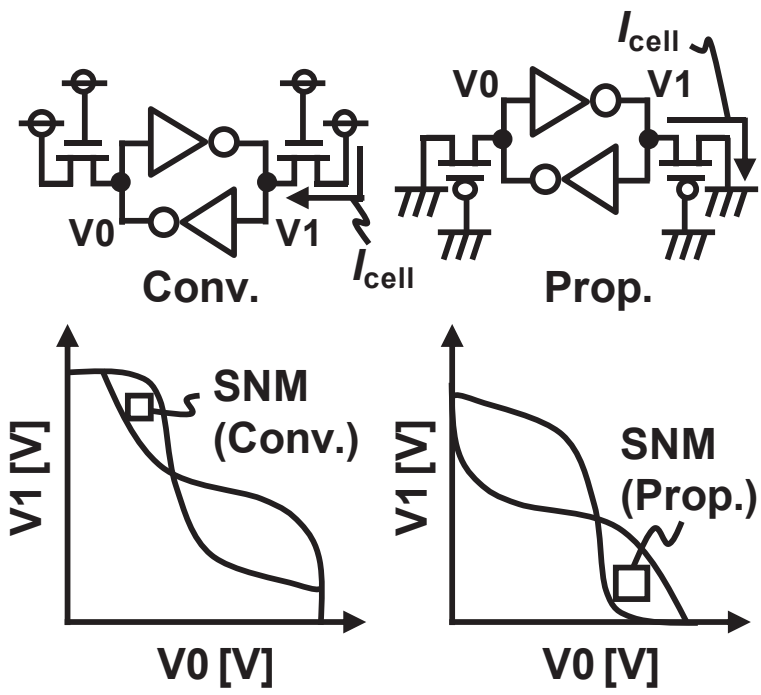


Fig. 6.23 Circuit setup for SNM and I_{cell} estimation.

6.3.4 Circuit and Soft-Error Simulation Results

The SNMs of the conventional and proposed 6T SRAM cells are calculated using the 20 K Monte Carlo HSPICE simulations at the worst process corners: The FS (nMOS = Fast; pMOS = Slow) corner for the conventional cell and the SF corner for the proposed cell. The I_{cell} is calculated at the SS corner. Figure 6.24 shows that the SNM and I_{cell} are decreasing continuously with process scaling attributable to the reduced VDD and the increased σ_{Vth}. The proposed cell, however, has a greater SNM and I_{cell} because the proposed cell has pMOS access and driver transistors and their σ_{Vthp} is smaller than the σ_{Vthn} in the conventional one. The SNM of the proposed cell is larger at every node and is 2.04 times as large at the 22-nm node. The I_{cell} in the proposed cell is larger than that in the conventional one at the 32-nm and less nodes and is 2.81 times as large at the 22-nm node.

Figure 6.25 shows neutron-induced soft-error simulation results. Although the critical charge is decreasing, the SBU SER is also decreasing with process scaling thanks to the smaller critical area. The MCU SER exhibits a similar tendency at the 65-nm and less nodes. The proposed n-p reversed cell has 33% smaller nMOS diffusion area. Therefore,

its SBU and MCU SERs are reduced by 11–51% and 34–70%, respectively, at the 22-nm node. Particularly for the column stripe pattern, the MCU SER is improved by 70% (but the SBU SER is decreased by only 11%) because nMOS diffusions in the conventional cells share the same p-substrate in the vertical direction and vertical MCUs easily occur. In the row stripe pattern, the MCU SER improvement is, however, the smallest, 34% (but the SBU SER improvement is the largest, 51%), because the distance from a sensitive nMOS node to another in the conventional cells is the longest among the four patterns.

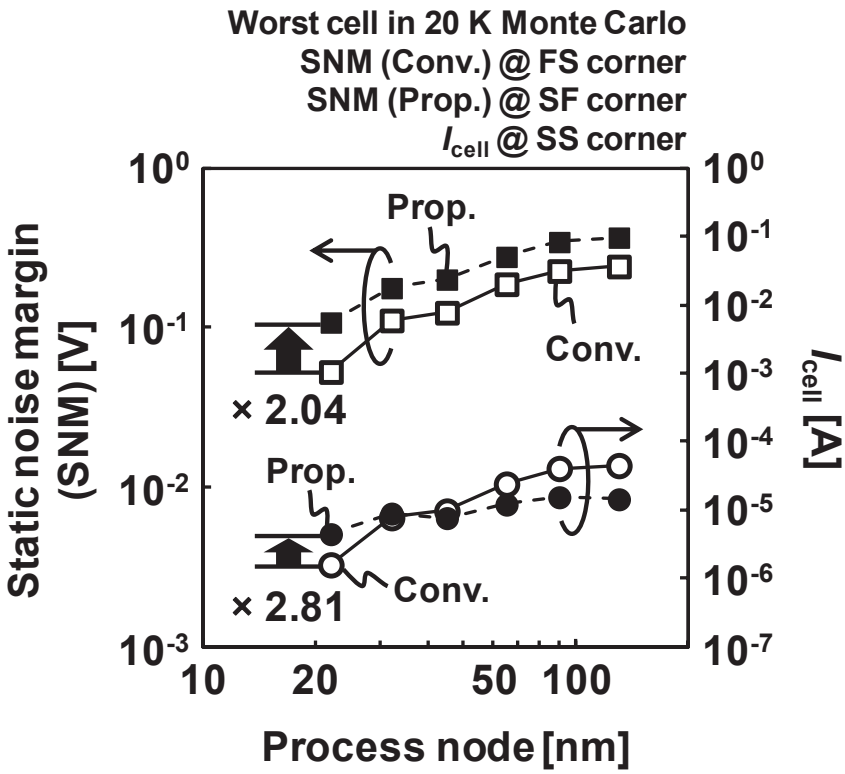


Fig. 6.24 SNM and I_{cell} comparisons between conventional and proposed cells.

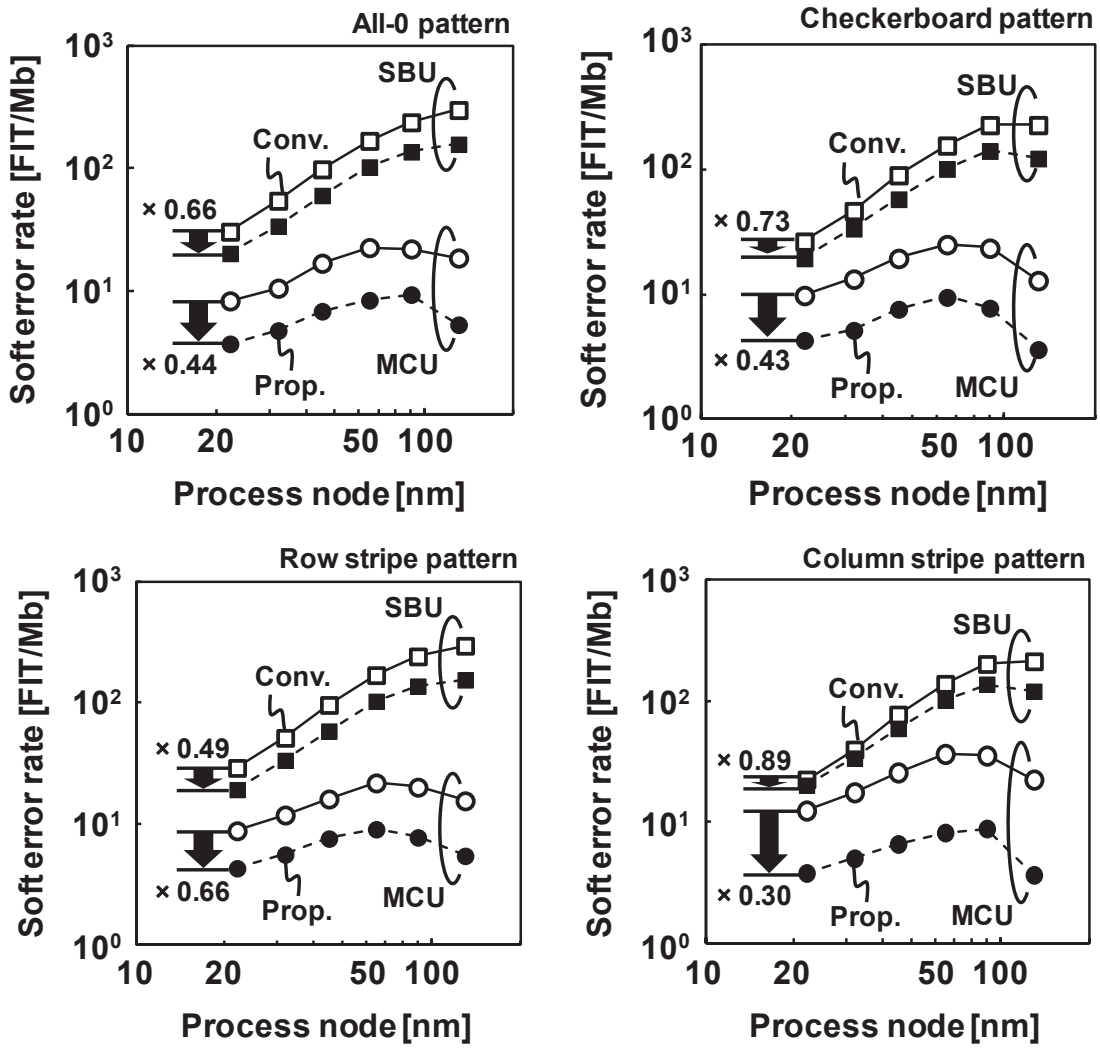


Fig. 6.25 SBU and MCU SERs of conventional and proposed cells.

6.4 Summary

As described in this chapter, we proposed 1) soft-error rate estimation tool, 2) nMOS-centered 6T SRAM, and 3) nMOS-pMOS reversed 6T SRAM:

1) First, the neutron-induced soft-error-rate (SER) estimation tool with a particle transport code (PHITS) is presented. The proposed tool can calculate the SER according to various data patterns and the layout of the memory cells in an SRAM.
2) Second, the PNP (NMOS-centered) 6T SRAM is presented to make a neutron-induced $MCU_{BL>1}$ SER lower than the general NPN 6T SRAM in the horizontal direction. We designed a 65-nm 1-Mb SRAM test chips including the

NPN and PNP SRAM macros. The measurement results demonstrate that the PNP layout suppresses the horizontal $MCU_{BL>1}$ SER by 67–98% in the CKB, ALL0, CS and RS patterns with the twin-well and triple-well structure in which the tap density is 1/32 of memory cells.

3) The nMOS-pMOS reversed 6T SRAM cell was proposed to improve the read stability, readout speed, and soft-error tolerance. At a 22-nm process, a static margin and cell current are improved, respectively, by factors of 2.04 and 2.81. Neutron-induced soft-error rates of the conventional proposed cells were investigated using the PHITS-based simulator. The proposed 6T cell improves the single-bit-upset and multiple-cell-upset soft-error rate by 11–51% and 34–70%, respectively, because the proposed n-p reversed cell has a 33% smaller nMOS diffusion than the conventional one and reduces a collected charge induced by a secondary ion.

Chapter 7 Conclusion

This dissertation presents robust circuit techniques for SRAM in the nanometer CMOS technology.

In Chapter 2, the intrinsic issues of the scaled SRAM are introduced as follows:

1) Decreased operating margin
2) Degraded energy efficiency
3) Poor soft-error immunity

In this study, the solutions to these issues are presented in Chapter 3 to Chapter 6 as shown in Fig. 7.1:

1) Half-select disturb tolerant 8T SRAM designs (Chapter 3)
2) Bitline limiting techniques for low-power 8T SRAM (Chapter 4)
3) Margin enhancement techniques for bit-error and soft-error tolerant SRAM (Chapter 5)
4) Neutron-induced soft-error simulator and soft-error resilient layout design (Chapter 6)

In Chapter 3, two half-select disturb tolerant SRAM designs are presented. First, the dual write wordline 8T SRAM leverages the sequential writing technique, which can mitigate the half-select problem. The write bitlines are precharged to half-VDD to decrease the disturb current. The proposed sequential writing technique further eliminates one of the two disturb currents, which thereby improves the half-select margin. The DW8T with sequential writing technique improves the half-select BERs by 71% at the disturb worst corner and by 79% at the typical corner, compared to a conventional 8T, respectively. The 256-Kb DW8T SRAM macro and the half-VDD generator are implemented on a single chip using a 40-nm CMOS process. The VDD_{min} of the proposed 256-Kb DW8T SRAM is improved by 367 mV on average among seven sample chips. Second, the disturb mitigation scheme is proposed to achieve low-power and low-voltage operation for an 8T SRAM. The proposed scheme has a 3.27σ yield at 0.5 V at the worst condition. The bitline charge energy is improved by 60% at a typical condition. The 512-Kb 8T SRAM test chips are implemented in a 40-nm bulk-CMOS process. The SRAM operates at a single 0.5-V supply voltage at room temperature and achieves 1.52-μW/MHz active energy in a write cycle and

72.8-μW leakage power, which are, respectively, 59.4% and 26.0% better than the conventional write-back scheme. The total energy is 12.9 μW/MHz at 0.5 V in a 50%-read / 50%-write operation.

Chapter 4 introduced two bitline swing-limiting techniques. The read bitline amplitude limiter (RBAL) and discharge acceleration (DA) scheme are presented first. The RBAL reduces the active energy dissipation by 13%–27% at 0.5 V. Circuits were implemented to 256-Kb SRAM macros by a 40-nm process. The energy dissipation in a cycle is less than 10 pJ / access at 0.5–0.7 V. Second, the selective source line control (SSLC) scheme and the address preset structure are proposed for a low-power 8T SRAM. The RBL swing is suppressed in an unselected column because the SSLC disconnects the source line (SL) of the dedicated read ports. Therefore, it does not fully discharge the unselected read bitlines (RBL). The 16-Kb 8T SRAM test chip implemented in a 40-nm bulk CMOS technology demonstrates that the SSLC with the address preset structure reduces read energy consumption by 57.2%, 0.0%, 45.0%, and 28.5%, respectively, in ALL0, ALL1, and CKB0 row address increments, and the CKB0 column address increment.

Chapter 5 presents two margin enhancement techniques for bit-error and soft-error resilient SRAM designs. First, the bit-error and soft-error tolerant 7T/14T SRAM is introduced. The 14T dependable mode improves the minimum operating voltage to 0.52 V from 0.66 V in the 7T normal mode. The respective alpha-induced and neutron-induced SERs in the 14T dependable mode are 80.0% and 34.4% less than that in the 7T normal mode. We observed a 10–70% increase of the 14T mode's Q_{crit} in a range of 0.3–1.5 V. The 7T/14T SRAM can change its BER and SER dynamically; the users can take a tradeoff between the reliability and area (cost), which is useful and effective for various applications. Second, the MBU-tolerant 8T SRAM cell layout is presented for the divided wordline structure. The layout improves MBU by 90.70%, and the MBU SER is decreased to 3.46 FIT at a supply voltage of 0.9 V. The TCAD simulation of results indicated that the proposed 8T cell layout improves the LET_{th} by 66% because of the common-mode effect. The proposed 8T SRAM array has a 48% area overhead over the conventional 6T SRAM. However, the minimum operation voltage can be improved by 0.45 V. Therefore, the operation power is decreased by 77.2%.

Chapter 6 presents a description of the neutron-induced soft-error simulator and two soft-error tolerant 6T bitcell layouts. First, the neutron-induced soft-error-rate (SER) estimation tool with a particle transport code (PHITS) is presented. The proposed tool can calculate the SER according to various data patterns and the layout of the memory cells in an SRAM. Second, the NMOS-centered 6T SRAM is presented to make a neutron-induced $MCU_{BL>1}$ SER lower than the general NPN 6T SRAM in the horizontal direction. We designed a 65-nm 1-Mb SRAM test chips including the NPN and PNP SRAM macros. The measurement results demonstrate that the PNP layout suppresses the horizontal $MCU_{BL>1}$ SER by 67–98% in the CKB, ALL0, CS, and RS patterns with the twin-well and triple-well structure in which the tap density is 1/32 of memory cells. Third, the nMOS–pMOS reversed 6T SRAM cell was proposed to improve the read stability, readout speed, and soft-error tolerance. At a 22-nm process, a static margin and cell current are improved, respectively, by factors of 2.04 and 2.81. Neutron-induced soft-error rates of the conventional proposed cells were investigated using the PHITS-based simulator. The proposed 6T cell improves the single-bit-upset and multiple-cell-upset soft-error rate by 11–51% and 34–70%, respectively, because the proposed n-p reversed cell has a 33% smaller nMOS diffusion than the conventional one and reduces the collected charge induced by a secondary ion.

Figure 7.2 compares conventional and the proposed low-power 8T SRAMs. The operating voltage and power consumption of the conventional 8T SRAM is assumed to be 1.0 V and 50%-read and 50%-write operation. The dual WL 8T SRAM in Section 3.1 can lower the operating voltage to 0.654 V, which reduces the power by 57.5%. The dual WL 8T SRAM with RBAL scheme in Section 4.1 reduces the read bitline energy by 22% at the CC corner. When the local read bitline consumes 10% of the total power, the operating power is reduced completely by 58.0% by the combination (3.1 + 4.1). The SSLC scheme additionally reduces the local and global bitline swings and can decrease the operating power by 67.1% in (3.1 + 4.2). The low-energy disturb mitigating scheme achieves 0.5 V operation and reduces the write energy by 59.4%. The operating energy was improved by 82.4%, 82.7%, and 88.1% using only the 8T SRAM (3.2), with RBAL scheme (3.2 + 4.1), and with SSLC scheme (3.2 + 4.2). Finally, the divided wordline 8T SRAM achieves 0.43 V operation. The 8T SRAM cannot cooperate with the other bitline swing limiting techniques because the SRAM has no half-selected

cells. The SRAM improves the operating power by 81.5%. Consequently, the low-energy disturb mitigating 8T SRAM with SSLC scheme presented in this dissertation can achieve the lowest energy consumption.

Figure 7.3 presents normalized single-bit-upset (SBU) and multiple-bit-upset (MBU) soft-error rates (SERs) for conventional and the proposed 6T SRAMs in Chapters 5–6. The 7T/14T SRAM in Section 5.1 can reduce the SBU SER by 34.4% using the dependable mode: the two 6T cells are mutually connected by the control transistors. The nMOS-centered 6T cell in Section 6.2 improves the MBU SER by 93.0% in the twin well and the checkerboard pattern. The nMOS-pMOS reversed 6T cell in Section 6.3 has 33% smaller nMOS diffusion than the nMOS-centered cell, which reduces the SBU and MCU SER by 33.3% and 96.9%. The 7T/14T SRAM with the nMOS-centered structure can improve the SBU and MCU SER by 33.3% and 93.0%, respectively. The dependable SRAM with the nMOS–pMOS reversed SRAM can lower the SBU and MCU SER by 56.7% and 96.9%, respectively. As reported in this dissertation, the 7T/14T SRAM with the nMOS-reversed structure achieves the minimum soft-error rate in the nanometer CMOS technology.

This dissertation presents practical circuit designs to achieve low-voltage, low-power, and soft-error tolerant SRAM in the nanometer CMOS process.

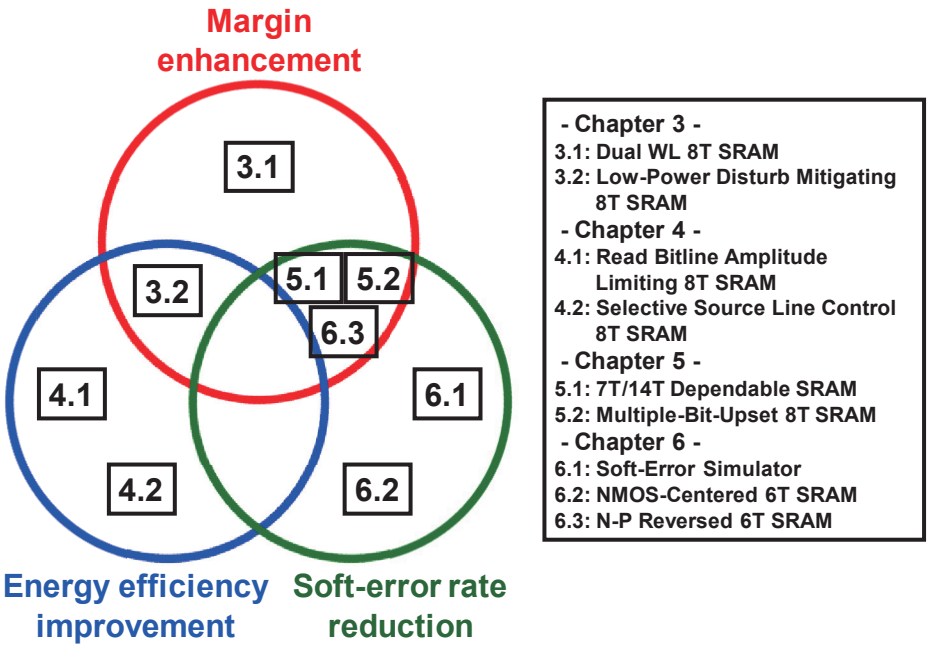


Fig. 7.1 Mapping of the proposed techniques in Chapter 3–6 for the issues in the nanometer CMOS technology.

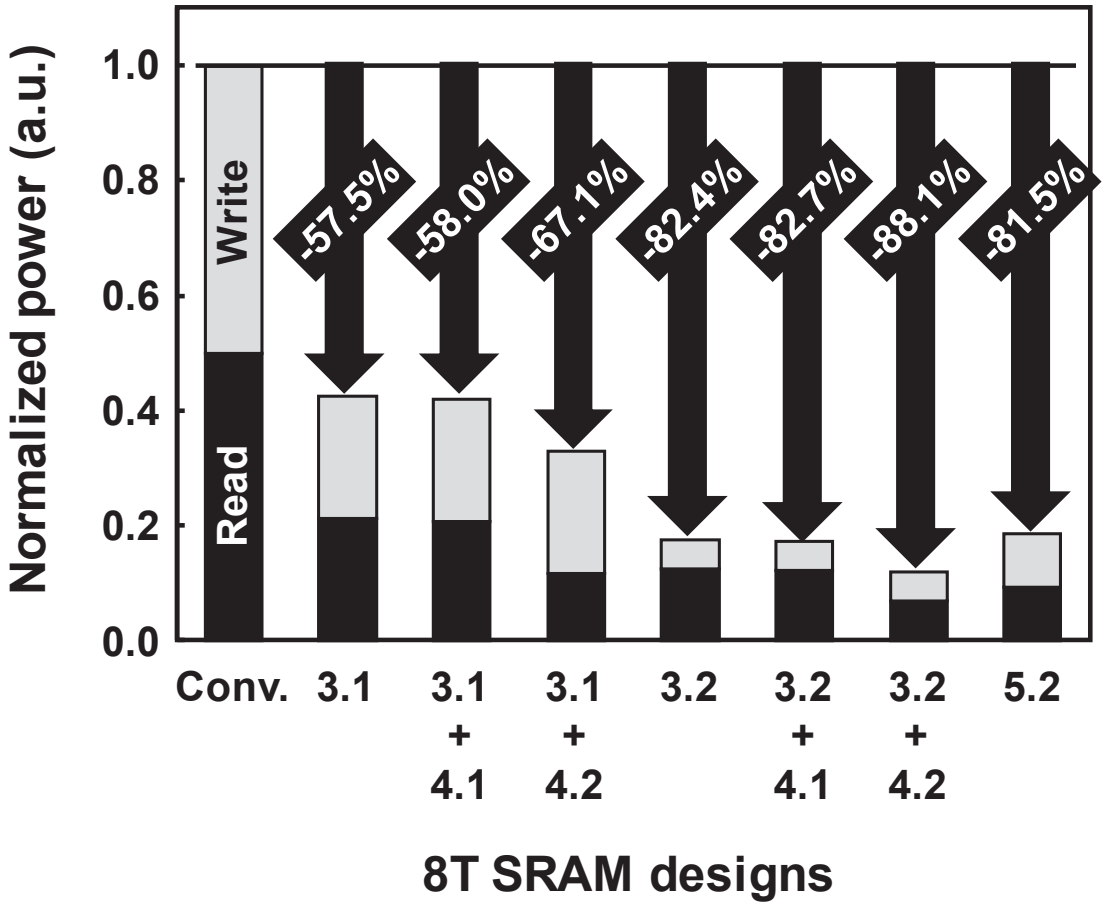


Fig. 7.2 Normalized power comparison using the proposed techniques in Chapter 3–6.

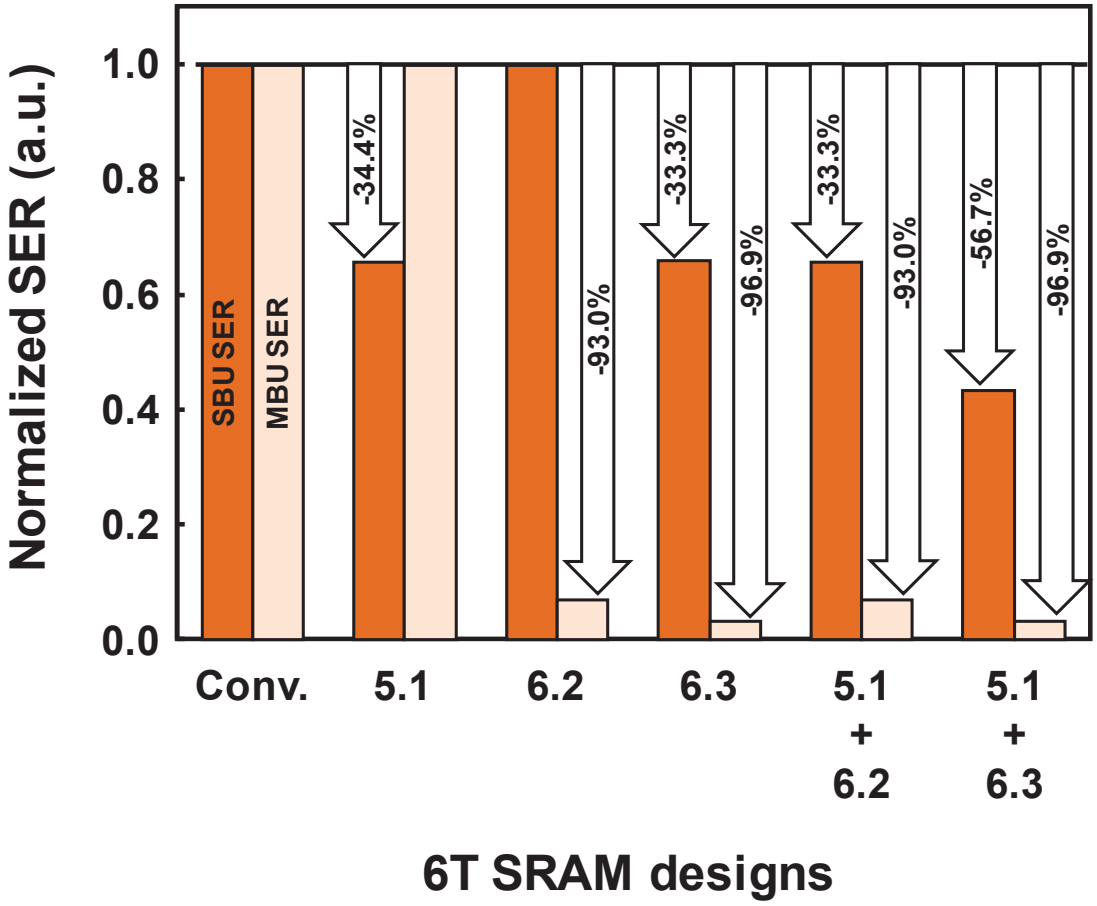


Fig. 7.3 Normalized soft-error rate comparison using the proposed techniques in Chapter 3–6.

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