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Doctoral Dissertation

博士論文

Study on threshold voltage and carrier mobility in organic thin-film transistors

有機薄膜トランジスタの閾値電圧およびキャリア移動度に関する研究

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Chapter 1
General Introduction

1.1 Background

Today, humans are living surrounded by a lot of electronic equipment such as personal computers and mobile phones. Electronics technology is an essential technology for human life. In particular, a transistor is the core device.

A metal-oxide-semiconductor field-effect transistor (MOSFET) using Si and SiO_2 was first reported by Kahng and Atalla in 1960 [1]. MOSFET is a device play a role of an electrical switch. Today, MOSFET is used for more than one million in one electronic device, and is an indispensable device in human life. Also, development of thin-film transistors (TFTs) using a hydrogenated amorphous silicon (a-Si:H) is important. TFT is different from FET in that the substrate and gate electrode are independent and the conducting channel is formed in the accumulation region. a-Si:H TFTs play an important role in applications where FETs are not suitable. The successes of transistors to date are achieved by improvements in these Si semiconductor.

Organic TFTs using organic materials have been attracted attention in recent years. Organic materials have advantages such as flexible, light-weight, and solubility. Thus, organic layer can be formed on an inexpensive substrate such as plastic and paper. In addition, organic layer can be deposited not only by vacuum process but also by printing process using organic solution. Therefore, by using organic materials, flexible, light-weight, large-area, low-cost, and thin devices can be fabricated. Organic TFTs are expected to realize a new type of electronic device

that is difficult for Si-based transistors.

1.2 Brief history of organic TFTs

Organic TFTs have been studied since the 1980's. Tsumura et al. reported the first organic TFT in 1986 [2]. The first organic TFT with polythiophene as an organic semiconductor showed a characteristic of a *p*-channel transistor and a field-effect mobility of about 10^{-5} $cm^2/(V\ s)$. Guillaud et al. reported *n*-channel organic TFTs using bisphthalocyanine derivatives in 1990 [3]. Since these reports, many researchers have investigated organic TFTs.

Many of the improvements in performance of organic TFTs have been focused on the improvements in a field-effect mobility. Figure 1 shows the evolution of field-effect mobility in organic TFTs depending on fabrication processes [4]. The mobility is 10^{-5} $cm^2/(V\ s)$ in the first report of 1986, and over 10 $cm^2/(V\ s)$ in 2015. The mobility has improved 10^6 times in the last 30 years. The mobility of organic TFTs exceeds that of a-Si (about 0.5 $cm^2/(V\ s)$) transistors. Therefore, the organic TFTs are considered to have practical performance in terms of the mobility.

Improvements in the organic semiconductor materials, device structures, and fabrication techniques contribute to the improvements of the mobility. In particular, the variety of fabrication techniques available for organic TFTs is a major advantage over Si MOSFETs. Organic TFTs are fabricated by thermal evaporation or solution process. The optimized process has contributed to not only improve device performance shown in Fig. 1.1 but also reduce deposition cost and time.

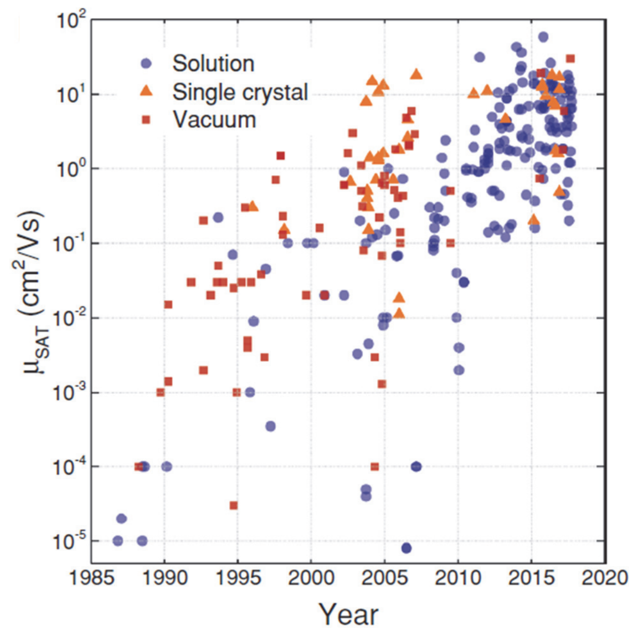


Figure 1.1: Evolution of field-effect mobility in organic TFTs depending on fabrication processes. [4]

1.3 Structure of organic TFTs

Figure 1.2 shows commonly used structures of organic TFTs. An organic TFT is made of four parts. They are a gate electrode, a gate dielectric, an organic semiconductor layer, and source/drain electrodes. The source and drain electrodes are in direct contact with the organic semiconductor layer. The gate electrode is isolated from the organic semiconductor by the gate dielectric. The current through the organic semiconductor is controlled by applying voltage to gate and drain electrode and connecting source electrode to ground. The structure of an organic TFT is called bottom-contact (shown in Fig. 1.2(a)) or top-contact (shown in Fig. 1.2(b)) structure depending on the positions of source/drain electrodes and organic semiconductor. Each of these structures has advantages. In the bottom-contact structure, source/drain electrodes are deposited on the gate dielectric. Because the micro-patterning techniques such as photolithography can be used, organic TFTs with micro channel-length can be fabricated easily. Reducing channel-length is important for TFTs to operate at high frequency. However, it is

difficult to fabricate the top-contact structure by using these micro-patterning techniques. This is because the organic semiconductor molecules are easily destroyed by high temperature, light irradiation, or an organic solvent. On the other hand, contact resistance at interface between the organic semiconductor and source/drain electrodes has been reported to be lower in top-contact structure than bottom-contact structure [5-7]. Therefore, the top-contact organic TFT tends to have good characteristics than bottom-contact one. Some groups have reported various other structures such as top-gate [8], floating-gate [9], and double-gate structures [10].

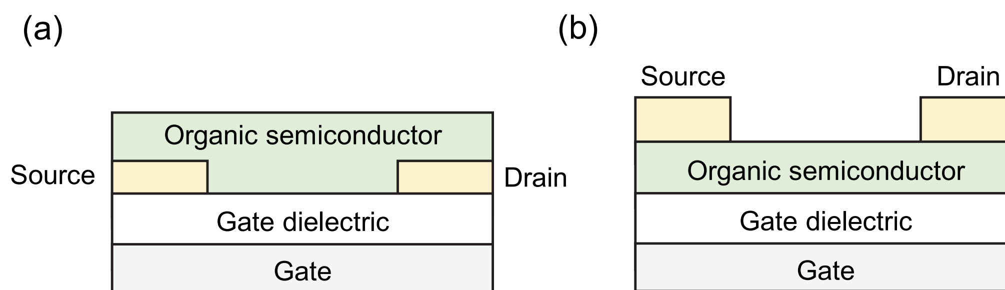


Figure 1.2: Illustration of bottom-gate (a) bottom-contact and (b) top-contact structures of organic TFTs.

1.4 Semiconductor properties of organic molecules

Carrier density and carrier mobility of organic semiconductor using for an organic TFT are much smaller than those of Si semiconductor. Thus, organic semiconductors are materials with characteristics closer to dielectrics than semiconductors [11]. This indicates that organic semiconductors are intrinsic semiconductors.

The operating mode of the semiconductor is classified into *n*-type or *p*-type depending on whether the conduction carrier is electron or hole. The operating mode of a Si semiconductor is determined by controlling the carrier density by doping donors or acceptors. On the other

hands, for organic semiconductors, because the carrier density in the organic semiconductor is low, it is difficult to control the carrier density by doping. Also, the organic molecules may be destroyed by doping. Thus, the carriers inside an organic semiconductor are dominated by the carriers injected from an electrode that is in direct contact with the organic semiconductor. In other words, the carriers accumulate in the organic semiconductor only when they are injected from the electrode. The injection barrier between an electrode and organic semiconductor affects carrier transport.

The operating mode of the organic TFTs depends on the positions of the work function of electrode and the frontier orbitals (highest occupied molecular orbitals, HOMO, and lowest unoccupied molecular orbitals, LUMO) of organic semiconductor. As an example, the case of pentacene and gold is explained. They are materials typically used for organic TFTs. Figure 1.3 shows the energy schemes of pentacene and gold. Data for pentacene and gold was taken from Ref. 12 and 13. The work function of gold and the HOMO level of pentacene are almost in the same position. This indicates that holes are easily injected because the injection barrier height for holes is low. On the other hand, the difference between the work function of gold and the LUMO level of pentacene is about 2 eV. This difference is much higher than the thermal energy at room temperature (0.026 eV). It is difficult to inject electrons in pentacene from Au. Therefore, when using pentacene as a semiconductor and gold as a contact metal, pentacene shows the conduction characteristic of a *p*-type semiconductor [12].

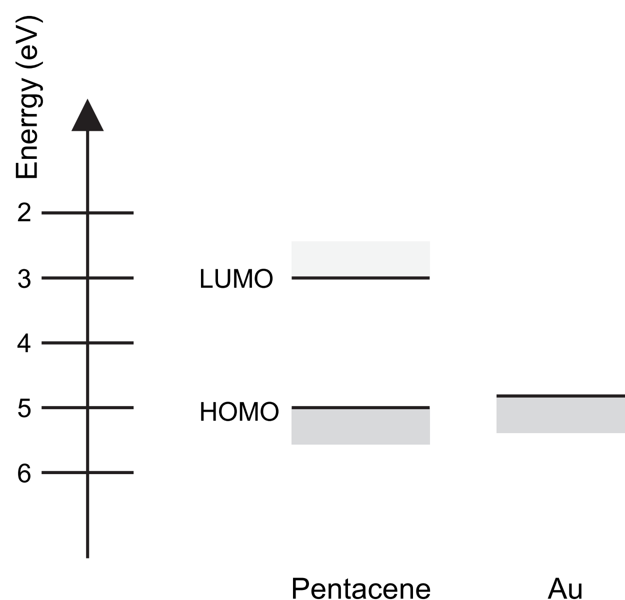


Figure 1.3: Energy schemes of pentacene and gold.

1.5 Charge transport for organic TFTs

The interfaces between the organic semiconductor and the source/drain electrodes and between the organic semiconductor and the gate dielectric have an important role for the performance of organic TFTs.

Carriers injected from the drain electrode flow through the organic semiconductor to the source electrode. Carrier transport is limited by contact resistance at the interface between the organic semiconductor and the source/drain electrodes. The contact resistance strongly affects the characteristics of the organic TFT. In particularly, a large contact resistance is a problem when the channel length between the source and drain electrodes is short. The injection barrier between the organic semiconductor and the source/drain electrodes in Fig. 1.3 is the main cause of the contact resistance. Thus, the characteristic is improved by matching the work function of the contact metal with the HOMO or LUMO level of the organic semiconductor. Modification

of the metal surface with a monolayer is one method to change the work function of the metal [13-15]. For example, by modifying the Au surface with pentafluorobenzenthiol (PFBT), work function of Au shifts from 4.8 eV to 5.5 eV [13]. Also, TFT characteristics are improved [16].

A channel region for carrier transport is formed within the organic semiconductor near the interface between the organic semiconductor and the gate dielectric [17]. In addition, the quality of organic semiconductor crystals depends on the flatness and energy of the gate dielectric surface. The organic semiconductor crystals change when treated with UV ozone or a self-assembled monolayer (SAM) [18-20]. Therefore, the interface properties also affect the characteristics of the organic TFT [19,20].

1.6 Materials for organic TFTs

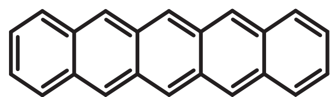
1.6.1 Organic semiconductor materials

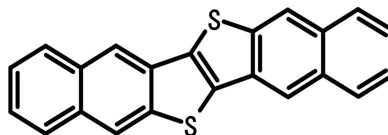
Many organic semiconductor materials used in organic TFTs have been reported because of the ease of designing new organic molecules. Figure 1.4 shows typical organic semiconductor materials used in organic TFTs. Organic semiconductor materials are classified as small molecules or polymers.

Small molecular materials have the advantage of showing better transistor characteristics than polymer materials. Pentacene is the material most used for *p*-channel organic TFTs [12]. As other materials, dinaphtho[2,3-*b*:2',3'-*f*]thieno[3,2-*b*]thiophene (DNTT) [21,22] and copper phthalocyanine (CuPc) [23] are famous materials as *p*-channel organic TFTs. On the other hand, fullerene C_{60} [24] and C_{60} derivatives [25] are generally used for *n*-channel organic TFTs. Because many small molecular materials are difficult to dissolve in organic solvent, they were generally deposited by thermal vapor deposition. On the other hand, solubility in organic solvents can be obtained by introducing side chains into the small molecular material such as alkyl DNTT [26,27] and 6,13-bis(triisopropyl-silyethynyl) pentacene [28,29]. In small

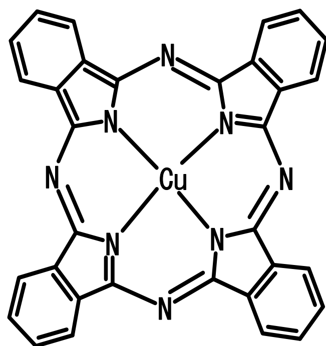
molecular materials with side chains, organic semiconductor layer can be formed by using solution processes such as inkjet and spin coat.

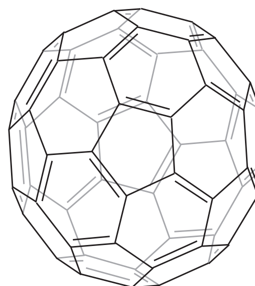
Polymer materials have the advantage of being easy to form an organic semiconductor film by using solution process. Solution process is available for small molecular materials. However, the stability of the characteristics of organic TFTs with small molecule semiconductor formed by solution process is low. In polymer materials, a uniform semiconductor film can be easily form by using solution process and TFTs operate stably. For polymer materials, poly(3-hexythiophene) (P3HT) [30,31] and poly(9,9-dioctylfluorene-co-bithiophene) (F8T2) [31,32] is widely used for organic TFTs.



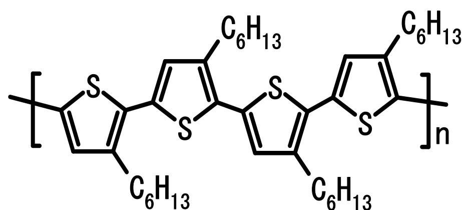


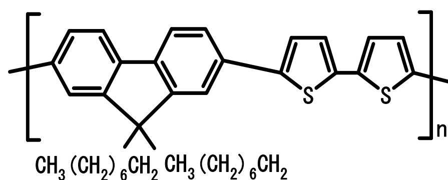
Pentacene **DNTT**





CuPc **C_{60}**





P3HT **F8T2**

Figure 1.4: Typical organic semiconductor materials for organic TFTs.

1.6.2 Gate dielectric materials

Gate dielectrics are as important as organic semiconductors. The gate dielectrics are required to have various properties such as high withstand voltage, high gate capacitance, flatness of surface, low surface energy, and mechanical flexibility. The dielectric materials are selected according to the application. As the gate dielectric materials for organic TFTs, inorganic materials or organic polymer materials are used.

SiO_2 is the most used materials for gate dielectric of organic TFTs. SiO_2 is easy to form a film and has excellent electrical and mechanical stability. However, the characteristics of organic TFTs are limited by the trapping sites and surface energy on the SiO_2 surface. In particular, surface energy strongly affects the quality of the organic semiconductor crystals formed on the gate dielectric. Their influence has been partially improved by covering the SiO2 surface with a SAM. For SAM materials, silane molecules, such as hexamethyldisilazane [33] and alkyl trichlorosilane [34,35], and phosphonic acid molecules [36] are used.

Organic polymer dielectrics are used to take advantage of its mechanical flexibility. Because the surface of organic polymer dielectrics is covered with organic molecules, they lead to good crystallinity of an organic semiconductor. For organic polymer dielectric materials, parylene [37,38] and CYTOP [39] are widely used. The flexible organic TFTs with organic polymer dielectric show performance close to that of the organic TFTs with SiO2 dielectric.

In many reports, organic TFTs operate at a high voltage of several tens of volts. Driving organic TFTs at low voltage is important to reduce power consumption of devices. In order to operate organic TFTs at low voltage, the gate dielectrics need to have a high gate capacitance. The gate capacitance C_{OX} is given as ε/d, where d is the thickness and ε is the dielectric constant of the gate dielectric. High dielectric constant or thin dielectric layer is needed to obtain a high gate capacitance. Thinning the gate dielectric layer may cause dielectric breakdown. Thus, use of dielectric materials with high dielectric constant (high-k) is effective for organic TFTs to

operate at low voltage. For high-*k* dielectric materials, Al_2O_3, TiO_2 or HfO_2 is used [40]. By using these materials, low voltage operation of organic TFTs is achieved.

1.7 Purpose of this thesis

Organic TFTs have various issues for practical applications. Control of the threshold voltage and accurate evaluation of the mobility for their applications are important issues. For a Si semiconductor, the threshold voltage can be controlled by changing the doping concentration. However, it is difficult to dope donor or acceptor in an organic semiconductor. Hence, control method of the threshold voltage in organic TFTs is not established. On the other hand, the mobility of organic TFTs is generally evaluated by using the current–voltage characteristics. However, this method evaluates the mobility including the contact resistance. Methods for controlling the threshold voltage and evaluating the intrinsic mobility of organic TFTs are required. In this thesis, influence of oxygen plasma treatment on the threshold voltage in organic TFTs is investigated. Furthermore, the charge at the surface of gate dielectric induced by oxygen plasma is evaluated quantitatively. In addition, the intrinsic mobility without including the contact resistance is evaluated by using a MOS capacitor structure.

1.8 Outline of this thesis

This thesis is structured in six chapters. Chapters 1 and 2 are the introductory part in this thesis. In chapter 1 “General Introduction”, brief introduction of organic TFTs were mentioned as research background. The TFTs, organic semiconductors and materials were briefly described. Then, purpose and outline of this thesis were described.

In chapter 2 “Analytical Methods of Organic Transistor Characteristics”, the typical analytical model for organic TFTs is summarized. Calculation methods for parameters, such as

field-effect mobility, threshold voltage, and contact resistance, in organic TFTs are presented.

Chapters 3 through 5 are the main part in this thesis. The main part is divided into two parts. One is about influence of oxygen plasma treatment on the threshold voltage in organic TFTs and the other is about evaluation of the intrinsic mobility of organic TFTs. The former is described in chapters 3 and 4, and the latter is described in chapter 5.

In chapter 3 “Operational Stability in Pentacene Thin-Film Transistors with Threshold Voltages Tuned by Oxygen Plasma Treatment”, organic TFTs having a gate dielectric treated with oxygen plasma have been investigated for control of the threshold voltage. The relationship between threshold voltage and oxygen plasma treatment is discussed. In addition, the influence of gate bias stress on threshold voltage is described.

In chapter 4 “Energy Distribution of Interface States Generated by Oxygen Plasma Treatment”, the characteristics of organic MOS capacitors have been investigated for evaluation of energy distribution of interface states. The relationship between oxygen plasma treatment and the MOS capacitor characteristics is described. The energy distribution of the interface states induced by oxygen plasma treatment is discussed.

In chapter 5 “Evaluation of Organic Metal-Oxide-Semiconductor Capacitors Based on a Distributed Constant Circuit”, the capacitance characteristics of organic MOS capacitors with a uncovered semiconductor area have been investigated for evaluation of the intrinsic mobility. The mobility of a MOS capacitor with an uncovered area is described assuming that the uncovered area is represented by a distributed constant circuit. In addition, the mobilities were compared with those calculated from the current–voltage characteristics of TFTs.

In chapter 6 “Conclusions”, the results in this thesis are summarized.

1.9 References

[1] D. Kahng, IEEE Trans. Electron Devices **23**, 655 (1976).

[2] A. Tsumura, H. Koezuka, and T. Ando, Appl. Phys. Lett. **49**, 1210 (1986).

[3] G. Guillaud, M. Al Sadoun, and M. Maitrot, Chem. Phys. Lett. **167**, 503 (1990).

[4] A. F. Paterson, S. Singh, K. J. Fallon, T. Hodsden, Y. Han, B. C. Schroeder, H. Bronstein, M. Heeney, I. McCulloch, and T. D. Anthopoulos, Adv. Mater. **30**, 1801079 (2018).

[5] K. Shibata, H. Wada, K. Ishikawa, H. Takezoe, and T. Mori, Appl. Phys. Lett. **90**, 193509 (2007).

[6] P. V. Necliudov, M. S. Shur, D. J. Gundlach, and T. N. Jackson, Solid-State Electron. **47**, 259 (2003).

[7] K. P. Puntambekar, P. V. Pesavento, and C. D. Frisbie, Appl. Phys. Lett. **83**, 5539 (2003).

[8] D. K. Hwang, C. F.-Hernandez, J. Kim, W. J. Potscavage Jr., S.-J. Kim, and B. Kippelen, Adv. Mater. **23**, 1293 (2011).

[9] T. Yokota, T. Sekitani, T. Tokuhara, N. Take, U. Zschieschang, H. Klauk, K. Takimiya, T.-C. Huang, M. Takamiya, T. Sakurai, and T. Someya, IEEE Trans. Electron. Devices **59**, 3434 (2012)

[10] K. Hizu, T. Sekitani, T. Someya, and J. Otsuki, Appl. Phys. Lett. **90**, 093504 (2007).

[11] R. Tamura, E. Lim, T. Manaka, and M. Iwamoto, J. Appl. Phys. **100**, 114515 (2006).

[12] M. Kitamura, and Y. Arakawa, J. Phys.: Condens. Matter **20**, 184011 (2008).

[13] Y. Kuzumoto, and M. Kitamura, Appl. Phys. Express **7**, 035701 (2014).

[14] I. H. Campbell, S. Rubin, T. A. Zawodzinski, J. D. Kress, R. L. Martin, D. L. Smith, N. N. Barashkov, and J. P. Ferraris, Phys. Rev. B **54**, 14321 (1996).

[15] S. D. Evans, and A. Ulman, Chem. Phys. Lett. **170**, 462 (1990).

[16] J. W. Borchert, B. Peng, F. Letzkus, J. N. Burghartz, P. K. L. Chan, K. Zojer, S. Ludwigs, and H. Klauk, Nat. Commun. **10**, 1119 (2019).

[17] C. D. Dimitrakopoulos, and P. R. L. Malenfant, Adv. Mater. **14**, 99 (2002).

[18] C.-L. Fan, Y.-Z. Lin, and C.-H. Huang, Semicond. Sci. Technol. **26**, 045006 (2011).

[19] S. Kang, S. Jung, J. Park, H.-J. Lee, and M. Yi, Microelectron. Eng. **84**, 1503 (2007).

[20] D. Kumaki, M. Yahiro, Y. Inoue, and S. Tokito, Appl. Phys. Lett. **90**, 133511 (2007).

[21] R. Yamamoto, K. Noda, Y. Wada, and T. Toyabe, Electron. Commun. Jpn. **100**, 61 (2017).

[22] U. Kraft, K. Takimiya, M. J. Kang, R. Rödel, F. Letzkus, J. N. Burghartz, E. Weber, and H. Klauk, Org. Electron. **35**, 33 (2016).

[23] R. Zeis, T. Siegrist, and Ch. Kloc, Appl. Phys. Lett. **86**, 022103 (2005).

[24] M. Kitamura, S. Aomori, J. H. Na, and Y. Arakawa, Appl. Phys. Lett. **93**, 033313 (2008).

[25] P. H. Wöbkenberg, D. D. C. Bradley, D. Kronholm, J. C. Hummelen, D. M. de Leeuw, M. Cölle, and T. D. Anthopoulos, Synth. Met. **158**, 468 (2008).

[26] M. Ito, T. Uemura, J. Soeda, and J. Takeya, Org. Electron. **14**, 2144 (2013).

[27] K. Nakayama, Y. Hirose, J. Soeda, M. Yoshizumi, T. Uemura, M. Uno, W. Li, M. J. Kang, M. Yamagishi, Y. Okada, E. Miyazaki, Y. Nakazawa, A. Nakao, K. Takimiya, and J. Takeya, Adv. Mater. **23**, 1626 (2011).

[28] S. K. Park, T. N. Jackson, J. E. Anthony, and D. A. Mourey, Appl. Phys. Lett. **91**, 063514 (2007).

[29] J.-P. Hong, A.-Y. Park, S. Lee, J. Kang, N. Shin, and D. Y. Yoon, Appl. Phys. Lett. **92**, 143311 (2008).

[30] B. H. Hamadani, and D. Natelson, Appl. Phys. Lett. **84**, 443 (2004).

[31] T. Nagase, T. Hirose, T. Kobayashi, R. Ueda, A. Otomo, and H. Naito, Appl. Sci. **8**, 1274 (2018).

[32] L. Bürgi, T. J. Richards, R. H. Friend, and H. Sirringhaus, J. Appl. Phys. **94**, 6129 (2003).

[33] J. B. Koo, S. H. Kim, J. H. Lee, C. H. Ku, S. C. Lim, and T. Zyung, Synth. Met. **156**, 99 (2006).

[34] F. Gholamrezaie, A.-M. Andringa, W. S. C. Roelofs, A. Neuhold, M. Kemerink, P. W. M. Blom, and D. M. de Leeuw, Small **8**, 241 (2012).

[35] Y. Chung, E. Verploegen, A. Vailionis, Y. Sun, Y. Nishi, B. Murmann, and Z. Bao, Nano Lett. **11**, 1161 (2011).

[36] M. Salinas, C. M. Jäger, A. Y. Amin, P. O. Dral, T. M.-Friedrichsen, A. Hirsch, T. Clark, and M. Halik, J. Am. Chem. Soc. **134**, 12648 (2012).

[37] K. Fukuda, T. Suzuki, D. Kumaki, and S. Tokito, Phys. Status Solidi A **209**, 2073 (2012).

[38] V. Podzorov, V. M. Pudalov, and M. E. Gershenson, Appl. Phys. Lett. **82**, 1739 (2003).

[39] W. L. Kalb, T. Mathis, S. Haas, A. F. Stassen, and B. Batlogg, Appl. Phys. Lett. **90**, 092104 (2007).

[40] R. P. Ortiz, A. Facchetti, and T. J. Marks, Chem. Rev. **110**, 205 (2010).

Chapter 2
Analytical Methods of Organic Transistor Characteristics

2.1 Introduction

In this chapter, equations for the evaluation and analysis of organic thin-film transistors (TFTs) characteristics are summarized. Firstly, the current–voltage characteristics and their equations generally used for evaluating organic TFTs are presented. Then, the evaluation method of the field-effect mobility, the threshold voltage, and the contact resistance is presented. Finally, relationship between threshold voltage and charge density is described.

2.2 Characteristics of organic TFTs

2.2.1 Current–voltage characteristics

The characteristics of organic TFTs are almost similar to those of Si transistors. Figures 2.1(a) and 2.1(b) show reported examples of drain current (I_D) versus drain voltage (V_D) and drain current versus gate voltage (V_G) characteristics of a pentacene TFT, respectively [1]. The drain current decreases with the gate voltage and saturates below a certain drain voltage. Their characteristics show typical *p*-channel MOSFET (field-effect transistor) characteristics. Therefore, standard analysis model for Si MOSFETs can be applied to organic TFTs. The following three approximations are assumed as correct [2]:

1. The channel length is much larger than the thickness of the gate dielectric and the carrier accumulation layer.

2. The field-effect mobility does not depend on electric field.
3. Only carriers accumulate when the gate voltage is applied.

The organic TFTs operate in saturation, linear, and cutoff regime. The drain current I_D flowing from the drain to the source for a *p*-cannel organic TFT is given by

$$I_D = -\frac{1}{2}\mu_{FE} C_{OX} \frac{W}{L}(V_G - V_{TH})^2 \qquad \text{for } |V_D| \geq |V_G - V_{TH}|, \qquad (2.1a)$$

$$I_D = -\mu_{FE} C_{OX} \frac{W}{L}\left[(V_G - V_{TH})V_D - \frac{1}{2}V_D^2\right] \qquad \text{for } |V_D| \leq |V_G - V_{TH}|, \qquad (2.1b)$$

$$I_D = 0 \qquad \text{for } V_G > V_{TH}, \qquad (2.1c)$$

where W and L are the channel width and length, μ_{FE} is the field-effect mobility, C_{OX} is the gate capacitance per unit area, V_{TH} is the threshold voltage, V_G and V_D are the source-gate and the source-drain voltages.

When $|V_D| << |V_G - V_{TH}|$, the drain current is approximated as

$$I_D \cong -\mu_{FE} C_{OX} \frac{W}{L}(V_G - V_{TH})V_D. \qquad (2.2)$$

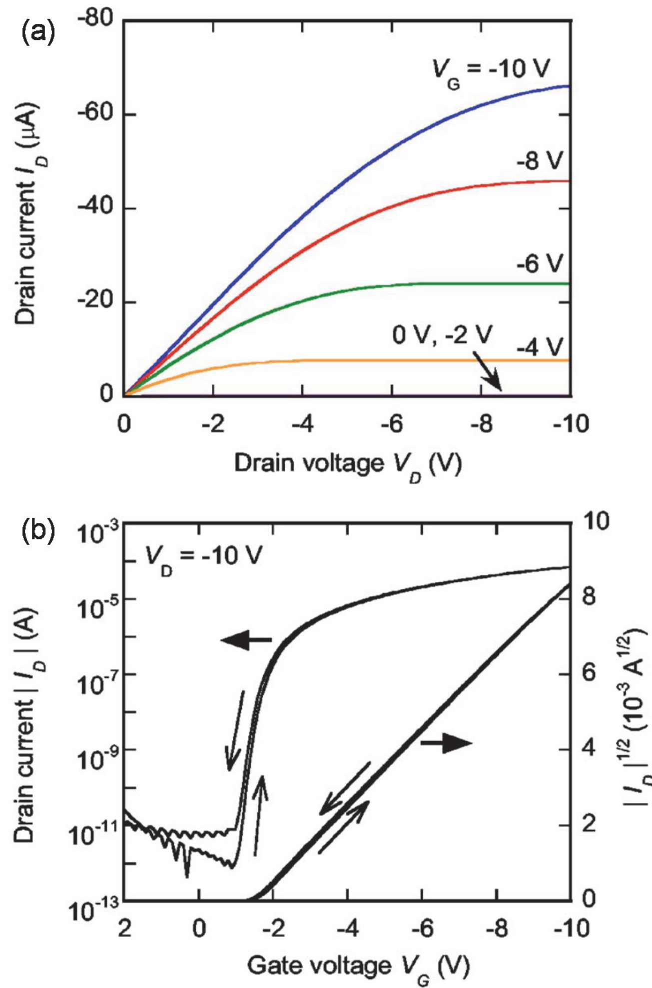


Figure 2.1: (a) Drain current versus drain voltage characteristics at various gate voltages and (b) drain current versus gate voltage characteristics of a pentacene TFT. [1]

2.2.2 Field-effect mobility and threshold voltage

In TFTs, the field-effect mobility and the threshold voltage are very important parameters. The field-effect mobility indicates the ease of carrier transport in semiconductor when an electric field is applied. The threshold voltage indicates the gate voltage at which drain current begins to flow. The field-effect mobility (μ_{sat}) and the threshold voltage values experimentally estimated in the saturation regime are calculated by fitting a line to a measured $|I_D|^{1/2}$-V_G curve with Eq. (2.1a). The experimental field-effect mobility (μ_{lin}) in the liner regime is calculated

from a measured $|I_D|$-V_G curve using Eq. (2.1b).

2.2.3 Contact resistance and sheet resistance

The contact resistance R_C between the organic semiconductor and the source/drain electrodes is estimated by using various methods such as transfer line method [3-5], gated four probe method [6], and Kelvin probe force microscopy [7]. The transfer line method is the most used method for experimentally evaluating the contact resistance. The contact resistance is estimated by the following procedure. First, the I_D-V_D characteristics of organic TFTs with several channel lengths are measured. Next, the on-resistance R_{ON}, which is defined as $|\partial V_D / \partial I_D|$ in the linear regime, is plotted for the channel length. Figure 2.2(a) shows an example of measured the on-resistance as a function of the channel length and the gate voltage [8]. The on-resistance increases linearly with the channel length. The on-resistance is assumed to be

$$R_{ON} = R_{ch} + R_C = \frac{L}{\mu_I W C_{OX} |V_G - V_{TH}|} + R_C , \quad (2.3)$$

Where R_{ch} is the channel resistance, μ_I is the mobility in the intrinsic transistor without contact resistance. The R_C and R_{ch} are estimated from the intercept and slope of figure 2.2(a). Figure 2.2(b) shows an example of the calculated R_C and R_{ch} [8]. The sheet resistance R_{TFT} is given by

$$R_{TFT} = R_{ch} \frac{W}{L} = \frac{1}{\mu_I C_{OX} |V_G - V_{TH}|} . \quad (2.4)$$

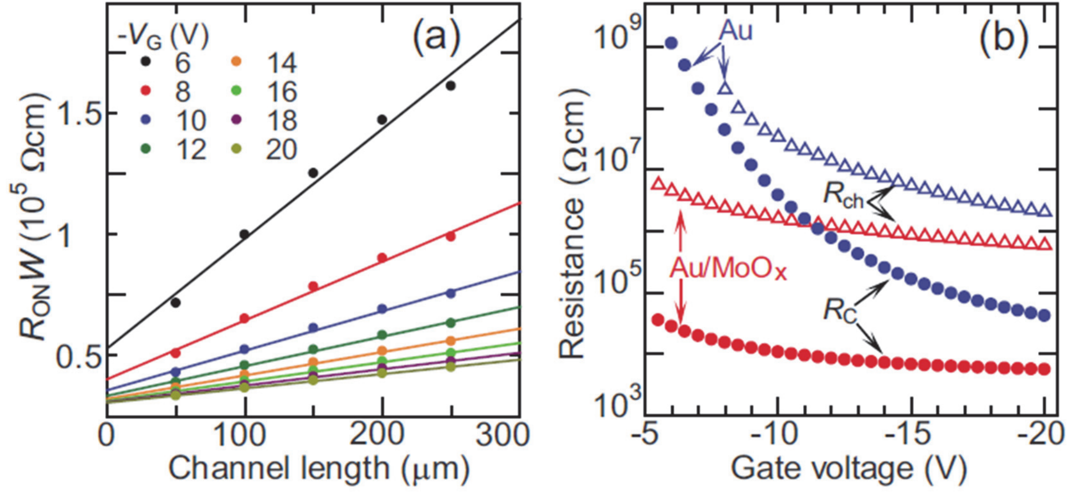


Figure 2.2: (a) Channel width normalized on-resistance as a function of channel length and gate voltage V_G. (b) Channel width normalized contact resistance and channel resistance as a function of V_G. [8]

2.2.4 Relationship between threshold voltage and charge density

Many organic TFTs operate in the accumulation mode. Therefore, the threshold voltage of organic TFTs equals the flat band voltage. Thus, the threshold voltage of organic TFTs can be given by

$$V_{TH} = \frac{\Phi_M - \Phi_S}{e} - \frac{1}{C_{OX}} Q = \frac{\Phi_M - \Phi_S}{e} - \frac{d}{\varepsilon} Q, \tag{2.5}$$

where e is the electron elementary charge, Φ_M and Φ_S are the work functions of the gate electrode and the organic semiconductor, respectively, d is the thickness and ε is the dielectric constant of the gate dielectric, respectively, Q is the charge density [9]. Q is written as

$$Q = Q_S + \int_0^d \frac{x}{d} \rho_{OX}(x)\, dx, \tag{2.6}$$

where Q_S is the surface charge density at the interface between the gate dielectric and the semiconductor and ρ_{OX} is the charge density per unit volume in the gate dielectric. The interfaces of the gate dielectric for the gate metal and the semiconductor are defined as $x = 0$

and d, respectively.

In this thesis, Q_S is assumed to be mainly induced by oxygen plasma treatment. The surface charge density Q_S is expressed as

$$Q_S = q_p t_p , \tag{2.7}$$

where q_P is the surface charge density induced by oxygen plasma treatment and t_P is the oxygen plasma treatment time. Although q_P depends on the conditions of plasma treatment, q_P is a constant under certain conditions of plasma treatment except treatment time. Substituting Eqs. (2.6) and (2.7) into Eq. (2.5), the threshold voltage is written as

$$V_{TH} = \frac{\Phi_M - \Phi_S}{e} - \frac{d}{\varepsilon}\left(Q_0 + q_p t_p\right). \tag{2.8}$$

where

$$Q_0 = \int_0^d \frac{x}{d} \rho_{OX}\left(x\right) dx , \tag{2.9}$$

As a result, the threshold voltage changes linearly as a function of d and t_P under the assumption that q_P is a constant.

2.4 References

[1] M. Kitamura, and Y. Arakawa, Appl. Phys. Lett. **89**, 223525 (2006).

[2] D. K. Schroder, Semiconductor Material and Device Characterization, 3rd ed. New York, USA, Wiley.

[3] M. Kitamura, S. Aomori, J. H. Na, and Y. Arakawa, Appl. Phys. Lett. **93**, 03331 (2008).

[4] S. D. Wang, Y. Yan, and K. Tsukagoshi, Appl. Phys. Lett. **97**, 063307 (2010).

[5] U. Kraft, K. Takimiya, M. J. Kang, R. Rödel, F. Letzkus, J. N. Burghartz, E. Weber, and H. Klauk, Org. Electron. **35**, 33 (2016).

[6] P. V. Pesavento, R. J. Chesterfield, C. R. Newman, and C. D. Frisbie, J. Appl. Phys. **96**, 7312 (2004).

[7] K. P. Puntambekar, P. V. Pesavento, and C. D. Frisbie, Appl. Phys. Lett. **83**, 5539 (2003).

[8] M. Kano, T. Minari, and K. Tsukagoshi, Appl. Phys. Lett. **94**, 143304 (2009).

[9] M. Kitamura, and Y. Arakawa, J. Phys.: Condens. Matter **20**, 184011 (2008).

Chapter 3
Operational Stability in Pentacene Thin-Film Transistors with Threshold Voltages Tuned by Oxygen Plasma Treatment

3.1 Introduction

Organic thin-film transistors (TFTs) have been applied to logic circuits [1-4] and addressing devices for active-matrix displays [5-9]. Threshold voltage control for organic TFTs is essential for realizing a circuit design for such applications of organic TFTs. Also, accurate control of the threshold voltage contributes to stable [10], high-speed [11], and low-power [12] operations of circuits.

Some approaches have been attempted to control the threshold voltage in organic TFTs. In one approach, a change in parasitic resistance between a contact electrode and a channel layer is applied [13,14]. In another approach, a self-assembled monolayer (SAM) is prepared on the surface of the gate dielectric [15-17]. However, these approaches affect other characteristics of the TFTs such as field-effect mobility and subthreshold swing. Threshold voltages are also controlled using a double-gate structure [18,19]. Although this approach enables a continuous change in the threshold voltage, it requires the fabrication of an additional electrode in the double-gate structure.

Oxygen plasma [17] and UV ozone treatments [15,20,21] have been used to obtain a hydrophilic surface for formation of a SAM on a gate dielectric. Since the threshold voltage in organic TFTs depends on fixed charges on the surface of and inside the gate dielectric, oxygen

plasma and UV ozone treatments to the surface of the gate dielectric may possibly affect the threshold voltage. In fact, the effects of oxygen plasma [22-24] and UV ozone [25,26] treatments on threshold voltages have been reported. Thus, oxygen plasma or UV ozone treatment has potentials in the accurate control of the threshold voltage in organic TFTs suitable for practical use [27].

The stability of the characteristics of organic TFTs under operation is also an important issue for their practical applications. Thus, some groups have intensively investigated the change in the threshold voltage in organic TFTs as a function of bias stress time and bias voltage [28-34]. Since the stability of the threshold voltage in organic TFTs is strongly related to condition of the gate dielectric, investigation of the stability in organic TFTs with controlled threshold voltage is demanded.

In this chapter, we report the characteristics of pentacene-based TFTs with a SiO_2 gate dielectric treated with oxygen plasma. In particular, the dependence of the threshold voltage in the TFTs on treatment time is examined. The threshold voltage after gate bias stress is also shown to evaluate the stability of the threshold voltage change induced by plasma treatment.

3.2 Experimental methods

A cross section of the pentacene TFT examined in this chapter in shown in Fig. 3.1(a). The pentacene TFT was fabricated on a highly doped n-type Si substrate with thermally grown SiO_2 serving as the gate dielectric. Silicon substrates with various SiO_2 thickness were used to examine the characteristics of pentacene TFTs on the basis of Eq. (2.5). The SiO_2 thickness, d, are 35, 90, 300, and 500 nm, which provide unit area capacitances of 92.0, 36.9, 11.3, and 6.61 nF/cm^2, respectively. The SiO_2 surface was treated using an oxygen plasma equipment (SAKIGAKE-Semiconductor YHS-GNS), an illustration of which is shown in Fig. 3.1(b). The oxygen flow rate was fixed at 100 mL/min. The AC power for plasma generation, p_{AC}, which

is controllable in the range of less than or equal to 50 W, was adjusted by monitoring the emission intensity of the plasma. The AC power was set at 5.8 W as a standard power in this chapter. Although the power 0f 5.8 W seems to be slightly low, this power is sufficient to affect the characteristics of TFTs. This is because the vacuum chamber and the electrode of the equipment are not large, as shown in Fig. 3.1(b). The treatment time t_p was set in the range between 5 and 900 s. After the oxygen plasma treatment, the substrate was immediately exposed to hexamethyldisilazane (HMDS) vapor to obtain a hydrophobic surface. A 45-nm-thick pentacene layer was then deposited on the SiO_2 dielectric at room temperature through a shadow mask. The deposition rate was 1.2 nm/min. Finally, a 45-nm-thick Au layer was deposited through another shadow mask to define the drain and source electrodes. The channel width was 1 mm, and the channel length (L) was 80 or 100 μm. Since pentacene TFTs with L = 100 μm were mainly investigated, the channel length of TFTs not specified in this manuscript is 100 μm. The current–voltage characteristics of pentacene TFTs were measured in a dry-nitrogen glovebox at room temperature using a semiconductor parameter analyzer.

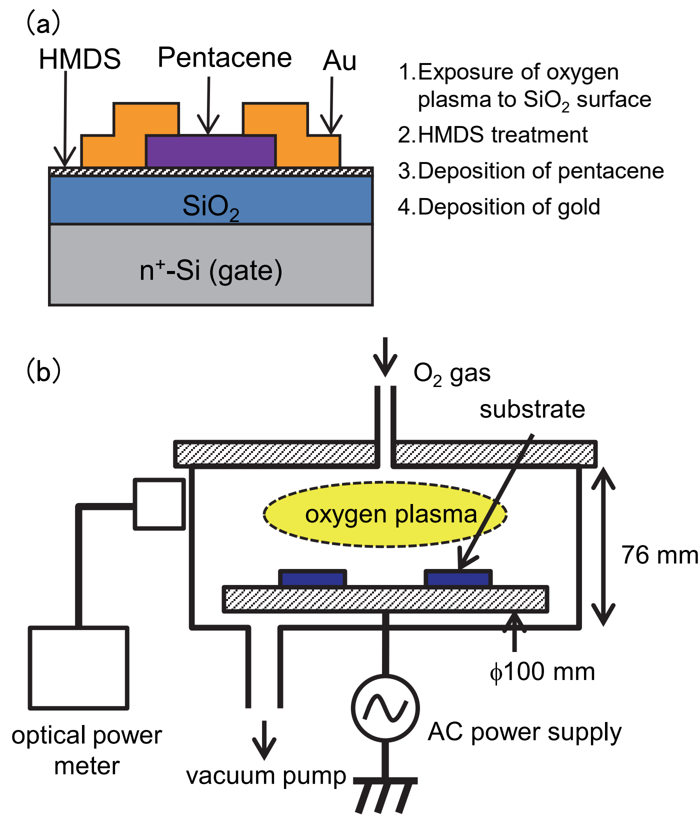


Figure 3.1: (a) Cross section of fabricated pentacene-based TFT and the fabrication process. (b) Illustration of oxygen plasma equipment used for surface treatment of SiO_2 gate dielectric.

3.3 Results and discussion

Figure 3.2(a) shows the drain current (I_D) versus gate voltage (V_G) characteristics at a drain voltage (V_D) of −20 V of pentacene TFTs with 90-nm-thick SiO_2 layers treated with oxygen plasma. The plasma treatment times, t_p, were 5, 10, 30, 60, and 120 s. The transfer curves in Fig. 3.2(a) shift to positive gate voltages with increase in plasma treatment time. The slopes of $|I_D|^{1/2}–V_G$ curves, the subthreshold swing, and the off current are almost the same for all TFTs. The results indicate that the oxygen plasma treatment with the treatment time affects only the threshold voltages. The threshold voltage, V_{TH}, and the field-effect mobility in the saturation

regime, μ_{sat}, of pentacene TFTs with different SiO_2 thickness are shown as a function of t_p in Figs. 3.2(b) and 3.2(c), respectively. The V_{TH} and μ_{sat} values were estimated by fitting a line to the $|I_D|^{1/2}$–V_G curves in the saturation regime. For the measurement of pentacene TFTs with d = 35, 90, 300, and 500 nm in the saturation regime, the drain voltages were set at −10, −20, −60, and −100 V, respectively. The threshold voltage is in the range from −15 to 36 V. The V_{TH} for each SiO_2 thickness increases linearly with t_p. This is consistent with Eq. (2.8). The slopes of V_{TH} versus t_p for d = 35, 90, 300, and 500 nm are 0.027, 0.061, 0.27, and 0.45 V/s, respectively. The slope increases with SiO_2 thickness. The dependence of the slope on SiO_2 thickness is also consistent with Eq. (2.8). On the other hand, it seems that μ_{sat} is independent of treatment time, as seen from Fig. 3.2(c). μ_{sat} is in the range of 0.57 to 0.85 $cm^2/(V\ s)$ and the average is 0.73 $cm^2/(V\ s)$. The results shown in Figs. 3.2(b) and 3.2(c) suggest that the threshold voltage can be controlled without large change in mobility.

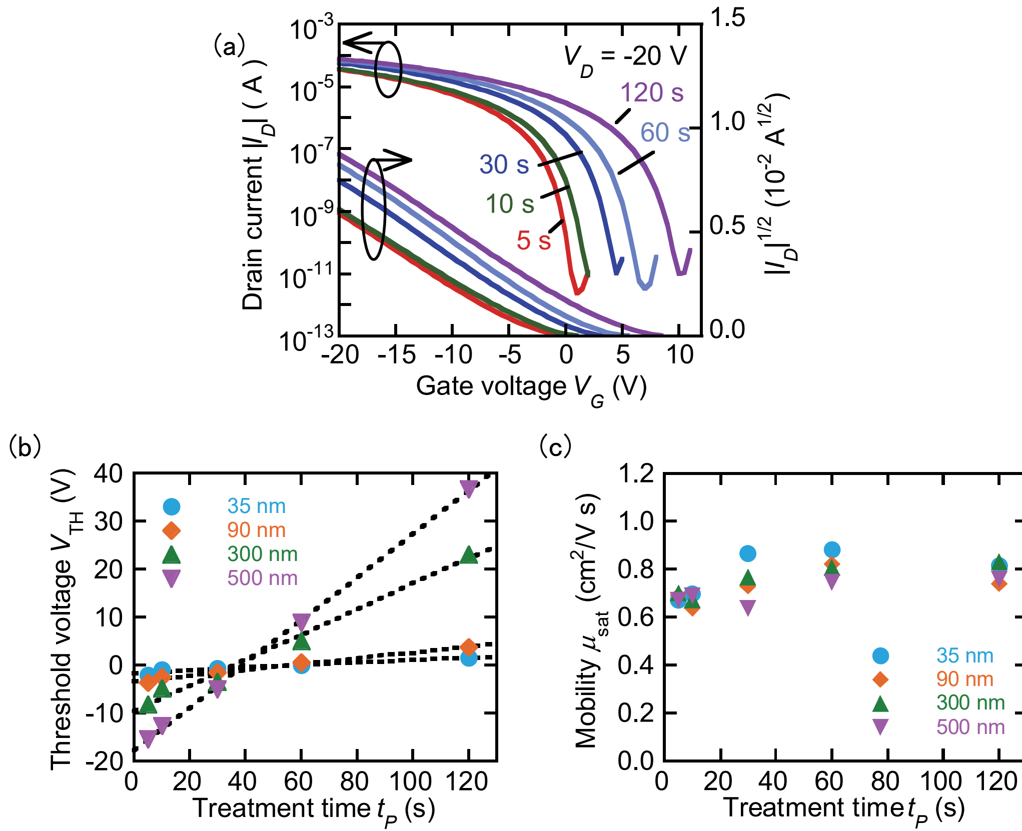


Figure 3.2: (a) Transfer characteristics of pentacene TFTs with 90-nm-thick SiO_2 with oxygen plasma treatment times between 5 and 120 s. (b) Threshold voltage and (c) mobilities in the saturation regime of TFTs with 35-, 90-, 300-, and 500-nm thick SiO_2 as a function of treatment time.

To estimate the surface charge density Q_S, the threshold voltage is plotted as a function of SiO_2 thickness in Fig. 3.3(a). The slope of the fitting line for treatment time in Fig. 3.3(a) corresponds to the surface charge for treatment time. Figure 3.3(b) shows the surface charge density estimated from Fig. 3.3(a). On the basis of Eqs. (2.6), (2.7), and (2.9), the intrinsic surface charge density Q_0 and the surface charge density induced by plasma treatment, q_p, are estimated to be 113 nC/cm^2 and −3.1 nC/(cm^2 s), respectively. The Q_0 value of 113 nC/cm^2 corresponds to the charge site density of about 7×10^{11} cm^{-2}. Although the reason for the intrinsic surface charge is under investigation, sites not terminated with HMDS and/or dopants

in the highly doped silicon may be related to the positive surface charge. On the other hand, the negative value of q_P indicates that oxygen plasma treatment generates electron trapping sites on and/or near the SiO_2 surface. In addition, the result of threshold voltage shift suggests that electrons captured at the trapping sites work as negative fixed charges even after the surface is treated with HMDS.

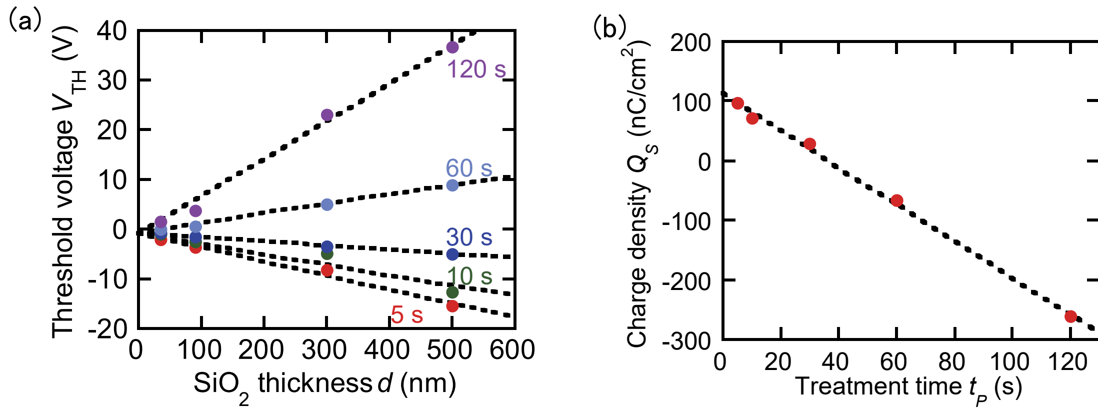


Figure 3.3: (a) Threshold voltages of pentacene TFTs with gate dielectrics plasma-treated for 5, 10, 30, 60, and 120 s as a function of SiO_2 thickness. (b) Surface charge density estimation from the threshold voltage in (a) as a function of treatment time.

The effect of long plasma treatment on the transistor characteristics was examined to investigate the limitation of the threshold voltage changes. Figure 3.4(a) shows the $|I_D|$–V_G and $|I_D|^{1/2}$–V_G characteristics of TFTs with 90-nm-thick SiO_2 layers treated with oxygen plasma for t_P between 5 and 900 s. The transfer curves in forward and reverse sweeps are shown with solid and dashed lines, respectively. For the treatment times of 5, 60, and 180 s, the transfer curve in reverse sweep almost traces the curve in forward sweep. On the other hand, the long plasma treatments for t_P = 300 and 900 s lead to hysteresis I the transfer curves. This indicates that long plasma treatments lead to an increase in shallow trap density. Figures 3.4(b) and 3.4(c) respectively show the threshold voltage and mobility in the saturation regime of TFTs with d =

90 and 300 nm. The values were estimated from the transfer curves in forward sweep. The dashed line in Fig. 3.4(b) for each d is the same as the fitted line in Fig. 3.2(b). The difference between the dashed line and the plot increases with t_p. This indicates that the surface charge density induced by plasma treatment does not increase linearly with treatment time. This means that q_p is not constant with respective to t_p and decreases with an increase in t_p. On the other hand, the mobilities for long treatment times between 180 and 900 s are lower than those for t_p between 5 and 120 s. As a result, plasma treatment for t_p longer than 120 s leads to decreases in mobility and hysteresis in transfer curves.

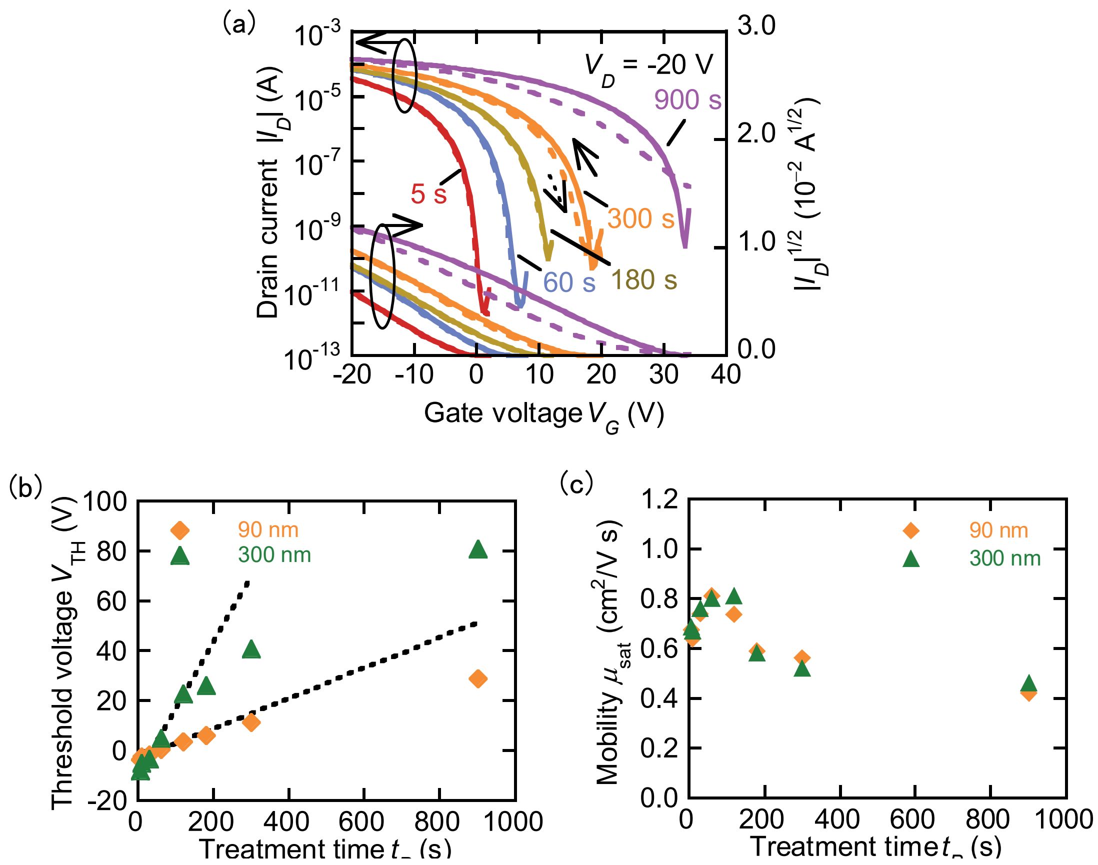


Figure 3.4: (a) Transfer characteristics of pentacene TFTs with 90-nm-thick SiO_2 with oxygen plasma treatment times between 5 and 900 s. (b) Threshold voltage and (c) mobilities in the saturation regime of TFTs with 90- and 300-nm-thick SiO_2 as functions of treatment time.

The dependence of AC power on the transfer characteristics was also investigated. Figures 3.5(a) and 3.5(b) show the transfer characteristics and mobility in the saturation regime of pentacene TFTs with 90-nm-thick SiO_2 layers treated with oxygen plasma for 60 s. The AC power p_{AC} was set in the range between 3.8 and 38 W. The increase in p_{AC} leads to positive shift in the threshold voltage. However, a high AC power causes hysteresis in the transfer curves as well as long treatment time.

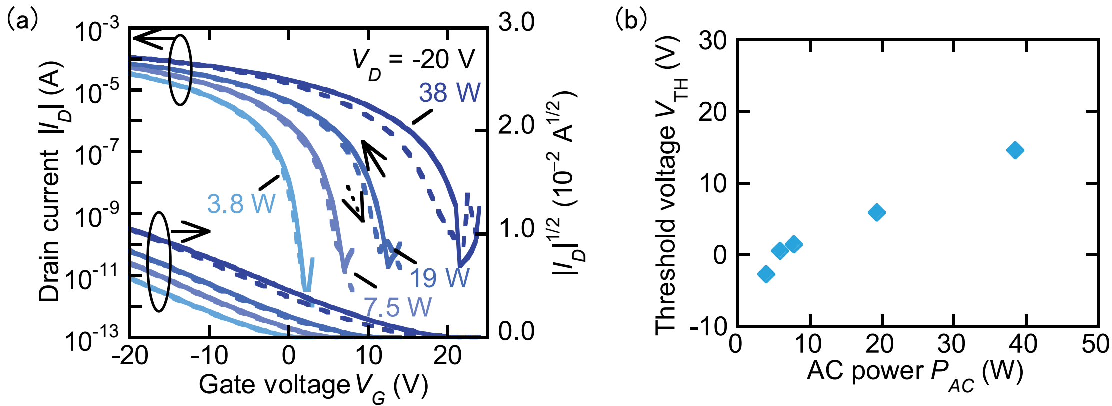


Figure 3.5: (a) Transfer characteristics of pentacene TFTs with 90-nm-thick SiO_2 treated with oxygen plasma at AC power from 3.8 to 38 W. (b) Threshold voltages of TFTs with 90-nm-thick SiO_2 as a function of AC power.

To evaluate the stability of threshold voltage change, the effect of gate bias stress on the transfer characteristics was investigated. The voltage of gate bias, V_{GB}, was set in the range of −50 to 50 V, and the drain voltage was fixed at 0 V. The stress time t_s was in the range from 0 to 5000 s. Figures 3.6(a) and 3.6(b) show the threshold voltage and mobility in the saturation regime of the TFTs with L = 80 μm for different t_p after applying bias at V_{GB} = −20 V as a function of t_s, respectively. The V_{TH} for each TFT decreases with increase in t_s. The threshold voltage shifts during stress are 1.6 V for t_p = 10 s, 1.7 V for t_p = 120 s, and 2.3 V for t_p = 300 s. The threshold voltage does not depend strongly on t_p. This indicates that a relative threshold

voltage among different t_p is maintained during gate bias stress. This suggests that the negative bias stress does not affect the negative charge induced by plasma treatment. Although the threshold voltage shift between 1.6 and 2.3 V induced by gate bias stress is slightly larger than that of a pentacene TFT with a polymer gate dielectric [32], the shift is not as large as those other organic TFTs [28,30,35,36], amorphous Si TFTs [37-39] and oxide TFTs [40-42].

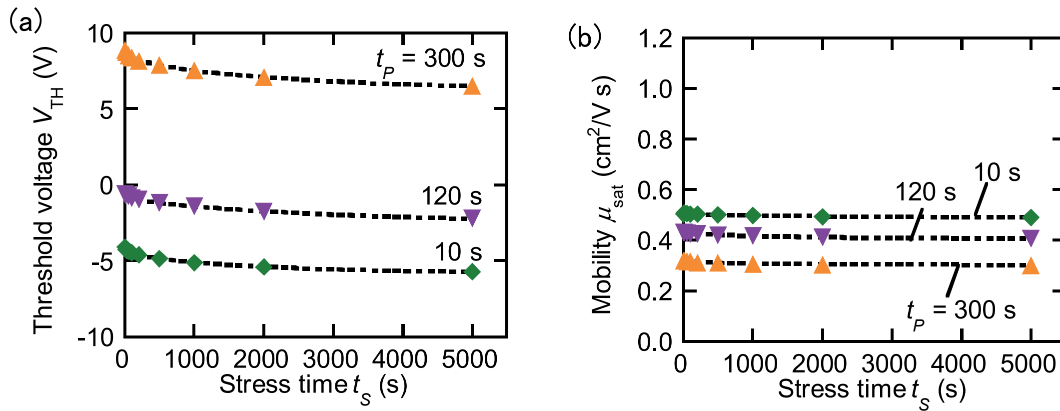


Figure 3.6: (a) Threshold voltages and (b) mobilities in the saturation regime of three TFTs with 90-nm-thick SiO_2 plasma treated for 10, 120, and 300 s as a function of bias stress time. The gate bias and drain voltage are −20 and 0 V, respectively.

Figure 3.7(a) shows the transfer characteristics of a TFT with a 90-nm-thick SiO_2 dielectric treated with p_{AC} = 3.8 W and t_p = 60 s measured after applying bias at V_{GB} = 0, −10, . . . , −50 V, and 10, . . . , 50 V for t_s = 60 s. The measurement for positive bias was conducted about one day after the negative bias examination. The threshold voltage and the mobility in the saturation regime estimated from the transfer characteristics are shown in Fig. 3.7(b) and 3.7(c), respectively. The threshold voltage changes in accordance with the bias stress, although the mobility is almost independent of the bias stress. The negative bias stress induces negative shift in the threshold voltage, which decreases non linearly with decrease in V_{GB}. Although the bias stress at V_{GB} less than −20 V induces a threshold voltage shift greater than 1 V, the threshold

voltage shift under a agate bias stress in the range of 0 to −20 V is as small as 0.4 V. The small shift in the threshold voltage contributes to stable operation. In contrast, the positive bias stress induces positive shift in the threshold voltage, which increases linearly with increase in V_{GB}. In addition, the V_{TH} value at $V_{GB} = 0$ for positive bias stress is close to that at $V_{GB} = 0$ for the negative bias. Since the transfer characteristics for the positive bias stress were measured about one day after the measurement of the negative bias stress, the recovery of the V_{TH} implies that storage under no operation extinguishes the effect of the bias stress. This means that the threshold voltage shift induced by the bias stress is a temporary effect. Since the V_{TH} value at $V_{GB} = 0$ for the positive bias stress is close to that at $V_{GB} = 0$ for negative bias, the V_{TH} value obtained after oxygen plasma treatment is more stable. In fact, it is confirmed that relative threshold voltage among different t_p is maintained for more than one month at least. This is probably because the oxygen plasma treatment generates electron trapping sites at deep levels in the SiO_2 gate dielectric.

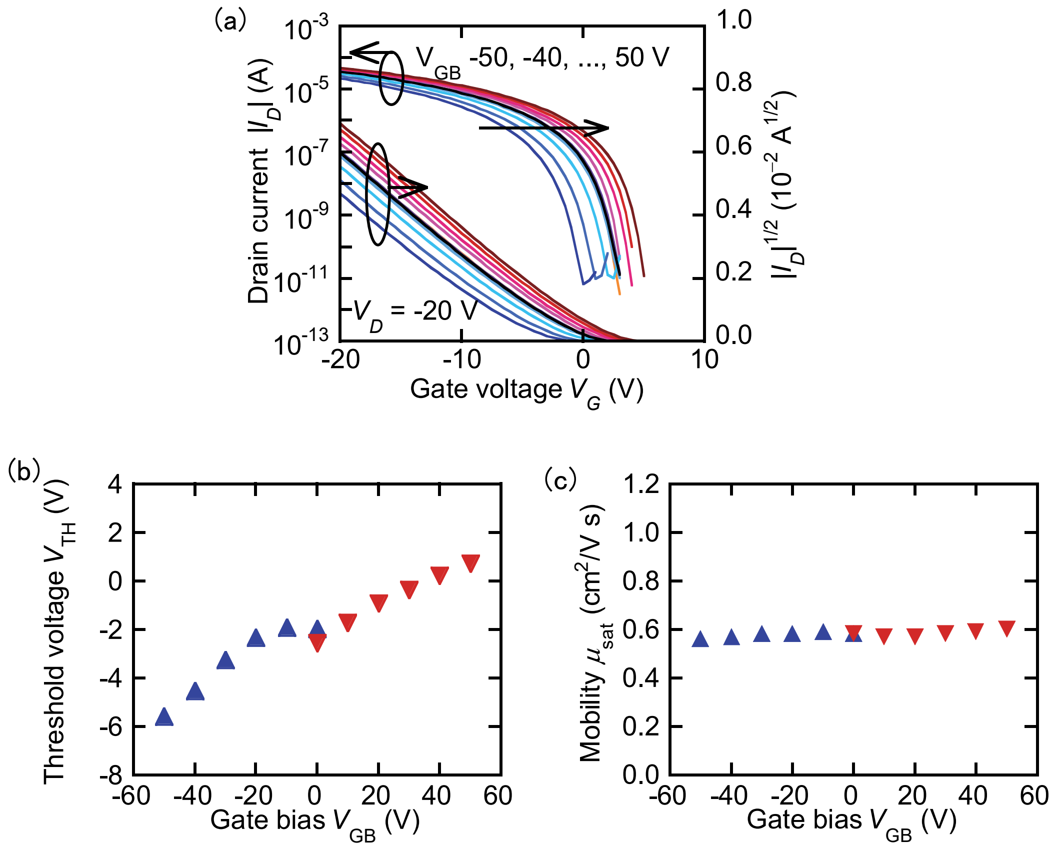


Figure 3.7: (a) Transfer characteristics of a pentacene TFT with L = 80 μm and 90-nm-thick SiO_2 plasma-treated at a AC power of 3.8 W for t_p = 60 s after bias stresses of V_{GB} = 0 (black line), −10 to −50, and 10 to 50 V were applied to the TFT for t_s = 60 s. (b) Threshold voltages and (c) mobilities in the saturation regime of the TFT estimated from the drain current versus gate voltage characteristics in (a).

Point defects in SiO_2 have been experimentally and theoretically studied in the fields of electronics and optics [43-46]. Many types of point defects have been reported, including ≡Si–Si≡, =Si–H, ≡Si–O–O–Si≡, ≡Si–O–O•, ≡Si–O•, and ≡Si–O–H. Here, "≡" and "=" denote, respectively, three and two network Si–O bonds, and "•" represents an unpaired electron. Perfect SiO_2 has a bandgap energy of about 9 eV [43] and the point defect generates an energy level within the bandgap. Pacchioni and Ierano have examined defect energy levels in SiO_2 [44]. Since oxygen plasma treatment was used for surface treatment in this study, we focus on O-

related defects. Figure 3.8 shows a schematic illustration of the defect energy levels for ≡Si–O–O–Si≡, ≡Si–O–O•, ≡Si–O•, and ≡Si–O–H. The energy level of the highest occupied molecular orbital (HOMO) of pentacene [47] is also shown. The ≡Si–O–O• and ≡Si–O• defects having an unpaired electron would act as electron traps, whereas the ≡Si–O–H and ≡Si–O–O–Si≡ defects would not [45]. It is possible that oxygen atoms incorporated into SiO_2 form ≡Si–O–O–Si≡, ≡Si–O–O•, and ≡Si–O• defects [46]. In oxygen plasma treatment, oxygen ions accelerate to the surface of a substrate. Thus, oxygen plasma treatment would generate ≡Si–O–O•, and ≡Si–O• defects that act as electron traps. This is a conceivable reason why the oxygen plasma treatment induces threshold voltage change.

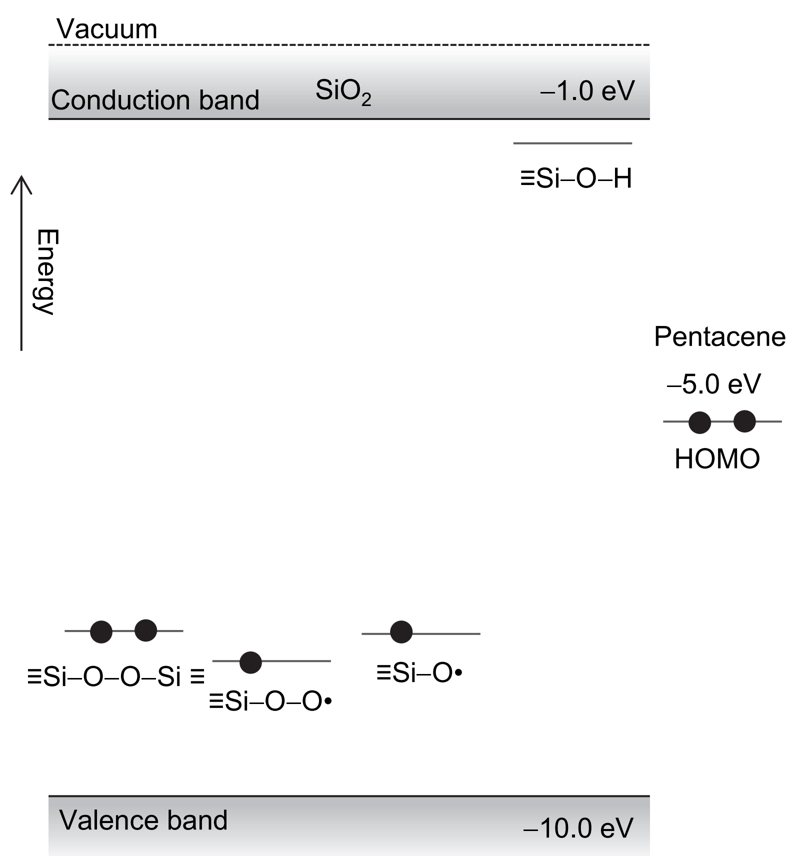


Figure 3.8: Schematic illustration of energy levels for various defects in SiO_2 and the HOMO level of pentacene.

3.4 Summary

We investigated the effect of oxygen plasma treatment of the SiO_2 gate dielectric on the characteristics of pentacene TFTs. The plasma treatment for less than 120 s enables the control of the threshold voltage without a large change in the mobility. The threshold voltage shift, which is proportional to the treatment time, can be explained by supposing that the plasma treatment induces negative charges on and/or near to the gate dielectric surface. Also, we investigated the effect of gate bias stress on the TFT characteristics. The gate bias stress did not extinguish the threshold voltage change induced by plasma treatment. The threshold voltage shift in the TFT induced by gate bias stress was as small as about 2 V. The information on the threshold voltage shift and stability obtained in this study is useful for the application of organic TFTs to integrated circuits.

3.5 References

[1] P. F. Baude, D. A. Ender, M. A. Haase, T. W. Kelley, D. V. Muyres, and S. D. Theiss, Appl. Phys. Lett. **82**, 3964 (2003).

[2] D. Bode, K. Myny, B. Verreet, B. van der Putten, P. Bakalov, S. Steudel, S. Smout, P. Vicca, J. Genoe, and P. Heremans, Appl. Phys. Lett. **96**, 133307 (2010).

[3] M. Kitamura, Y. Kuzumoto, S. Aomori, and Y. Arakawa, Appl. Phys. Express **4**, 051601 (2011).

[4] K.-J. Baeg, S.-W. Jung, D. Khim, J. Kim, D.-Y. Kim, J. B. Koo, J. R. Quinn, A. Facchetti, I.-K. You, and Y.-Y. Noh, Org. Electron. **14**, 1407 (2013).

[5] P. Mach, S. J. Rodriguez, R. Nortrup, P. Wiltzius, and J. A. Rogers, Appl. Phys. Lett. **78**, 3592 (2001).

[6] C. D. Sheraw, L. Zhou, J. R. Huang, D. J. Gundlach, and T. N. Jackson, Appl. Phys. Lett. **80**, 1088 (2002).

[7] M. Kitamura, T. Imada, and Y. Arakawa, Jpn. J. Appl. Phys. **42**, 2483 (2003).

[8] L. Zhou, S. Park, B. Bai, J. Sun, S.-C. Wu, T. N. Jackson, S. Nelson, D. Freeman, and Y. Hong, IEEE Electron Device Lett. **26**, 640 (2005).

[9] S. C. Lim, S. H. Kim, H. Y. Chu, J. H. Lee, J.-I. Lee, J. Y. Oh, D. Kim, and T. Zyung, Synth. Met. **151**, 197 (2005).

[10] G. H. Gelinck, H. E. A. Huitema, E. van Veenendaal, E. Cantatore, L. Schrijnemakers, J. B. P. H. van der Putten, T. C. T. Geuns, M. Beenhakkers, J. B. Giesbers, B.-H. Huisman, E. J. Meijer, E. M. Benito, F. J. Touwslager, A. W. Marsman, B. J. E. van Rens, and D. M. de Leeuw, Nat. Mater. **3**, 106 (2004).

[11] M. Kitamura and Y. Arakawa, Jpn. J. Appl. Phys. **50**, 01BC01 (2011).

[12] L. Shang, Z. Ji, H. Wang, Y. Chen, C. Lu, X. Liu, M. Han, and M. Liu, IEEE Tran. Electron Devices **58**, 2127 (2011).

[13] R. Schroeder, L. A. Majewski, and M. Grell, Appl. Phys. Lett. **83**, 3201 (2003).

[14] M. Kitamura, Y. Kuzumoto, S. Aomori, M. Kamura, J. H. Na, and Y. Arakawa, Appl. Phys. Lett. **94**, 083310 (2009).

[15] S. Kobayashi, T. Nishikawa, T. Takenobu, S. Mori, T. Shimoda, T. Mitani, H. Shimotani, N. Yoshimoto, S. Ogawa, and Y. Iwasa, Nat. Mater. **3**, 317 (2004).

[16] K. P. Pernstich, S. Haas, D. Oberhoff, C. Goldmann, D. J. Gundlach, B. Batlogg, A. N. Rashid, and G. Schitter, J. Appl. Phys. **96**, 6431 (2004).

[17] S. C. Lim, S. H. Kim, J. H. Lee, M. K. Kim, D. J. Kim, and T. Zyung, Synth. Met. **148**, 75 (2005).

[18] S. Iba, T. Sekitani, Y. Kato, T. Someya, H. Kawaguchi, M. Takamiya, T. Sakurai, and S. Takagi, Appl. Phys. Lett. **87**, 023509 (2005).

[19] K. Hizu, T. Sekitani, T. Someya, and J. Otsuki, Appl. Phys. Lett. **90**, 093504 (2007).

[20] M. Kitamura, Y. Kuzumoto, M. Kamura, S. Aomori, J. H. Na, and Y. Arakawa, Phys. Status Solidi C **5**, 3181 (2008).

[21] Y. Ito, A. A. Virkar, S. Mannsfeld, J. H. Oh, M. Toney, J. Locklin, and Z. Bao, J. Am. Chem. Soc. **131**, 9396 (2009).

[22] M. W. Lee and C. K. Song, Jpn. J. Appl. Phys. **42**, 4218 (2003).

[23] A. Wang, I. Kymissis, V. Bulović, and A. I. Akinwande, IEEE Trans. Electron Devices **53**, 9 (2006).

[24] K. Fukuda, T. Sekitani, U. Zschieschang, H. Klauk, K. Kuribara, T. Yokota,T. Sugino, K. Asaka, M. Ikeda, H. Kuwabara, T. Yamamoto, K. Takimiya, T. Fukushima, T. Aida, M. Takamiya, T. Sakurai, and T. Someya, Adv. Funct. Mater. **21**, 4019 (2011).

[25] A. Wang, I. Kymissis, V. Bulović, and A. I. Akinwande, Appl. Phys. Lett. **89**, 112109 (2006).

[26] D. Guo, S. Entani, S. Ikeda, and K. Saiki, Chem. Phys. Lett. **429**, 124 (2006).

[27] Y. Kimura, M. Kitamura, and Y. Arakawa, Ext. Abstr. Solid State Devices and Materials, 2014, p. 926.

[28] S. J. Zilker, C. Detcheverry, E. Cantatore, and D. M. de Leeuw, Appl. Phys. Lett. **79**, 1124 (2001).

[29] T. Sekitani, S. Iba, Y. Kato, Y. Noguchi, T. Someya, and T. Sakurai, Appl. Phys. Lett. **87**, 073505 (2005).

[30] J. B. Chang and V. Subramanian, Appl. Phys. Lett. **88**, 233513 (2006).

[31] D. K. Hwang, K. Lee, J. H. Kim, S. Im, J. H. Park, and E. Kim, Appl. Phys. Lett. **89**, 093507 (2006).

[32] T. Umeda, D. Kumaki, and S. Tokito, Org. Electron. **9**, 545 (2008).

[33] K. Fukuda, T. Hamamoto, T. Yokota, T. Sekitani, U. Zschieschang, H. Klauk, and T. Someya, Appl. Phys. Lett. **95**, 203301 (2009).

[34] U. Zschieschang, R. T. Weitz, K. Kern, and H. Klauk, Appl. Phys. A **95**, 139 (2009).

[35] D. Knipp, R. A. Street, A. Völkel, and J. Ho, J. Appl. Phys. **93**, 347 (2003).

[36] A. Salleo, F. Endicott, and R. A. Street, Appl. Phys. Lett. **86**, 263505 (2005).

[37] M. J. Powell, Appl. Phys. Lett. **43**, 597 (1983).

[38] F. R. Libsch and J. Kanicki, Appl. Phys. Lett. **62**, 1286 (1993).

[39] C.-H. Lee, D. Striakhilev, and A. Nathan, IEEE Tran. Electron Devices **54**, 45 (2007).

[40] J.-S. Park, K. Kim, Y.-G. Park, Y.-G. Mo, H. D. Kim, and J. K. Jeong, Adv. Mater. **21**, 329 (2009).

[41] M. E. Lopes, H. L. Gomes, M. C. R. Medeiros, P. Barquinha, L. Pereira, E. Fortunato, R. Martins, and I. Ferreira, Appl. Phys. Lett. **95**, 063502 (2009).

[42] J. S. Park, W.-J. Maeng, H.-S. Kim, and J.-S. Park, Thin Solid Films **520**, 1679 (2012).

[43] T. H. DiStefano and D. E. Eastman, Solid State Commun. **9**, 2259 (1971).

[44] G. Pacchioni and G. Ierano, Phys. Rev. B **57**, 818 (1998).

[45] V. A. Gritsenko, A. V. Shaposhnikov, Yu. N. Novikov, A. P. Baraban, Hei Wong, G. M. Zhidomirov, and M. Roger, Microelectron. Reliab. **43**, 665 (2003).

[46] K. Kajihara, T. Miura, H. Kamioka, A. Aiba, M. Uramoto, Y. Morimoto, M. Hirano, L. Skuja, and H. Hosono, J. Non-Cryst. Solids **354**, 224 (2008).

[47] S. J. Kang, Y. Yi, C. Y. Kim, S. W. Cho, M. Noh, K. Jeong, and C. N. Whang, Synth. Met. **156**, 32 (2006).

Chapter 4
Energy Distribution of Interface States Generated by Oxygen Plasma Treatment

4.1 Introduction

Organic thin-film transistors (TFTs) have attracted considerable attention because of their potential applications to large-area, mechanically flexible, light-weight, and cost-effective devices [1-3]. In addition to the advantage, field-effect mobilities in organic TFTs have reached to about 10 $cm^2/(V\ s)$ [5-8], Which is close to those of oxide TFTs practically used in flat panel displays. For practical application, threshold voltage control in organic TFTs is an important issue as well as improvement of the performance. Some groups have been attempting threshold voltage control in organic TFTs using various methods such as using self-assembled monolayers (SAM) on a gate dielectric [9-12], utilizing new polymer gate dielectrics [13,14], doping into organic layers [15-17], choosing gate metals [18,19], adjusting parasitic resistance [20,21], and using multi gate structures [22].

Another approach of threshold voltage control utilized oxygen plasma treatment to the surface of gate dielectrics [23-25]. Oxygen plasma treatment has been used to obtain a hydrophilic surface for formation of a SAM on a gate dielectric [26,27]. Thus, the threshold voltage control by oxygen plasma treatment does not require an additional process if the organic TFT requires a SAM layer. In addition, the threshold voltage gradually changes with plasma treatment time. The continuous change is suitable for application to integrated circuits of organic TFTs. In actual, we applied pentacene TFTs with the controlled threshold voltage to

logic circuits [28,29]. Since the threshold voltage shifts to positive gate voltage with plasma treatment time, the threshold voltage change in probably attributed to electrons captured at interface states generated by oxygen plasma treatment. Although a concern is that the change is temporary, we described that gate bias stress does not negate the threshold voltage change provided by oxygen plasma treatment in chapter 3. This implies that the interface states work as deep traps for electrons. On the other hand, the presence of shallow traps has been unclear.

For Si metal-oxide-semiconductor (MOS) field-effect transistors (FET), electron states at the interface between semiconductors and gate dielectric have been examined using some methods including electron spin resonance spectroscopy [30], current−voltage measurements [31], and capacitance−voltage ($C-V$) measurements [32,33]. Among the method, $C-V$ measurement has an advantage that the measurement is performed without light irradiation and elevated temperature. Since organic TFTs are generally sensitive to light and temperature change, $C-V$ measurement is suitable for evaluation of organic TFTs and MOS capacitors. In actual, interface traps in organic MOS capacitors have been investigated by $C-V$ measurement [34-36].

In this chapter, we report $C-V$ characteristics of pentacene MOS capacitors with a SiO_2 gate dielectric treated with oxygen plasma to examine the energy distribution of interface states generated by the treatment. First, we show current−voltage characteristics of pentacene TFTs to compare the characteristics of those of the MOS capacitors. Then, $C-V$ characteristics of the MOS capacitors are shown. The energy distribution of the interface states is calculated from the $C-V$ characteristics.

4.2 Analytical methods

4.2.1 Characteristics of MOS capacitors

Figure 4.1 shows schematic band diagram of a SiO_2/pentacene MOS capacitor examined in this study, we attempt to estimate the interface state density by $C-V$ measurement. The total

capacitance per unit area of MOS capacitor (C_G) is expressed as

$$\frac{1}{C_{\mathrm{G}}}=\frac{1}{C_{\mathrm{OX}}}+\frac{1}{C_{\mathrm{S}}}, \tag{4.1}$$

where C_S is the capacitance per unit area of the pentacene layer. The capacitances C_G and C_S are functions of the gate voltage (V_G) and are represented as $C_G(V_G)$ and $C_S(V_G)$. The interface state density in experimentally classified into three groups denoted as D_L, D_M, and D_H. The D_L, D_M, and D_H are expected to be roughly distributed in ascending order shown in Fig. 4.1. Because the fixed charge in the gate dielectric is expect to be positive, it is represented by a plus sign.

Flat band voltage (V_{FB}) of a MOS capacitor without inversion mode is equal to threshold voltage (V_{TH}) of a transistor as described in chapter 2, and is written as

$$V_{\mathrm{FB}}=\frac{\Phi_{\mathrm{M}}-\Phi_{\mathrm{S}}}{e}-\frac{Q}{C_{\mathrm{OX}}}, \tag{4.2}$$

where e is the electron elementary charge, Φ_M and Φ_S are the work functions of the gate electrode and the organic semiconductor, respectively. When a V_{FB} value is experimentally obtained, Q is calculated from Eq. (4.2) as well as the charge density Q in Eq. (2.5). Also, the V_{FB} value is used in an equation for surface potential shown below. An issue is how to determine V_{FB} experimentally. In this study, the V_{FB} value is experimentally determined as

$$C_{\mathrm{S}}(V_{\mathrm{FB}})=20\min\left[C_{\mathrm{S}}\left(V_{\mathrm{G}}\right)\right]. \tag{4.3}$$

Although this definition is not standard, Eq. (4.3) for a MOS capacitor provides a V_{FB} value close to a V_{TH} value obtained from the current characteristics of a TFT prepared under the same condition as that of the MOS capacitor. Physically, Eq. (4.3) means that one twentieth thickness of a pentacene layer acts as insulator. In this study, the average thickness of a pentacene is about 22.5 nm as explained later. Thus, the one twentieth thickness is about 1.1 nm.

4.2.2 Interface states of MOS capacitors

The interface state density D_{it} in an evaluated MOS capacitor is generally obtained as a function of the surface potential at the interface between the semiconductor and the gate dielectric. The surface potential Ψ_{S} is expressed as [37,38]

$$\Psi_{\mathrm{S}}\left(V_{\mathrm{G}}\right)=V_{\mathrm{G}}-V_{\mathrm{FB}}-\int_{V_{\mathrm{FB}}}^{V_{\mathrm{G}}}\left(\frac{C_{\mathrm{G}}\left(V\right)}{C_{\mathrm{OX}}}\right)dV \tag{4.4}$$

as a function of V_{G} and is constructed by using V_{FB} and $C_{\mathrm{G}}(V_{\mathrm{G}})$. The calculation of D_{it} requires the C−V characteristic of a MOS capacitor, which ideally has no interface state, as a reference. Here, the surface potential and the total capacitance of the reference MOS capacitor are denoted as $\Psi_{\mathrm{ref}}(V_{\mathrm{G}})$ and $C_{\mathrm{ref}}(V_{\mathrm{G}})$, respectively. Using these notations, the interface state density (D_{it}) can be calculated from

$$D_{\mathrm{it}}\left(\Psi_{\mathrm{S}}\left(V_{\mathrm{G}}\right)\right)=\lim_{\Delta V_{\mathrm{G}}\to 0}\frac{1}{e^{2}}\frac{\Delta Q_{\mathrm{G}}-\Delta Q_{\mathrm{ref}}}{\Psi_{\mathrm{S}}\left(V_{\mathrm{G}}+\Delta V_{\mathrm{G}}\right)-\Psi_{\mathrm{S}}\left(V_{\mathrm{G}}\right)} \tag{4.5}$$

where

$$\Delta Q_{\mathrm{G}}=\int_{V_{\mathrm{G}}}^{V_{\mathrm{G}}+\Delta V_{\mathrm{G}}}C_{\mathrm{G}}\left(V\right)dV \tag{4.6a}$$

$$\Delta Q_{\mathrm{ref}}=\int_{V_{\mathrm{G}}'}^{V_{\mathrm{G}}'+\Delta V_{\mathrm{G}}'}C_{\mathrm{ref}}\left(V\right)dV \tag{4.6b}$$

The V_{G}' and $\Delta V_{\mathrm{G}}'$ are defined as the following equations:

$$\Psi_{\mathrm{ref}}\left(V_{\mathrm{G}}'\right)=\Psi_{\mathrm{S}}\left(V_{\mathrm{G}}\right), \tag{4.7a}$$

$$\Psi_{\mathrm{ref}}\left(V_{\mathrm{G}}'+\Delta V_{\mathrm{G}}'\right)=\Psi_{\mathrm{S}}\left(V_{\mathrm{G}}+\Delta V_{\mathrm{G}}'\right). \tag{4.7b}$$

The ΔQ_{G} and ΔQ_{ref} are charges stored in the evaluated and reference MOS capacitors, respectively, when the surface potential changes from $\Psi_{\mathrm{S}}(V_{\mathrm{G}})$ to $\Psi_{\mathrm{S}}(V_{\mathrm{G}}+\Delta V_{\mathrm{G}})$.

Equation (4.5) is mathematically equivalent to

$$D_{\mathrm{it}}\left(\Psi_{\mathrm{S}}\right)=\frac{C_{\mathrm{OX}}}{e^{2}}\frac{d\left(V_{\mathrm{G}}-V_{\mathrm{G}}'\right)}{d\Psi} \tag{4.8}$$

known as Terman method [38-40]. A calculated D_{it} value generally contains numerical errors. Thus, a value calculated from Eq. (4.5) may be slightly different from that calculated fro Eq. (4.8). In this study, we use Eq. (4.5) for calculation of D_{it}. This is because the increases in accumulated charges ΔQ_G, ΔQ_{ref} can be seen in the calculation process.

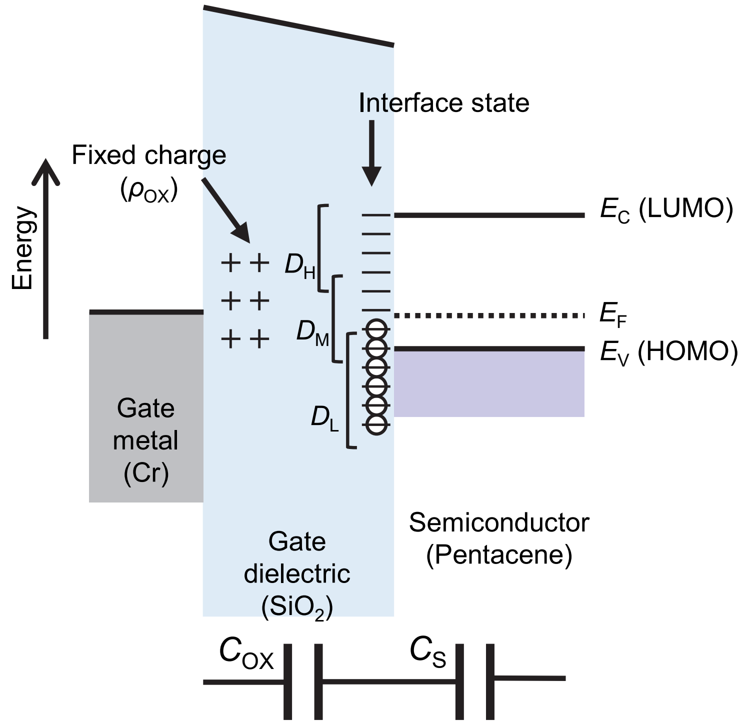


Figure 4.1: Schematic band diagram of Cr/SiO_2/pentacene structure.

4.3 Experimental methods

Figures 4.2(a) and 4.2(b) show cross sections of a pentacene TFT and a MOS capacitor, respectively. TFTs and MOS capacitors were fabricated on glass substrates, Corning (R) EAGLE XG. Each layer for the TFT and capacitor was deposited through a metal mask. First, a 20-nm-thick Cr layer was deposited as a gate electrode. Then, a SiO_2 layer was deposited as a gate dielectric by rf sputtering. The SiO_2 layer has a thickness of about 120 nm and a capacitance per unit area (C_{OX}) of about 27 nF/cm^2. The C_{OX} values determined from C–V

measurement are shown in Table 4.1. The substrates were cleaned with acetone, isopropanol, and UV ozone. Then, the SiO_2 surfaces were exposed to oxygen plasma for a time (t_p) of 10 to 30 s under a condition of an O_2 flow rate of 100 mL/min and an AC power for plasma generation of 9.2 W. After oxygen plasma treatment, or UV ozone treatment as a reference without oxygen plasma treatment, the substrates were immediately exposed to hexamethyldisilazane (HMDS) vapor for 30 min at 120 ˚C. The TFT without oxygen plasma treatment is represented as $t_p = 0$ s afterhere. A 45-nm-thick pentacene layer was deposited at a rate of 0.2 Å/s on the substrate of room temperature. Finally, a 45-nm-thick Au layer was thermally deposited as the top electrode of MOS capacitors and as the drain/source electrodes of TFTs. For TFTs, the channel width (W) is 400 μm and the channel length (L) is 120 μm. For MOS capacitors, the MOS capacitor area of Au/pentacene/SiO_2/Cr structure is 2.7×10^{-3} cm^2. The MOS capacitor has an area of Au/SiO_2/Cr structure, which is 0.3×10^{-3} cm^2. Capacitance values excluding the capacitance of the Au/SiO_2/Cr area are shown as then capacitance of a MOS capacitor.

All characteristics were examined in a dry-nitrogen filled glovebox at room temperature. The current–voltage characteristics of TFTs were measured by using a semiconductor parameter analyzer, Agilent Technologies, B1500A. The capacitance characteristics of MOS capacitors were measured by using a source/measurement unit, Keysight Technologies, B2912A. A 100-mVrms AC voltage of a frequency of 200 Hz superimposed on a DC voltage (V_G) was applied to the Cr electrode with respect to the Au electrode as seen in Fig. 4.2(b).

For MOS capacitors, the C–V measurement was perfomed in the range of $V_G = V_1$ to V_2 where $V_1 = -10$ V, $V_2 = 10$, 15, 18, and 23 V for $t_p = 0$, 10, 20, and 30 s, respectively. To change the number of charges trapped in the interface states at a certain V_G, we adopted two time-profiles of applied V_G shown in Figs. 4.3(a) and 4.3(b). One is a quasi-pulse wave and the other is a normal sweep. The holding voltage in the quasi-pulse wave, which was set at –10 V, contributes to suppression of unintended charge transfer under a certain V_G.

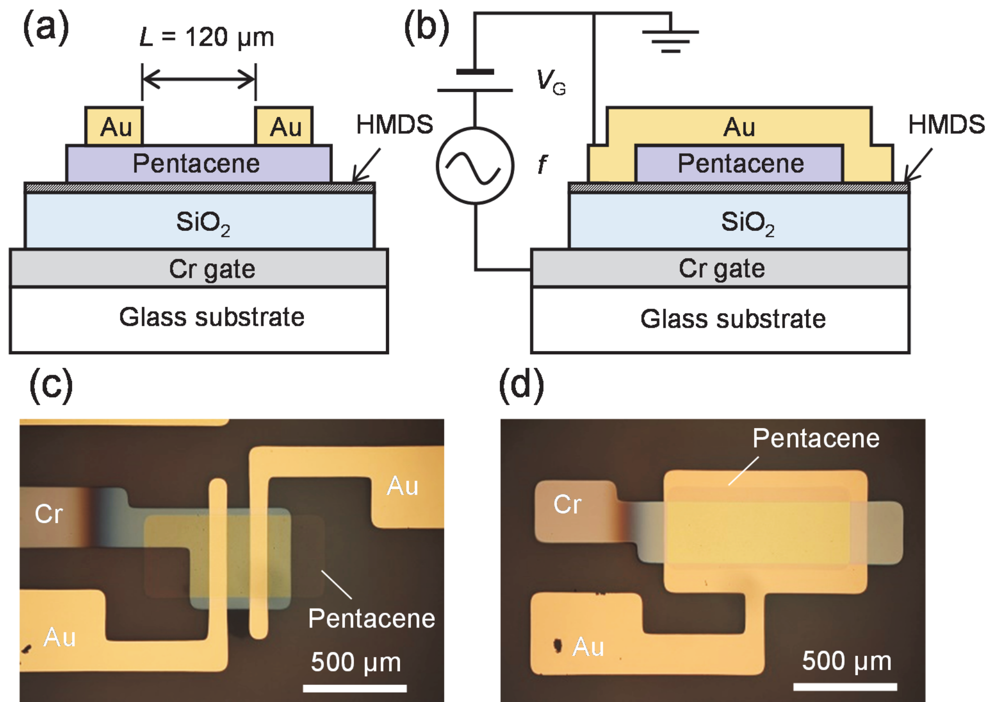


Figure 4.2: Cross sections of a pentacene (a) TFT and (b) MOS capacitor. Microphotographs of a fabricated (c) TFT and (d) MOS capacitor.

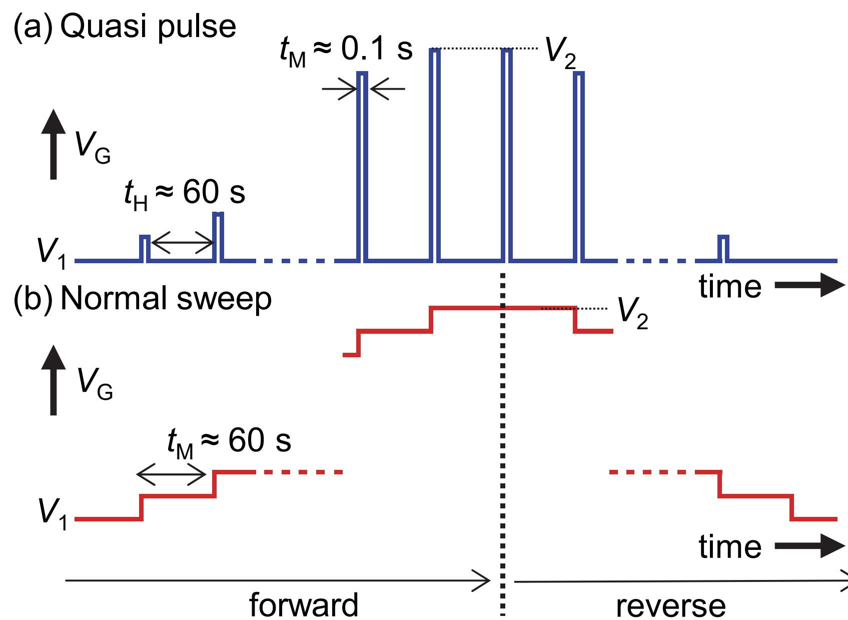


Figure 4.3: Measuring methods of capacitance–voltage characteristics of MOS capacitors in this study. Two time-profiles of applied gate voltage: (a) a quasi-pulse wave and (b) a normal sweep.

4.4 Results and discussion

4.4.1 Transistor characteristics

Figure 4.4(a) shows the drain current (I_D) versus gate voltage (V_G) characteristics of pentacene TFTs in the saturation regime at a drain voltage (V_D) of −20 V. The I_D–V_G characteristics were obtained by the forward sweep from a positive V_G to −20 V, and the reverse sweep from −20 V to the positive V_G. The plasma treatment time t_p is 0, 10, 20, and 30 s. The I_D–V_G curves shift to positive gate voltages with increase in t_p. For $|I_D| > 10^{-10}$ A, the I_D–V_G curves do not exhibit large hysteresis in the forward of positive to negative V_G and reverse of negative and positive V_G sweeps. For $|I_D| < 10^{-10}$ A, a small hysteresis appears in the sweep. This hysteresis may relate to shallow traps shown as D_M and/or D_H in Fig. 4.1.

The field-effect mobilities in the saturation regime (μ_{sat}), V_{TH}, and sub-threshold swing (S) are summarized in Table 4.1. The μ_{sat} and V_{TH} are calculated by fitting a line to $|I_D|^{1/2}$–V_G plots. The C_{OX} value shown in Table 4.2 is used for the calculation of μ_{sat}, being obtained from C–V measurement. μ_{sat} is in the range of 0.78 to 0.86 cm^2/(V s), and does not largely depend on t_p. In Fig. 4.4(b), V_{TH} is plotted with respect to t_p. By assuming values of Φ_M and Φ_S, Q in Eq. (2.5) can be calculated as a function of t_p. We used $\Phi_M = 4.8$ eV and $\Phi_S = 4.5$ eV for the calculation. Although Cr was used for the gate metal, the surface of Cr is easily oxidized in general. Thus, we adopted the work function reported for Cr_2O_3 as Φ_M [41]. The Φ_S value corresponds to the Fermi energy of pentacene [42].

Figure 4.4(c) shows the charge density Q_{TFT} calculated from Eq. (2.5). From the fitting curve, Q_0 and q_p are estimated to be 118.8 nC/cm^2 and −5.24 nC/(cm^2 s). By assuming that positive charges are uniformly distributed in SiO_2, ρ_0 is calculated as 2.0×10^{-2} C/cm^3 which corresponds to positive charges of 1.2×10^{17} /cm^3. The negative q_p value suggests that oxygen plasma treatment generates interface states serving as electron traps. The surface charge density $Q_{S,TFT}$ (= q_p t_p) is shown in Table 4.1.

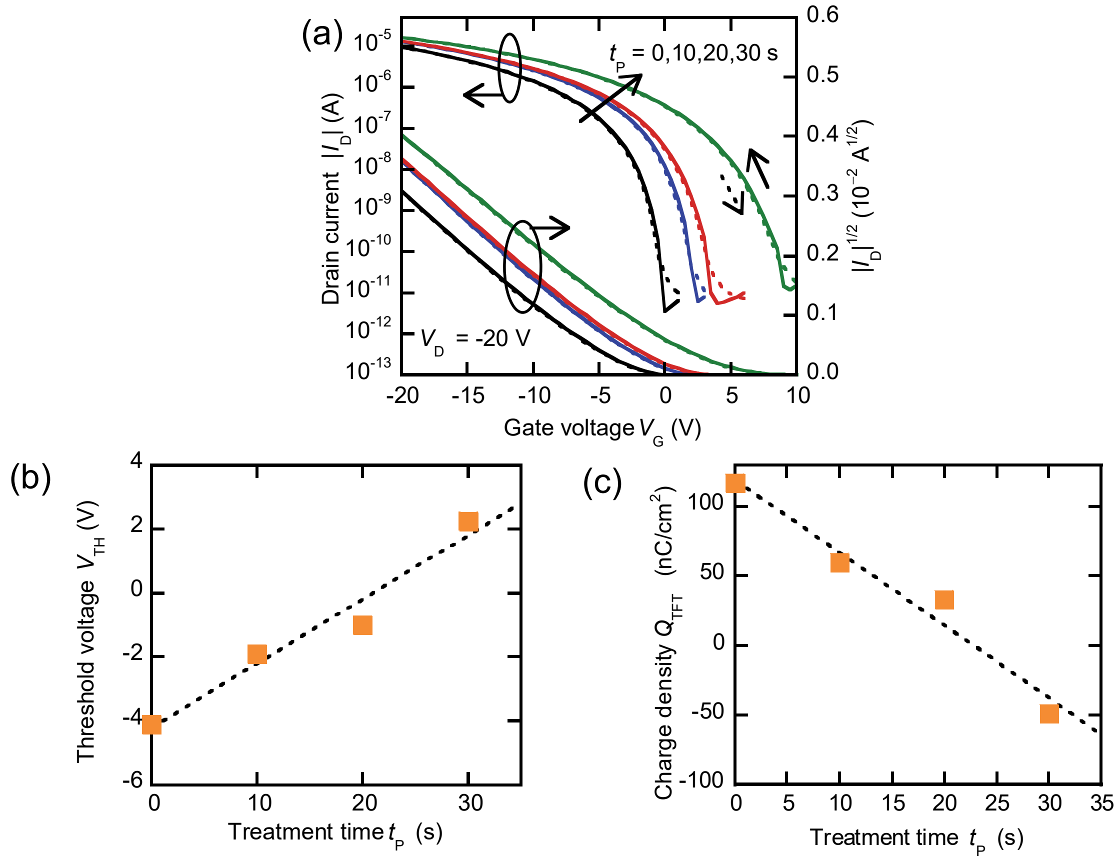


Figure 4.4: (a) Drain current versus gate voltage characteristics measured drain voltage $V_D = -20$ V for pentacene TFTs with SiO_2 gate dielectric treated by oxygen plasma for $t_P = 0$, 10, 20, and 30 s. (b) Threshold voltage estimated from the transfer characteristics of pentacene TFTs. (c) Charge density Q_{TFT} calculated from the threshold voltage in (b).

Table 4.1: Electrical properties of pentacene TFTs with SiO_2 treated by oxygen plasma for $t_P = 0$, 10, 20, and 30 s: mobility in the saturation regime μ_{sat}, threshold voltage V_{TH}, sub-threshold swing S, and surface charge density $Q_{S,TFT}$ (= q_P t_P).

t_P (s)	μ_{sat} (cm^2/(V s))	V_{TH} (V)	S (V/decade)	$Q_{S,TFT}$ (nF/cm^2)
0	0.85	–4.11	0.61	–
10	0.86	–1.90	0.70	–59.0
20	0.83	–0.99	0.72	–85.8
30	0.78	2.25	1.00	–168

4.3.2 MOS capacitor characteristics

Figures 4.5(a)–4.5(d) show the capacitance measured by quasi-pulse wave shown in Fig. 4.3(a), $C_{G,pulse}$, versus V_G characteristics of pentacene MOS capacitors for t_p = 0, 10, 20, and 30 s. Properties extracted from the $C_{G,pulse}$ characteristics are summarized in Table 4.2. For t_p = 10, 20, and 30 s, the C–V characteristics do not exhibit hysteresis in the forward and reverse measurement. This suggests that electrons trapped at the interface states by applying $V_G > -10$ V leave from the states when applying $V_G = -10$ V for a holding time of about 60 s. On the other hand, the C–V characteristic for t_p = 0 s exhibits a small hysteresis. The $C_{G,pulse}$ in the reverse measurement is slightly lower than that in the forward measurement. This may be due to presence of hole traps at the interface without oxygen plasma treatment.

The maximum and minimum values of C_G depend on the SiO_2 thickness. Although the SiO_2 layers were deposited under the same condition, unintentional difference in conditions leads to the difference in the SiO_2 thickness. For comparison of the C–V characteristics, we calculated a normalized capacitance C_n defined as

$$C_n = \frac{C_G(V_G) - \mathrm{Min}[C_G(V_G)]}{\mathrm{Max}[C_G(V_G)] - \mathrm{Min}[C_G(V_G)]}. \tag{4.9}$$

Figure 4.5(e) shows $C_{n,pulse}$ versus V_G of pentacene MOS capacitors for t_p = 0, 10, 20, and 30 s. The C–V curves shift to positive gate voltage with an increase in t_p.

The V_{FB} values were calculated based on Eq. (4.3). Figure 4.5(f) shows the C_S values calculated by substituting $C_{G,pulse}$ values into Eq. (4.1). The C_S decreases with an increase in V_G, and approaches 1.55, 1.58, 1.53, and 1.53 × 10^{-7} F/cm^2 for t_p = 0, 10, 20, and 30 s, respectively. The V_{FB} value, which equals V_G that satisfies $C_S \approx 3.1 \times 10^{-6}$ F/cm^2, are estimated to be −3.57, −0.77, 0.64, and 3.61 V for t_p = 0, 10, 20, and 30 s, respectively. For each t_p, this value is close to the V_{TH} value shown in Table 4.1. The V_{FB} as well as V_{TH} can be used for estimation of Q, Q_0, and q_p. Q_0 and q_p are estimated to be 98.7 nC/cm^2 and −5.92 cm^2/(cm^2 s), which are not far

from those estimated from V_{TH}. Electrons that cause Q_S (= q_P t_P) probably capture at interface states. We classify the interface state density into D_L. This is because Q_S does not cause hysteresis in the transfer characteristics of pentacene TFTs. This indicates that D_L work as deep traps. Thus, D_L corresponds to low energy levels as shown in Fig. 4.1. In other words, Q_S is expressed as

$$Q_S = e\int D_L dE. \tag{4.10}$$

The surface charge density $Q_{S,MOS}$ for D_L is shown in Table 4.2.

An increase in V_G leads to depletion of holes in the pentacene layer. Consequently, the minimum C_S corresponds to the capacitance of pentacene as insulator. By assuming the thickness of pentacene, relative dielectric constant can be calculated from the minimum C_S. The thickness of 45 nm shown in Sect. 4.3 is the thickness at the top of the pentacene. A pentacene generally has a dendritic structure. Thus, the average thickness is roughly assumed to be a half of 45 nm. Under this assumption, the relative dielectric constant is estimated to be 3.9. This value is almost the same as that reported by other group [43].

Table 4.2: Properties of pentacene MOS capacitors with SiO_2 treated by oxygen plasma for t_P = 0, 10, 20, and 30 s: gate dielectric capacitance per unit area C_{OX}, minimum capacitance of pentacene layer Min[C_S], flat band voltage V_{FB}, and surface charge density $Q_{S,MOS}$.

t_P (s)	C_{OX} (nF/cm^2)	Min[C_S] (nF/cm^2)	V_{FB} (V)	$Q_{S,MOS}$ (nF/cm^2)
0	26.5	155	−3.57	–
10	27.2	158	−0.77	−69.6
20	25.6	153	−0.64	−107
30	25.0	153	3.61	−181

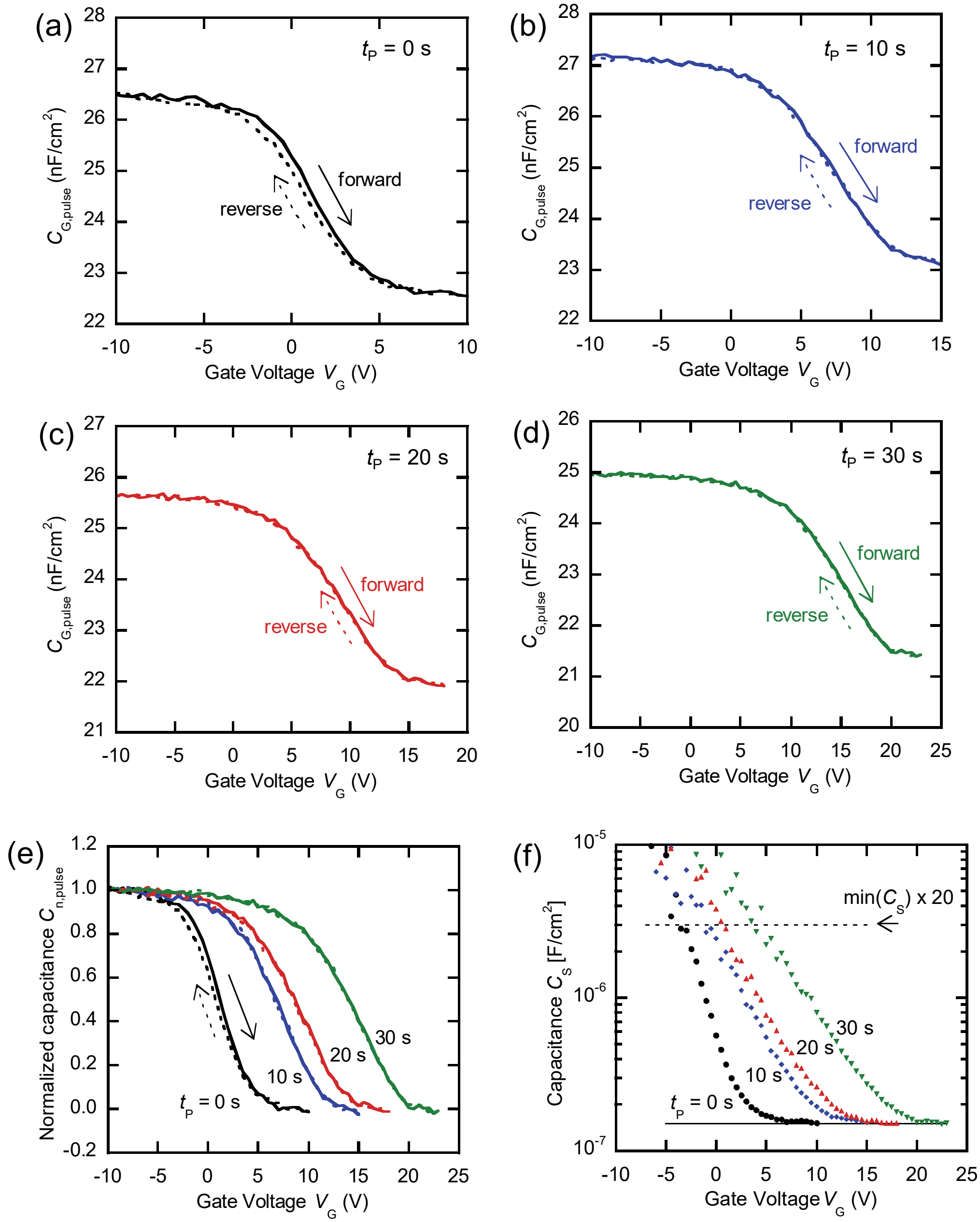


Figure 4.5: Capacitance versus gate voltage characteristics measured by applying a quasi-pulse wave for plasma treatment time t_P = (a) 0 s, (b) 10 s, (c) 20 s, and (d) 30 s. (e) Normalized capacitance versus gate voltage characteristics measured by applying a quasi-pulse wave for t_P = 0, 10, 20, 30 s. (f) Semiconductor capacitance calculated by substituting capacitance values, shown in (a)–(d), into Eq. (4.1).

4.3.3 Interface state density

For calculation of $D_{it}(\Psi_S)$, $C_{G,sweep}$ measured in the forward shown in Fig. 4.3(b) were used. Calculation of $D_{it}(\Psi_S)$ from Eq. (4.5) requires $C_{ref}(V_G)$ and $\Psi_{ref}(V_G)$. First, $D_{it}(\Psi_S)$ calculated from $C_{G,pulse}(V_G)$. For the calculation, $C_{G,pulse}(V_G)$ for $t_p = 0$ s is used as $C_{ref}(V_G)$. The $D_{it}(\Psi_S)$ is assigned as D_M. Next,

Since a MOS capacitor of $t_p = 0$ s has no interface state generated by oxygen plasma treatment, we chose $C_G(V_G)$ of $t_p = 0$ s as $C_{ref}(V_G)$. However, $C_G(V_G)$ of $t_p = 10$, 20, and 30 s involves the change in V_{FB} induced by the influence of D_L. To eliminate this influence, we shifted $C_G(V_G)$ of $t_p = 0$ s by the difference in V_{FB} and used it as $C_{ref}(V_G)$. In addition, the maximum and minimum of $C_{ref}(V_G)$ were adjusted to the maximum and minimum of $C_G(V_G)$ of $t_p = 10$, 20, or 30 s, respectively. Figures 5.6(a)–5.6(c) show $C_G(V_G)$ and $C_{ref}(V_G)$ curves for $t_p = 10$, 20, and 30 s. The $C_G(V_G)$ of $t_p > 0$ s is larger than $C_G(V_G)$ of $t_p = 0$ s. The difference in $C_G(V_G)$ is probably attributed to electrons trapped at interface states corresponding to D_M.

Quasi-static voltage of the normal sweep leads to electrons trapped at higher interface states. Figure 4.7 shows $C_G(V_G)$ measured by applying a quasi-pulse wave voltage and a normal sweep voltage. For $t_p = 10$, 20, and 30 s, the difference in $C_G(V_G)$ for pulse and sweep increase at $V_G > 10$ V. Here, we adopt $C_{G,pulse}(V_G)$ as $C_{ref}(V_G)$. The $C_{G,pulse}(V_G)$ involves the influence of D_M. Thus, the difference corresponds to electrons trapped at D_H.

Figure 4.8 shows D_M and D_H calculated from $C_G(V_G)$ and $C_{ref}(V_G)$ explained above. Indeed, D_M is distributed near $\Psi_S = \Psi_{FB}$ as shown in Fig. 5.1. The D_M are distributed in the range of $\Psi_S - \Psi_{FB} = 0.0 - 0.6$ eV. The D_M has the maximum at about 0.1 eV. The interface density increased with plasma treatment time. The difference in D_M for $t_p = 10$ s and for $t_p = 20$ s is small. For pentacene TFTs, the Q_{TFT} value for $t_p = 20$ s is far from the fitting line as seen in Fig. 4.4(c). This suggests that the interface state density for $t_p = 20$ s is less than density expected from $t_p =$ 20 s. Probably, the small difference in D_M is due to unintentional low density for $t_p = 20$ s. On

the other hand, the maximum of the interface density for t_p = 30 s is approximately 4.5 × 10^{12} /(cm^2 eV), which is three times as high as 1.5 × 10^{12} /(cm^2 eV) for t_p = 10 s. The D_M is roughly proportional to t_p.

On the other hand, D_H obtained by a normal sweep is distributed at high energy as compared with D_M obtained by a quasi-pulse wave. The D_H is broadly distributed in the range of $\Psi_S - \Psi_{FB}$ = 0.3 – 1.3 eV, and is in the order from 10^{10} to 10^{11} /(cm^2 eV). For $\Psi_S - \Psi_{FB}$ = 0.6 – 1.0 eV, the D_H is about 5 × 10^{10}, 1 × 10^{11}, and 2 × 10^{11} /(cm^2 eV) on average for t_p = 10, 20, and 30 s, respectively.

Probably, the interface states for D_M and D_H do not largely influence on the characteristics of TFTs when TFTs operates at V_G < 0 V. Conversely, positive V_G may temporarily lead to threshold voltage shift by electrons trapped at the interface states. The finding in this study is useful for operational stability in organic TFTs. The interface states at high energy level such as D_M and D_H may be used for applications that intentionally require temporary characteristic changes.

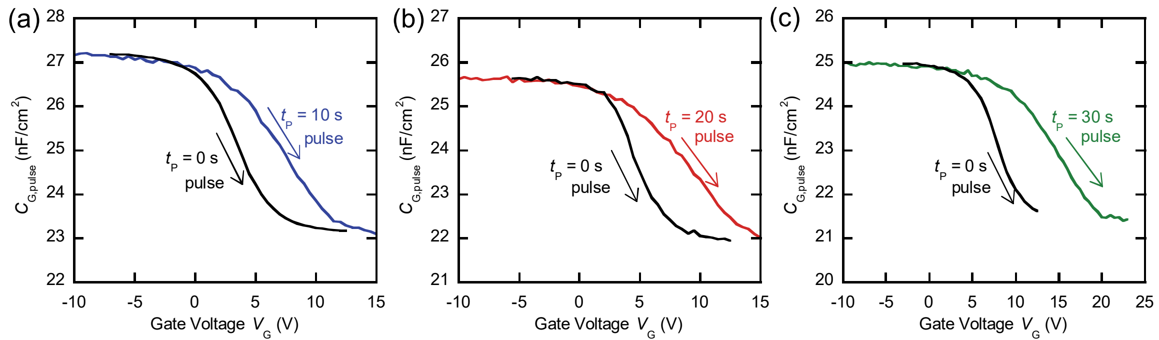


Figure 4.6: Capacitance versus gate voltage characteristics measured by applying a quasi-pulse wave for plasma treatment time t_p = 0 s as a reference characteristic and t_p = (a) 10 s, (b) 20 s, or (3) 30 s, respectively. The maximum and minimum values and flat band voltage value of a reference characteristic (t_p = 0 s) are adjusted to those of characteristics for t_p = 10, 20, or 30 s.

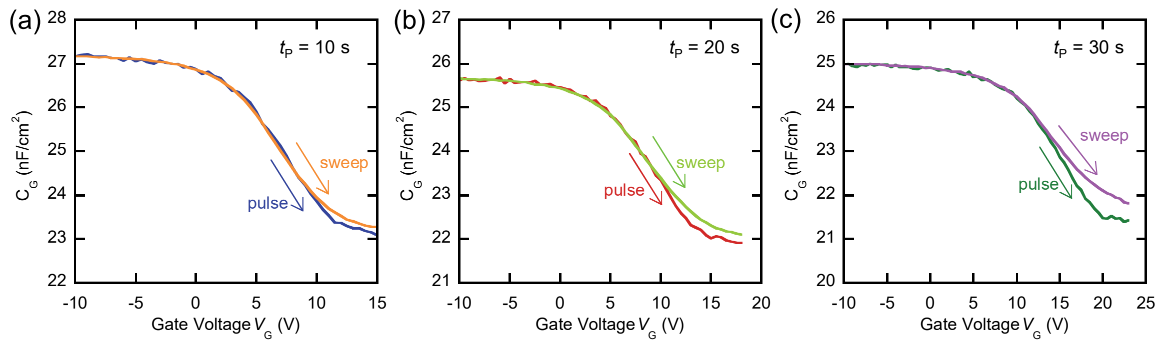


Figure 4.7: Capacitance versus gate voltage characteristics measured by a quasi-pulse wave and by a normal-sweep for plasma treatment time t_P = (a) 10 s, (b), 20 s, and (c) 30 s.

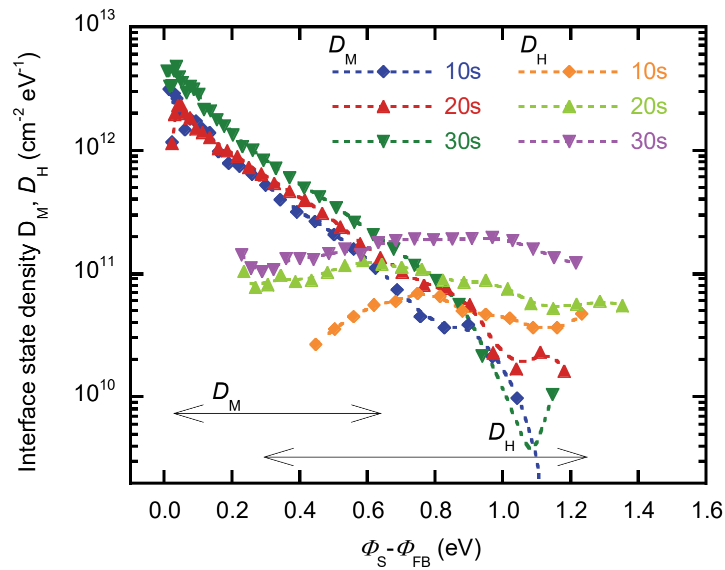


Figure 4.8: Energy distribution of interface trap densities D_M and D_H calculated from Eq. (4.5).

4.4 Summary

We measured C–V characteristics of pentacene MOS capacitors with a SiO_2 dielectric treated by oxygen plasma to extract the energy distribution of the interface states. For the pentacene MOS capacitors, the V_{FB} determined by the definition in this study were close to those of threshold voltages estimated from transfer curves of pentacene TFTs. The V_{FB} values increased with an increase in plasma treatment time. First, the C–V characteristics of MOS capacitors not treated by oxygen plasma was used as a reference for extraction of energy distribution. The interface states extracted from the C–V characteristics measured by applying a quasi-pulse wave voltage were distributed in the range of $\Psi_S - \Psi_{FB} = 0.0 - 0.6$ eV. The interface density increased from 1.5 to 4.5×10^{12} /(cm^2 eV) with plasma treatment time. Next, the C–V characteristics for a quasi-pulse wave voltage was used as a reference. The interface states extracted from the C–V characteristics measured by applying a normal sweep voltage were broadly distributed in the range of $\Psi_S - \Psi_{FB} = 0.3 - 1.3$ eV. The interface density is in the range of 1×10^{10} to 2×10^{11} /(cm^2 eV). The information of the energy distribution contributes to development of inorganic FET with oxide gate dielectric as well organic TFTs.

4.5 References

[1] C. D. Dimitrakopoulos, and P. R. L. Malenfant, Adv. Mater. **14**, 99 (2002).

[2] V. Coropceanu, J. Cornil, D. A. da S. Filho, Y. Oliver, R. Silbey, and J.-L. Brédas, Chem. Rev. **107**, 926 (2007).

[3] D. M. Taylor, Jpn. J. Appl. Phys. **55**, 02BA01 (2016).

[4] M. J. Kang, I. Doi, H. Mori, E. Miyazaki, K. Takimiya, M. Ikeda, and H. Kuwabara, Adv. Mater. **23**, 1222 (2011).

[5] K. Nakayama, Y. Hirose, J. Soeda, M. Yoshizumi, T. Uemura, M. Uno, W. Li, M. J. Kang, M. Yamagishi, Y. Okada, E. Miyazaki, Y. Nakazawa, A. Nakao, K. Takimiya, and J. Takeya, Adv. Mater. **23**, 1626 (2011).

[6] H. Minemawari, T. Yamada, H. Matsui, J. Tsutsumi, S. Haas, R. Chiba, R. Kumai, and T. Hasegawa, Nature **475**, 364 (2011).

[7] K. He, W. Li, H. Tian, J. Zhang, D. Yan, Y. Geng, and F. Wang, ACS Appl. Mater. Interfaces **9**, 35427 (2017).

[8] S. Haas, Y. Takahashi, K. Takimiya, T. Hasegawa, Appl. Phys. Lett. **95**, 022111 (2009).

[9] S. Kobayashi, T. Nishikawa, T. Takenobu, S. Mori, T. Shimoda, T. Mitani, H. Shimotani, N. Yoshimoto, S. Ogawa, and Y. Iwasa, Nat. Mater. **3**, 317 (2004).

[10] K. P. Pernstich, S. Haas, D. Oberhoff, C. Goldmann, D. J. Gundlach, B. Batlogg, A. N. Rashid, and G. Schitter, J. Appl. Phys. **96**, 6431 (2004).

[11] M. Salinas, C. M. Jäger, A. Y. Amin, P. O. Dral, T. M.-Friedrichsen, A. Hirsch, T. Clark, and M. Halik, J. Am. Chem. Soc. **134**, 12648 (2012).

[12] I. Hirata, U. Zschiechang, T. Yokota, K. Kuribara, M. Kaltenbrunner, H. Klauk, T. Sekitani, and T. Someya, Org. Electron. **26**, 239 (2015).

[13] T. T. Dao, T. Matsushima, R. Friedlein, H. Murata, Org. Electron. **14**, 2007 (2013).

[14] W.-J. Wum C.-H. Lee, C.-H. Hsu, S.-H. Yang, and C.-T. Lin, Thin Solid Films **548**, 576 (2013).

[15] Y. Abe, T. Hasegawa, Y. Takahashi, T. Yamada, and Y. Tokura, Appl. Phys. Lett. **87**, 153506 (2005).

[16] J. B.elasco, S. K. Mohapatra, Y. Zhang, S. Barlow, S. R. Marder, and A. Kahn, Appl. Phys. Lett. **105**, 063301 (2014).

[17] G. Nie, B. Dong, S. Wu, S. Zhan, Y. Xu, W. Sheng, Y. Liu, and X. Wu, ACS Omega **4**, 8506 (2019).

[18] Y. Chung, O. Johnson, M. Deal, Y. Nishi, B. Murmann, and Z. Bao, Appl. Phys. Lett. **101**, 063304 (2012).

[19] R. Shiwaku, Y. Yoshimura, Y. Takeda, K. Fukuda, D. Kumaki, and S. Tokito, Appl. Phys. Lett. **106**, 053301 (2015).

[20] R. Schroeder, L. A. Majewski, and M. Grell, Appl. Phys. Lett. **83**, 3201 (2003).

[21] M. Kitamura, Y. Kuzumoto, S. Aomori, M. Kamura, J. H. Na, and Y. Arakawa, Appl. Phys. Lett. **94**, 083310 (2009).

[22] S. Iba, T. Sekitani, Y. Kato, T. Someya, H. Kawaguchi, M. Takamiya, T. Sakurai, and S. Takagi, Appl. Phys. Lett. **87**, 023509 (2005).

[23] K. Fukuda, T. Sekitani, U. Zschieschang, H. Klauk, K. Kuribara, T. Yokota, T. Sugino, K. Asaka, M. Ikeda, H. Kuwabara, T. Yamamoto, K. Takimiya, T. Fukushima, T. Aida, M. Takamiya, T. Sakurai, and T. Someya, Adv. Funct. Mater. **21**, 4019 (2011).

[24] Y. Kimura, M. Kitamura, A. Kitani, and Y. Arakawa, Jpn. J. Appl. Phys. **55**, 02BB14 (2016).

[25] A. Kitani, Y. Kimura, M. Kitamura, and Y. Arakawa, Jpn. J. Appl. Phys. **55**, 03DC03 (2016).

[26] M. Halik, H. Klauk, U. Zschieschang, G. Schmid, C. Dehm, M. Schütz, S. Maisch, F. Effenberger, M. Brunnbauer, and F. Stellacci, Nature **431**, 964 (2004).

[27] A. Zen, D. Neher, K. Silmy, A. Holländer, U. Asawapirom, and U. Scherf, Jpn. J. Appl. Phys. **44**, 3721 (2005).

[28] H. Takahashi, Y. Hanafusa, Y. Kimura, and M. Kitamura, Jpn. J. Appl. Phys. **57**, 03EH03 (2018).

[29] H. Takahashi, M. Kitamura, Y. Hattori, and Y. Kimura, Jpn. J. Appl. Phys. **58**, SBBJ04 (2019).

[30] P. M. Lenahan. J. F. Conley Jr., J. Vac. Sci. Technol. B **16**, 2134 (1998).

[31] M. J. Powell, C. van Berkel, A. R. Franklin, S. C. Deane, and W. I. Milne, Phys. Rev. B **45**, 4160 (1992).

[32] M. L. Reed, and J. D. Plummer, J. Appl. Phys. **63**, 5776 (1988).

[33] S. C. Witczak, J. S. Suehle, and M. Gaitan, Solid State Electron. **35**, 345, (1992).

[34] Y. S. Yang, S. H. Kim, J.-I. Lee, H. Y. Chu, L.-M. Do, H. Lee, J. Oh, T. Zyung, M. K. Ryu, and M. S. Jang, Appl. Phys. Lett. **80**, 1595 (2002).

[35] J. Lee, J. W. Chung, J. Jang, D. H. Kim, J.-I. Park, E. Lee, B.-L. Lee, J.-Y. Kim, J. Y. Jung, J. S. Park, B. Koo, Y. W. Jin, and D. H. Kim, Chem. Mater. **25**, 1927 (2013).

[36] J. Jang, J. Kim, M. Bae, J. Lee, D. M. Kim, D. H. Kim, J. Lee, B.-L. Lee, B. Koo, and Y. W. Jin, Appl. Phys. Lett. **100**, 133506 (2012).

[37] M. Kuhn, Solid State Electron. **13**, 873 (1970).

[38] D. K. Schroder, Semiconductor Material and Device Characterization, 3rd ed. New York, USA, Wiley.

[39] L. M. Terman, Solid State Electron. **5**, 285 (1962).

[40] K. Zeng, Y. Jia, and U. Singisetti, IEEE Electron Device Lett. **37**, 906 (2016).

[41] M. Wilde, I. Beauport, F. Stuhl, K. Al-Shamery, and H.-J. Freund, Phys. Rev. B **59**, 13401 (1999).

[42] D.-J. Yun, J. G. Chung, C. H. Jung, H.-S. Han, J. C. Lee, B. Anass, S. Lee, Y. Kyung, and S.-H. Park, J. Electrochem. Soc. **160**, H436 (2013).

[43] P. E. Schwenn, P. L. Burn, and B. J. Powell, Org. Electron. **12**, 394 (2011).

Chapter 5
Evaluation of Carrier Mobility by Using Organic Metal-Oxide-Semiconductor Capacitors Based on a Distributed Constant Circuit

5.1 Introduction

Organic semiconductor devices, including thin film transistors (TFTs) [1,2], light-emitting diodes [3,4], photovoltaics [5,6], and chemical sensors [7,8], have attracted attention because of their potential application to flexible, large-area, light-weight, and low-cost electronic devices. In addition to these features, the field-effect mobilities in organic TFTs significantly improving with finding of novel materials [9] have reached over 10 $cm^2/(V\ s)$. With the improvement of organic device performance, the carrier transport in organic devices is required to be investigated in more detail [11,12].

For organic TFTs, the field-effect mobility and threshold voltage calculated from the current-voltage characteristics are used as standard evaluation for them [13]. The contact resistance between the contact electrode and the organic semiconductor in organic TFTs is often calculated based on a transfer line method [14-16]. In this method, the contact resistance is also calculated from the current-voltage characteristics obtained by DC measurement. On the other hand, impedance spectroscopy based on AC measurement is an evaluation methods for organic TFTs when focusing on the metal-oxide-semiconductor (MOS) or metal-insulator-semiconductor (MIS) structure [17,18]. Actually, the capacitance-voltage characteristics measured at a certain frequency have been used for investigation of the interface states [19,20], the flat-band voltage

[21-23], the injection barrier [24], and the stability [25]. The investigation is based on theory for Si-based MOS capacitors [26]. However, an organic MOS capacitor often has an area uncovered with the contact electrode to the organic semiconductor. In order to eliminate the influence, it is necessary to remove the organic layer uncovered with the contact electrode [18].

Some groups have examined organic TFTs [27,28] and organic MOS capacitors [29-33] considering organic semiconductor areas uncovered with the contact electrode. Hamadani et al. and Girolamo et al. investigated the characteristics of organic TFTs using equivalent circuits consisting of distributed elements for the uncovered area [27,28]. On the other hand, Jung et al. and Hayashi et al. reproduced the characteristics of organic MOS capacitors with uncovered organic areas using a distributed constant circuit [29] and a diffusion equation [30], respectively. In order to reproduce the measured results, it is necessary to consider both the effect of the uncovered area and that of the MOS capacitors covered by the electrode. The lengths of the uncovered areas were up to about 95 μm for Ref. 29 and 235 μm for Ref. 30. On the other hand, Ucurum and Goebel investigated the capacitance-voltage characteristics of pentacene MOS capacitors having uncovered areas up to 4 mm in length [31]. They analyzed the characteristics separating into three components for metal/insulator/metal, covered MIS, and uncovered MIS structures. Although the method of the analysis is effective, it is seems that the hysteresis in the capacitance-voltage characteristics caused difficulty in quantitative analysis. If a MOS capacitor having an uncovered MOS area sufficiently larger than a covered area is examined, it is possible to eliminate the influence of the covered MOS area and intensively analyze the carrier transport in organic layers uncovered with an electrode.

In this chapter, we report the capacitance characteristics of pentacene MOS capacitors with a large uncovered area in detail. The measured capacitance is systematically examined by assuming that the uncovered area is represented by a distributed constant circuit. The sheet resistance derived from the measured capacitance is used for calculation of the carrier mobility

in the pentacene layer. The carrier mobilities are compared with those calculated from the current-voltage characteristics of pentacene TFTs fabricated on the same substrates.

5.2 Analytical method

5.2.1 Characteristics of MOS capacitors with a large uncovered pentacene area

Figure 5.1(a) shows illustration of a pentacene MOS capacitor examined in this study. The pentacene layer has an area uncovered with the top electrode. For measurement of the capacitance, an AC voltage of frequency f superimposed on a gate voltage V_G is applied to the Cr gate electrode as seen Fig. 5.1(a). The length and the width of the uncovered area are denoted by L_{dis} and W_{dis}, respectively. The total capacitance of the MOS capacitor C can be represented as

$$C = C_0 + C_{MOS} + C_{dis}, \tag{5.1}$$

where C_0, C_{MOS}, and C_{dis} are the capacitances of Au/SiO_2/Cr, Au/pentacene/SiO_2/Cr, and pentacene/SiO_2/Cr structures shown in Fig. 5.1(b), respectively. When the capacitance per unit area of SiO_2 is denoted C_{OX}, $C_0 = C_{OX}\, S_0$ where S_0 is the area of the Au/SiO_2/Cr structure. The capacitance of the Au/pentacene/SiO_2/Cr structure C_{MOS} is given by

$$C_{MOS} = \begin{cases} C_{SiO2} & \text{when carriers are accumulated in the pentacene} \\ 1/\left(1/C_{SiO2} + 1/C_{semi}\right) & \text{when no carrier presents in the pentacene} \end{cases}, \tag{5.2}$$

where $C_{SiO2} = C_{OX}\, S_{MOS}$, $C_{semi} = \varepsilon_{semi}\, S_{MOS}/d_{semi}$, S_{MOS} is the area of the Au/pentacene/SiO_2/Cr structure, ε_{semi} is the dielectric constant, and d_{semi} is the thickness of the pentacene. Assuming that the pentacene/SiO_2/Cr structure is represented by a distributed constant circuit shown in Fig. 5.1(c), the capacitance component C_{dis} in the admittance Y ($Y = G + jB = G + j2\pi C_{dis}$), which is composed of conductance G and susceptance B, is given by

$$C_{dis} = C_{OX} W_{dis} L_{dis} \frac{1}{\alpha} \frac{\sinh\alpha + \sin\alpha}{\cosh\alpha + \cos\alpha}, \tag{5.3}$$

where

$$\alpha = \sqrt{4\pi f C_{\mathrm{OX}} R_{\mathrm{sh}} L_{\mathrm{dis}}^{2}} \,, \tag{5.4}$$

is a dimensionless quantity, R_{sh} is the sheet resistance in the pentacene layer, and f is the frequency for capacitance measurement [32,33]. Equation (5.3) can be derived by assuming that the line inductance and parallel resistance in a distributed constant circuit with open termination are equal to zero. When a function $g(\alpha)$ is defined as

$$g(\alpha) = \frac{1}{\alpha} \frac{\sinh\alpha + \sin\alpha}{\cosh\alpha + \cos\alpha} \,, \tag{5.5}$$

the function has the following properties:

$$\lim_{\alpha \to +0} g(\alpha) = 1 \,, \tag{5.6a}$$

$$\lim_{\alpha \to +\infty} g(\alpha) = 0 \,. \tag{5.6b}$$

Therefore, the dependence of C_{dis} on R_{sh} exhibits that

$$C_{\mathrm{dis}} \approx C_{\mathrm{OX}} W_{\mathrm{dis}} L_{\mathrm{dis}} \quad \text{for} \quad R_{\mathrm{sh}} \ll \left(1 / f C_{\mathrm{OX}} L_{\mathrm{dis}}^{2}\right), \tag{5.7b}$$

$$C_{\mathrm{dis}} \approx 0 \quad \text{for} \quad R_{\mathrm{sh}} \gg \left(1 / f C_{\mathrm{OX}} L_{\mathrm{dis}}^{2}\right), \tag{5.7b}$$

When pentacene is a *p*-type material, the decreases in V_{G} leads to the accumulation of holes in a semiconductor layer, the decrease in R_{sh}, and the asymptotic to ($C_0 + C_{\mathrm{SiO2}} + C_{\mathrm{OX}} W_{\mathrm{dis}} L_{\mathrm{dis}}$) of C. On the other hand, the increase in V_{G} leads to the depletion of hole, the increase in R_{sh}, and the asymptotic to $\{C_0 + 1/(1/C_{\mathrm{SiO2}} + 1/C_{\mathrm{semi}})\}$ of C. Since R_{sh} can be estimated from an experimental C value.

For the Au/pentacene/SiO_2/Cr structure in Fig. 5.1(b), the bulk resistance for the pentacene and the contact resistance at the interface of Au and pentacene are not considered in this thesis. This is because we focus on the characteristics of C_{dis} for the pentacene/SiO_2/Cr structure. Although C defined in Eq. (5.1) does not contain effect of the resistances mentioned above, capacitances measured in this study are actually reproduced by the C defined in Eq. (5.1) as

seen in Sect. 5.4.

5.2.2 Mobility and threshold voltage in uncovered pentacene area

When V_G is applied to the Cr gate electrode, the sheet resistance R_{sh} induced by hole carriers accumulated in the pentacene layer can be expressed as

$$R_{\mathrm{sh}} = \frac{1}{\mu C_{\mathrm{OX}} \left| V_{\mathrm{G}} - V_0 \right|}, \tag{5.8}$$

on the basis of the assumption that

$$R_{\mathrm{sh}} = \frac{1}{\sigma\delta}, \tag{5.9a}$$

$$\sigma = en\mu = e\frac{n_{\mathrm{S}}}{\delta}\mu = \frac{Q_{\mathrm{S}}}{\delta}\mu, \tag{5.9b}$$

$$Q_{\mathrm{S}} = C_{\mathrm{OX}} \left| V_{\mathrm{G}} - V_0 \right|. \tag{5.9c}$$

Here, μ is the carrier mobility for the hole, σ is the conductivity, n is the density of the hole, δ is the thickness of the accumulation layer, n_S is the area density of the charge, Q_S is the surface charge density, and V_0 is the maximum value in voltages at which holes accumulate. V_0 corresponds to threshold voltage of the MOS transistor. The notation for the voltage V_0 is used to distinguish it from the threshold voltage estimated from experimental results of transistors. The R_{sh} value estimated from an experimental C depends on V_G. The μ and V_0 values can be calculated by fitting a curve to the relation between R_{sh} and V_G. Equation (5.8) relates to Eq. (2.2). Actually, Eq. (5.8) is derived from Eq. (2.2) by dividing V_D by I_D. Since the structure in Fig. 5.1(a) corresponds to a transistor having no drain electrode, the measurement for the structure satisfies the condition that $|V_D|$ is small.

5.3 Experimental methods

Pentacene MOS capacitors and pentacene TFTs were fabricated on glass substrates, Corning (R) EAGLE SG. The cross sections are shown in Figs. 5.1(a) and 5.2(a), respectively. Figure 5.1(d) shows microphotograph of a fabricated pentacene MOS capacitor. The fabrication process is almost the same as that of study in chapter 4 except for oxygen plasma treatment. Each layer for the capacitor and the TFT was prepared by use of a metal mask common to the capacitor and the TFT. After cleaning the glass substrate, a 20 nm thick Cr layer for the gate electrode was deposited on the glass substrate by thermal evaporation. Then, a 120 nm thick SiO_2 gate dielectric was deposited by rf sputtering under a condition that a flat surface is obtained [34]. The SiO_2 dielectric had a capacitance per unit area (C_{OX}) of 26.5 nF/cm^2, which was determined by measurement of the capacitance at 1 kHz. The SiO_2 surface was treated with UV ozone for 15 min, and was immediately exposed to hexamithyldisilazane (HMDS) vapor at 120 ˚C for about 30 min. A 45 nm thick pentacene was deposited on the SiO_2 surface at room temperature. The deposition rate was 0.02 nm/s. Finally, a 45 nm thick Au layer was deposited as the drain/source electrodes for TFTs and as the top electrode for MOS capacitors. For MOS capacitors, the width (W_{dis}) and length (L_{dis}) of an uncovered pentacene layer are 200 µm and in the range of 500 to 2500 µm, respectively. For TFTs, the channel width (W) and length (L) were 400 µm and in the range of 55 to 215 µm, respectively.

All the measurements were performed in a dry-nitrogen filled glovebox at room temperature. The capacitance characteristics of MOS capacitors were measured with a source/measurement unit, Keysight Technologies, B2912A. An AC voltage of 100 mVrms superimposed on a DC voltage was applied to the Cr gate electrode. The current characteristics of TFTs were measured with a semiconductor parameter analyzer, Agilent Technologies, B1500A.

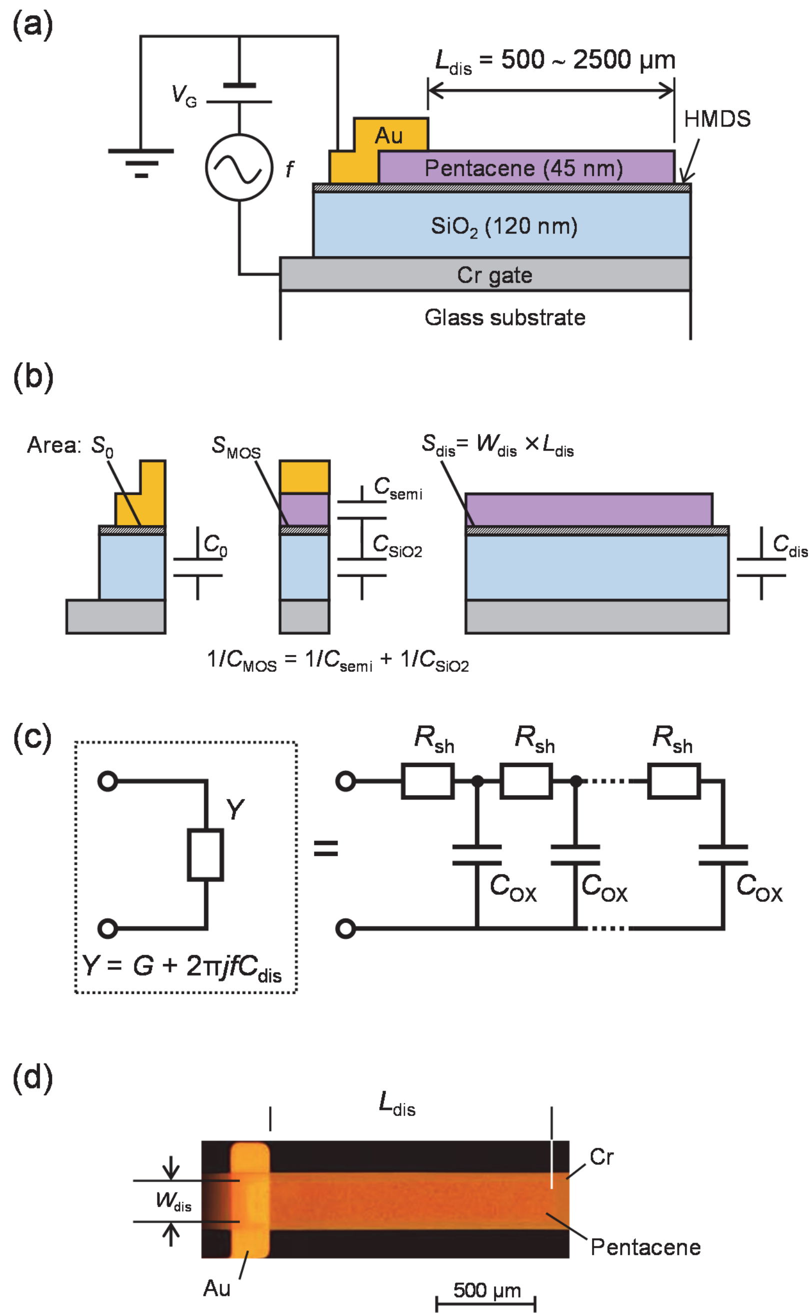


Figure 5.1: (a) Cross section of a pentacene MOS capacitor with an uncovered area examined in this study. (b) Structures separated into three parts of Au/SiO_2/Cr, Au/pentacene/SiO_2/Cr, and pentacene/SiO_2/ Cr. (c) Distributed constant circuit adopted as an equivalent circuit for the pentacene/SiO_2/Cr structure uncovered with Au. (d) Microphotograph of a fabricated pentacene MOS capacitor.

5.4 Results and discussion

5.4.1 Transistor characteristics

Pentacene TFTs were fabricated on the same substrate for MOS capacitors in order to compare the characteristics of TFTs with those of MOS capacitors. The schematic illustration of the TFT is shown in Fig. 5.2(a). Figure 5.2(b) shows the drain current (I_D) versus gate voltage (V_G) characteristics of a pentacene TFT with L = 115 μm measured at drain voltage V_D = −20 V. The transfer curve showed characteristics of a typical *p*-channel organic TFT, and exhibited no large hysteresis in the forward and reverse sweep. For the TFT in Fig. 5.2(b), the field-effect mobility (μ_{sat}) and the threshold voltage (V_{TH}) in the saturation regime were estimated to 0.86 $cm^2/(V\ s)$ and −4.51 V, respectively. The transfer characteristics in the saturation and linear regime o pentacene TFTs with different channel lengths are respectively shown in Figs. 5.3 and 5.4, respectively. The field-effect mobility (μ_{lin}) in the linear regime, μ_{sat}, and V_{TH} values calculated from transfer characteristics are summarized in Table 5.1. The μ_{lin} and μ_{sat} values did not largely depend on L. Although μ_{lin} was slight lower than μ_{sat}, the difference between μ_{lin} and μ_{sat} was not large. The averages of μ_{lin}, μ_{sat} and V_{TH} for TFTs with L = 55–215 μm were 0.79 $cm^2/(V\ s)$, 0.84 $cm^2/(V\ s)$, and −4.3 V, respectively. The mobilities are in the range of typical values for pentacene TFTs with top contact structure [13,35].

Figure 5.2(c) shows width-normalized on resistance (R_{on}) versus L calculated fot the TFT of Fig. 5.2(b). The plots for each V_G is almost on a line. From Eqs. (2.3) and (2.4), the slope and the intercept of the line fitting to data of $R_{on}\ W$ versus L are equal to the sheet resistance R_{TFT} and the contact resistance ($R_C\ W$), respectively. The $R_C\ W$ values decreased with an increase of $|V_G - V_{TH}|$, and 3.24 kΩ cm for $V_G - V_{TH}$ = −4 V and 214 Ω cm for $V_G - V_{TH}$ = −20 V. The R_{on} W values of the TFT with L = 55 μm are equal to 52.06 kΩ cm for $V_G - V_{TH}$ = −4 V and 13.12 kΩ cm for $V_G - V_{TH}$ = −20 V. The $R_C\ W$ value is less than 10% of the $R_{on}\ W$ value even if V_G − V_{TH} = −4 V. The low contact resistance supports no large channel-length dependence of μ_{lin} and

μ_{sat}. The output characteristics of pentacene TFTs with different channel lengths are shown in Fig. 5.5. It seems that the contact resistance did not largely influence on the output characteristics.

Figure 5.2(d) shows R_{TFT} obtained as a function of (V_G–V_{TH}). A curve fitting to the plots is obtained as

$$R_{TFT} = \frac{1}{\left(0.63\,\mathrm{cm}^2/\mathrm{V\,s}\right)\times C_{OX}\left|V_G-\left(V_{TH}+0.10\,\mathrm{V}\right)\right|}. \tag{5.10}$$

The threshold voltage requires a small calibration of 0.10 V. On the other hand, the mobility (μ_I) in the intrinsic transistor without contact resistance is estimated to be 0.63 cm^2/(V s). Although R_{TFT} does not include the influence of contact resistance, the mobility estimated from Fig. 5.2(d) is lower than μ_{lin} and μ_{sat} calculated from transfer curves. The slope of the $|I_D|^{1/2}$–V_G curve in the saturation regime slightly increases with a decrease of V_G as seen in Fig. 5.3. Also, the $|I_D|$–V_G curve in the linear regime slightly differs from the linearly increase as seen in Fig. 5.4. The nonlinearity may lead to over-estimation in the mobility estimated from R_{TFT} is close to the intrinsic mobility in the pentacene layer.

Table 5.1: Electrical properties of pentacene TFTs with different channel lengths: mobility in the linear regime μ_{lin}, mobility in the saturation regime μ_{sat}, and threshold voltage V_{TH}.

L (μm)	μ_{lin} (cm^2/(V s))	μ_{sat} (cm^2/(V s))	V_{TH} (V)
55	0.81	0.86	–4.2
75	0.76	0.80	–4.3
95	0.77	0.82	–4.5
115	0.79	0.84	–4.7
215	0.80	0.83	–3.5

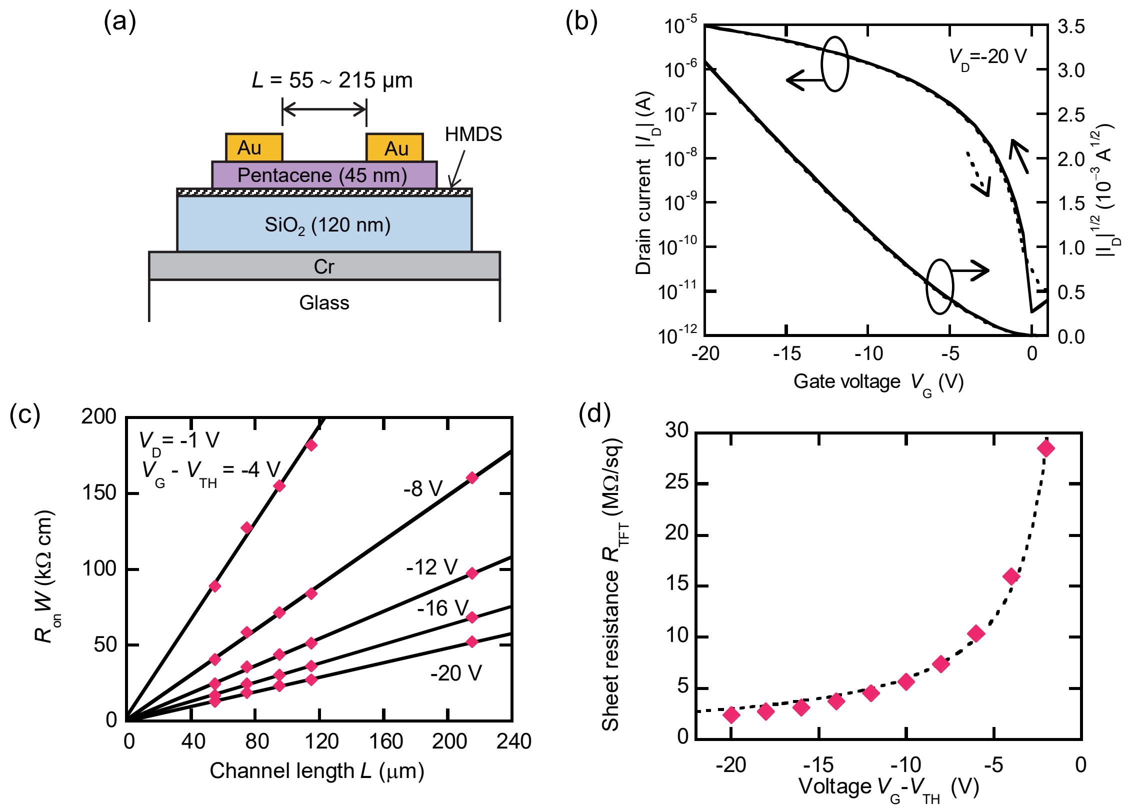


Figure 5.2: (a) Cross section of a pentacene TFT. (b) Transfer characteristics measured at $V_D = -20$ V for a pentacene TFT with $L = 115$ µm. (c) Width-normalized on-resistance $R_{on}\,W$ calculated for pentacene TFTs with $L = 55, 75, \ldots, 215$ µm. (d) Sheet resistance R_{TFT} for pentacene TFTs calculated from the width-normalized on-resistance shown in (c); the dashed line is a line fitting to measured R_{TFT} represented by filled diamonds using Eq. (2.4).

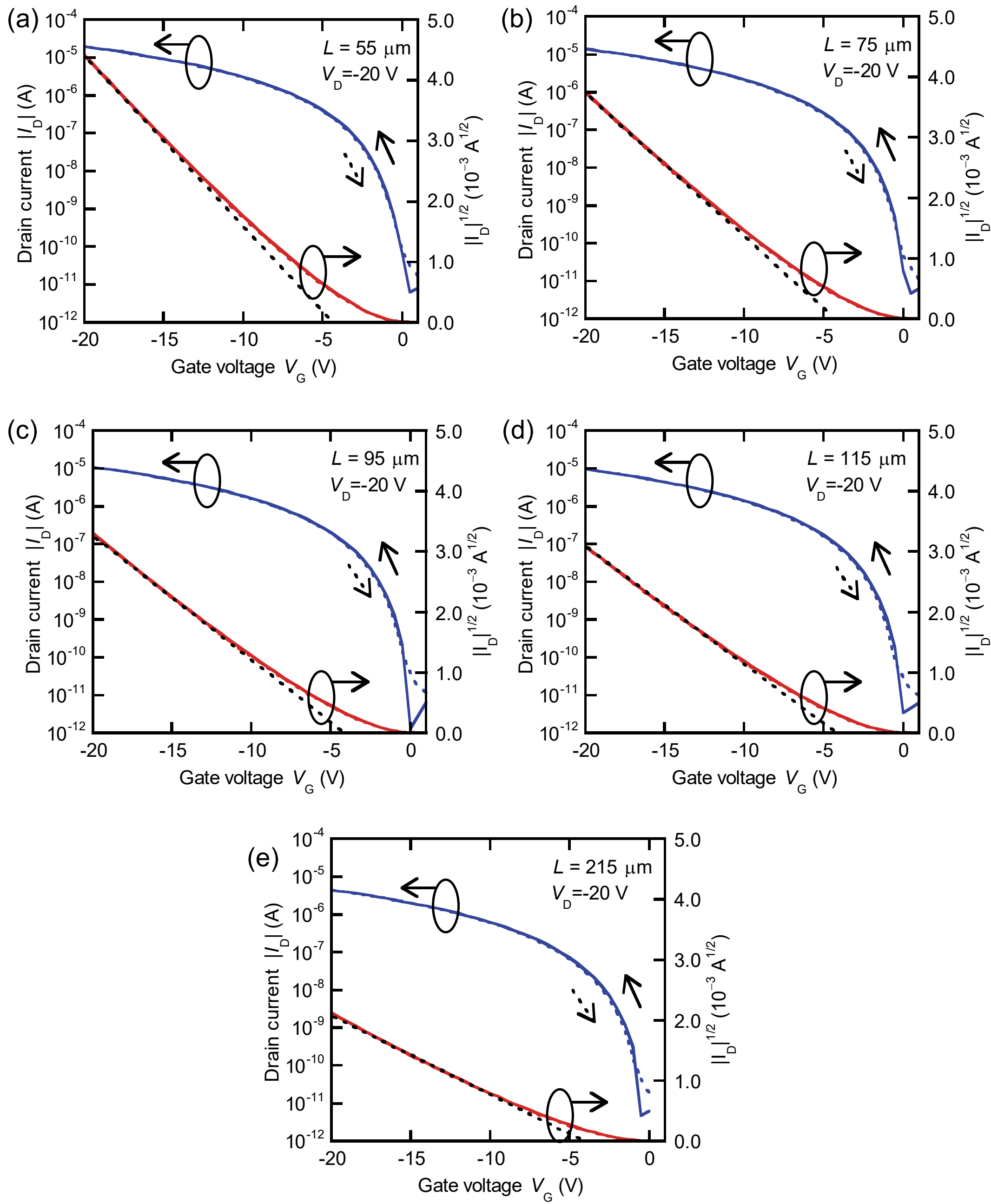


Figure 5.3: The transfer characteristics in the saturation regime at a drain voltage of –20 V of pentacene TFTs. The channel lengths are (a) 55 µm, (b) 75 µm, (c) 95 µm, (d) 115 µm, and (e) 215 µm. The solid and dotted lines are data taken from positive-to –negative (forward) and negative-to-positive (reverse) gate voltage sweeps, respectively. The black dotted line is a line fitting to the $|I_D|^{1/2}$–V_G curve, being for estimation of μ_{sat} and V_{TH}.

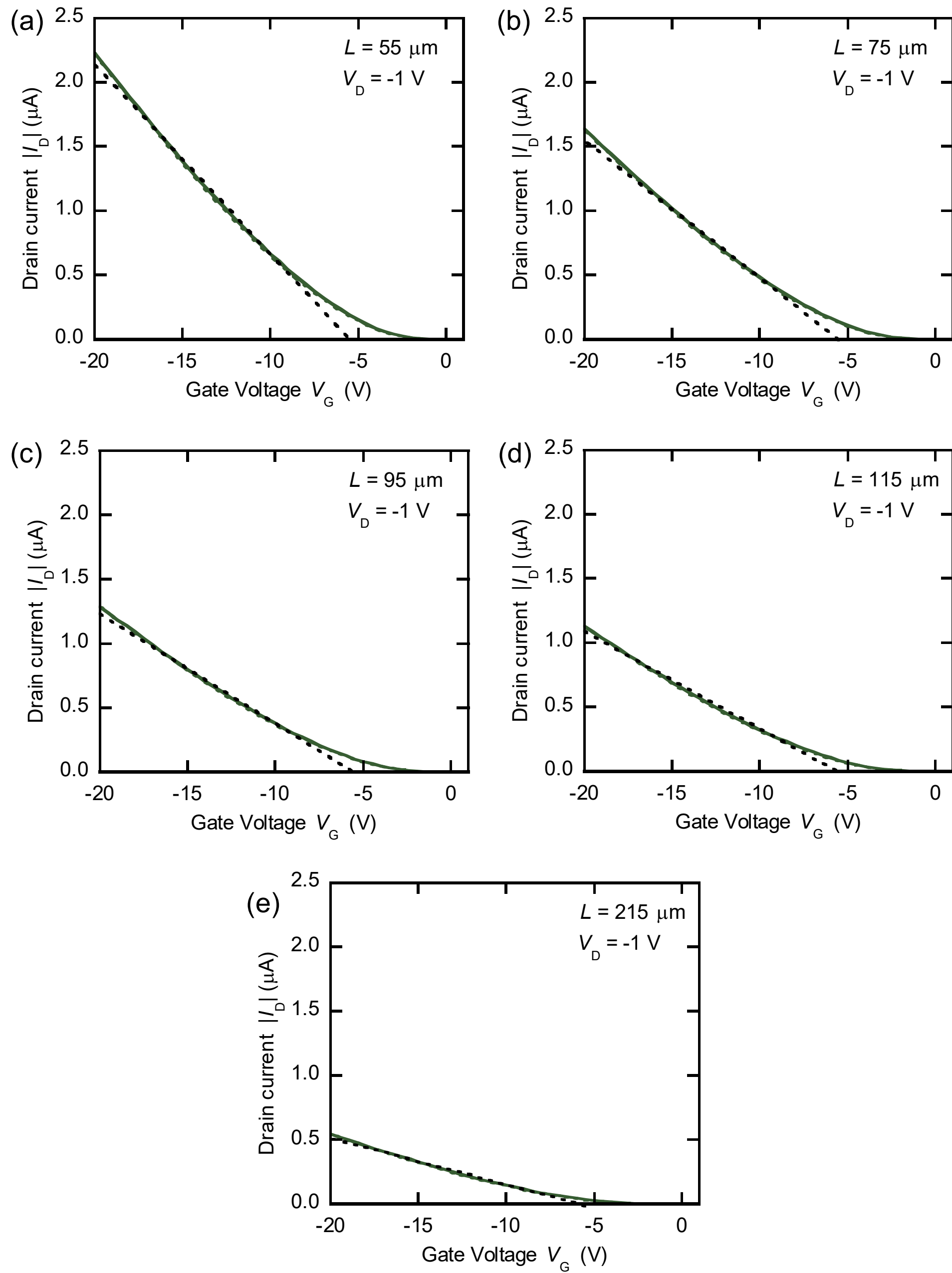


Figure 5.4: The transfer characteristics in the linear regime at a drain voltage of −1 V of pentacene TFTs. The channel lengths are (a) 55 μm, (b) 75 μm, (c) 95 μm, (d) 115 μm, and (e) 215 μm. The solid and dotted lines are data taken from positive-to –negative (forward) and negative-to-positive (reverse) gate voltage sweeps, respectively. The black dotted line is a line fitting to the $|I_D|-V_G$ curve, being for estimation of μ_{lin}.

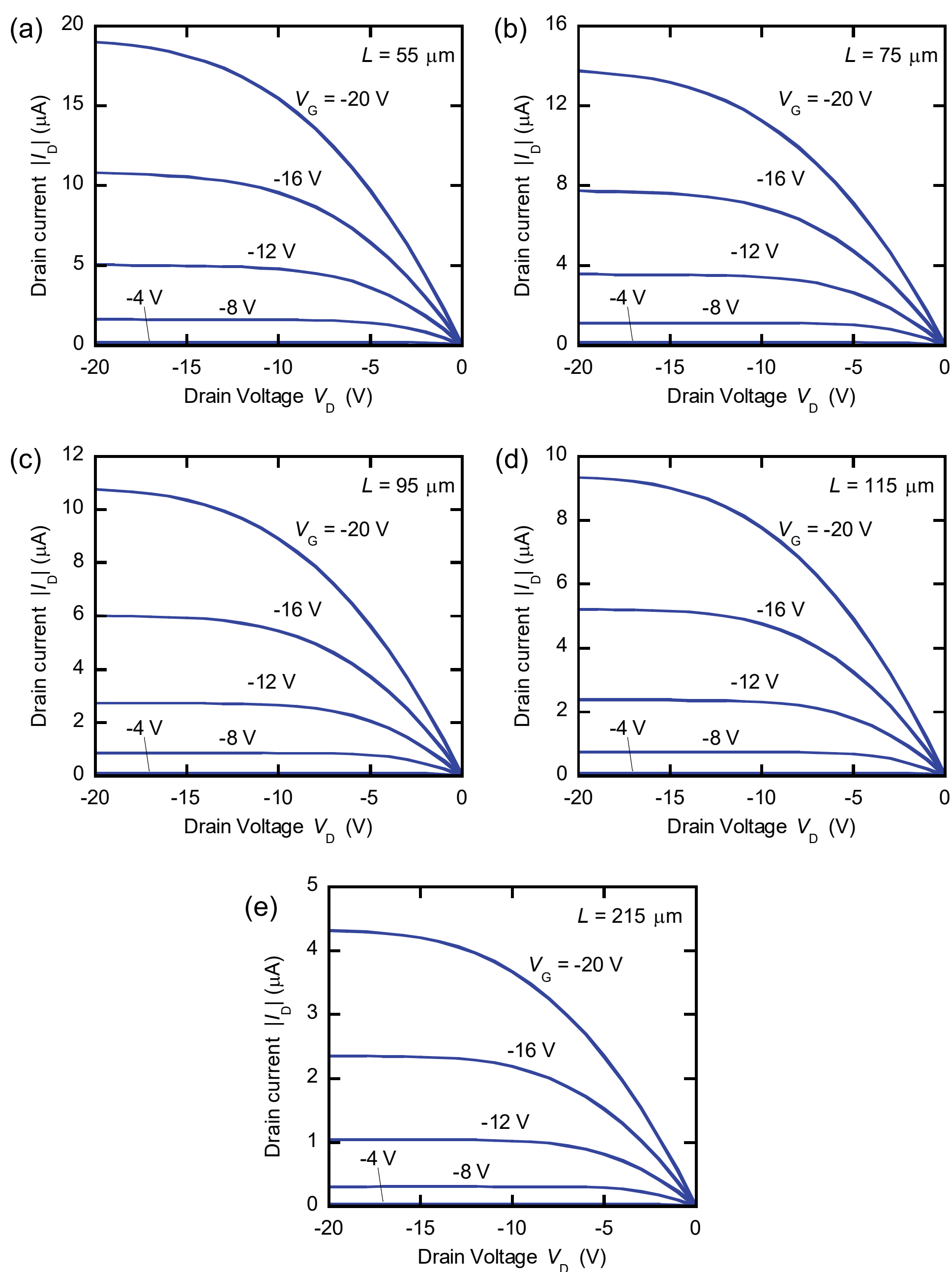


Figure 5.5: The output characteristics of pentacene TFTs with channel lengths of (a) 55 μm, (b) 75 μm, (c) 95 μm, (d) 115 μm, and (e) 215 μm.

5.4.2 MOS capacitor characteristics

Figure 5.6(a) shows the capacitance−voltage (C−V) characteristics measured for a pentacene MOS capacitor of L_{dis} = 500 μm. The C−V characteristics had no large hysteresis in the forward and reverse sweep. For frequency f = 1 and 10 Hz, the capacitance approaches 44.1 pF with a decrease of V_G. The value is close to $(C_0 + C_{SiO2} + C_{OX} W_{dis} L_{dis})$ = 42.4 pF. Thus, the approach is consistent with Eqs. (5.1), (5.2) and (5.7a). The capacitance of 44.1 pF indicates the accumulation of holes to the whole pentacene area of the pentacene/SiO_2/Cr structure. On the other hand, the capacitance at V_G > 5 V is about 15.7 pF for f = 1 to 1k Hz. The value is close to $\{C_0 + 1/(1/C_{SiO2} + 1/C_{semi})\}$ = 15.1 pF. Thus, the capacitance at V_G > 5 V is consistent with Eqs. (5.1), (5.2) and (5.7b). Note that it is difficult to know the accumulation of holes in the pentacene of the Au/pentacene/SiO_2/Cr structure from the C−V characteristics. This is because the difference between $1/(1/C_{SiO2} + 1/C_{semi})$ = 4.5 pF and C_{SiO2} = 5.3 pF is small. For f = 1 Hz, the C value dramatically decreases between V_G = −2 and 0 V. The gate voltage around −1 V corresponds to the threshold voltage V_0 in Eq. (5.9c) for a MOS capacitor.

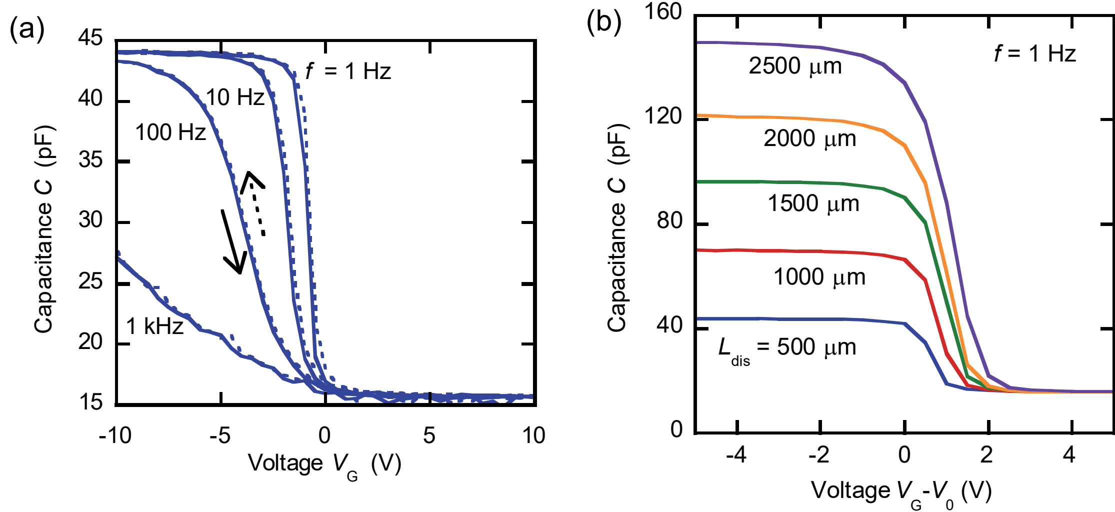


Figure 5.6: (a) C–V characteristics of a pentacene MOS capacitor with L_{dis} = 500 μm measured at f = 1, 10, 100, 1k Hz. (b) C versus (V_G – V_0) characteristics of pentacene MOS capacitors with different L_{dis} measured at 1 Hz.

Figure 5.6(b) shows the capacitance characteristics measured for pentacene MOS capacitors of L_{dis} = 500–2500 μm at f = 1 Hz. Since the MOS capacitors have different V_0, the horizontal axis is represented by (V_G – V_0). Here, the V_0 value roughly estimated from the C–V characteristics was used for Fig. 5.6(b). For all L_{dis}, the capacitance decreases down to 15.7 pF with an increase of (V_G – V_0). Since the MOS capacitors have the same S_0 and S_{MOS} values, where S_0 is the area of the Au/SiO_2/Cr structure, the approach to 15.7 pF is reasonable. On the other hand, the capacitance at (V_G – V_0) = –5 V depends on L_{dis}. The value of (C – 15.7 pF) is almost proportional to L_{dis}. This indicates that holes accumulate to the whole pentacene area at (V_G – V_0) = –5 V even for a long L_{dis} of 2500 μm.

Figure 5.7 shows the frequency dependence of C_{dis} at (V_G – V_0) of about –10 V for L_{dis} = 500–2500 μm, where C_{dis} is the capacitance of pentacene/SiO_2/Cr structure. For each L_{dis}, the C_{dis} value at f = 1 Hz almost (C – 15.7 pF) for the C value at (V_G – V_0) = –5 V shown in Fig. 5.6(b). The C_{dis} value gradually decreases with an increase of f. The dotted lines in Fig. 5.7 were

obtained by fitting to the plots of C_{dis} with Eq. (5.3). For each L_{dis}, the plots are almost on the dotted line. This indicates that the frequency dependence of C_{dis} is reproduced by Eq. (5.3), which is derived from the equivalent circuit shown in Fig. 5.1(c). In other words, C_{dis} at a certain V_G is determined by R_{sh} independent of f. Thus, R_{sh} at a certain V_G can be calculated from the C_{dis} at the V_G of the C–V characteristics using the inverse function of $g(\alpha)$ defined in Eq. (5.5). Note that the calculation of R_{sh} does not require the measurement of the frequency dependence of C_{dis}. In addition, the plots of C_{dis} measured are almost on the line fitting to them by use of Eq. (5.3) without the influence of the contact resistance. This suggests that the influence of the contact resistance on C_{dis} in negligible in the range of 1 Hz−1 kHz. The low contact resistance described in Sect. 5.4.1 also supports the suggestion. On the other hand, if a MOS capacitor with low channel resistance and/or large contact resistance is evaluated, the influence of the contact resistance should be considered [27]. In addition, the method is limited to a frequency range in which the presence of trap sites does not affect the admittance of evaluated MOS capacitor. If a MOS capacitor is evaluated at a frequency that trap sites affect the admittance, it is necessary to incorporate the component for the trap site into the admittance [36].

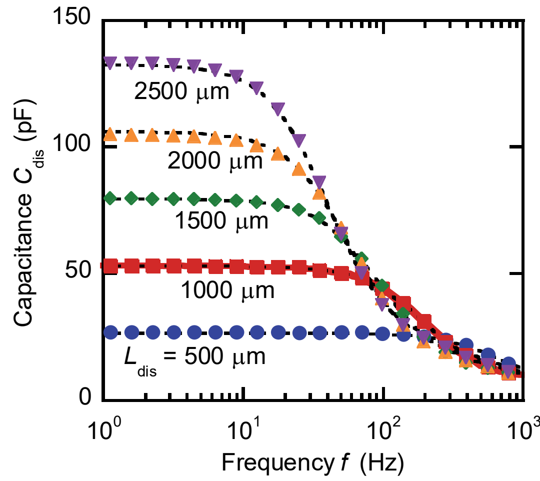


Figure 5.7: C_{dis} versus f characteristics of pentacene MOS capacitors with different L_{dis} measured at ($V_G - V_0$) of about −10 V. The dashed lines are lines fitting to measured C_{dis} data represented by filled plots using Eq. (2.4.3).

5.4.3 Sheet resistance and mobility

The sheet resistance of pentacene MOS capacitors were calculated on the basis of method described in Sect. 5.4.2. Figure 5.8(a) shows the V_G dependence of R_{sh} for L_{dis} = 500 μm. Since the C–V characteristics at f = 100 Hz exhibits gradual change to V_G as seen in Fig. 5.6(a), the characteristic was used for the calculation of R_{sh}. The carrier mobility for the hole (μ) and V_0 values were estimated by fitting a curve to the plots of R_{sh} with Eq. (5.8). The plots are approximately on the dotted line obtained by the fitting. The agreement supports the validity of derivation process for Eq. (5.8).

Figure 5.8(b) shows mobilities μ_{sat}, μ_{lin}, and μ_I for pentacene TFTs, and μ for pentacene MOS capacitors. The μ values were calculated from the V_G dependence of R_{sh}, and were in the range of 0.48 to 0.64 cm^2/(V s). The average of μ was 0.55 cm^2/(V s). As shown in Sect. 5.4.1, the values of μ_{sat} and the value of μ_I were 0.84 and 0.63 cm^2/(V s), respectively. On the other hand, the average of V_{TH} for Eq. (2.1a), the value of V_{TH} for Eq. (2.4), and the average of V_0 for Eq.

(5.8) were −4.3, −4.2, −3.7 V, respectively. The ascending order for V_{TH} and V_0 corresponds to the order of μ_{sat}, μ_I, and μ. The difference among V_{TH} and V_0 may relate to difference among μ_{sat}, μ_I, and μ. Another possibility of the reason is the difference in lateral DC voltage in the channel layer. Drain current for calculation of the mobility in a TFT is measured under a condition that a DC voltage is applied to the drain electrode. On the other hand, capacitance for calculation of the mobility in a MOS capacitor is measured under a condition that no lateral DC voltage is applied to the channel layer. Thus, μ represents the intrinsic carrier mobility in the channel material under no static electric field.

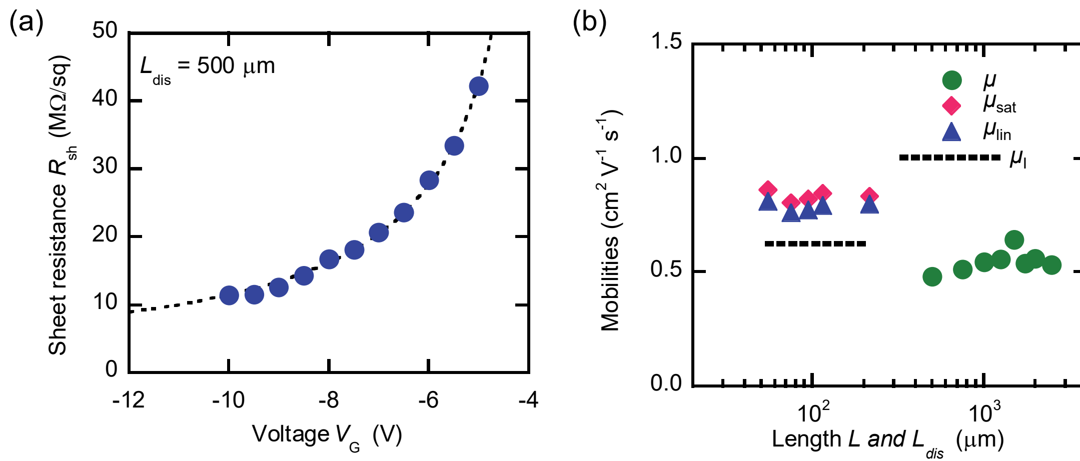


Figure 5.8: (a) Sheet resistance R_{sh} for pentacene MOS capacitors calculated from C–V characteristics; the dashed line is a line fitting to measured R_{sh} data (filled circle) using Eq. (5.8). (b) Mobility in the saturation regime (μ_{sat}; filled diamond) and in the linear regime (μ_{lin}; filled triangle) for individual pentacene TFTs; intrinsic mobility μ_I for pentacene TFTs (dashed line); carrier mobility μ for pentacene MOS capacitors (filled circle).

5.5 Summary

We investigated the capacitance characteristics of pentacene MOS capacitors with pentacene area uncovered with the top electrode. The frequency dependence of the capacitance was reproduced using an equation including a capacitance component based on a distributed constant circuit for the uncovered pentacene area. The sheet resistance for the uncovered pentacene area was calculated as a function of gate voltage from the measured capacitance. The mobility of a MOS capacitor with a different length of an uncovered pentacene area was estimated by fitting a curve to the gate voltage dependence of the sheet resistance. The mobility, which was in the range of 0.48–0.64 $cm^2/(V\ s)$, has no large dependence on the length. The mobility is considered as an intrinsic mobility evaluated under a condition of no static lateral electric field.

5.6 References

[1] J. S. Chang, A. F. Facchetti, and R. Reuss, IEEE Trans. Emerg. Sel. Topics Circuits Syst. **7**, 7 (2017).

[2] D. M. Taylor, Jpn. J. Appl. Phys. **55**, 02BA01 (2016).

[3] N. T. Kalyani and S. J. Dhoble, Renew. Sust. Energ. Rev. **16**, 2696 (2012).

[4] D. Volz, J. Photon. Energy **6**, 020901 (2016).

[5] R. Ganesamoorthy, G. Sathiyan, and P. Sakthivel, Sol. Energy Mater. Sol. Cells **161**, 102 (2017).

[6] A. Wadsworth, M. Moser, A. Marks, M. S. Little, N. Gasparini, C. J. Brabec, D. Baran, and I. McCulloch, Chem. Soc. Rev. **48**, 1596 (2019).

[7] L. Torsi, M. Magliulo, K. Manoli, and G. Palazzo, Chem. Soc. Rev. **42**, 8612 (2013).

[8] J. Liao, H. Si, X. Zhang, and S. Lin, Sensors **19**, 218 (2019).

[9] K. Takimiya, I. Osaka, T. Mori, and M. Nakano, Acc. Chem. Res. **47**, 1493 (2014).

[10] A. F. Paterson, S. Singh, K. J. Fallon, T. Hodsden, Y. Han, B. C. Schroeder, H. Bronstein, M. Heeney, I. McCulloch, and T. D. Anthopoulos, Adv. Mater. **30**, 1801079 (2018).

[11] C. Groves, Rep. Prog. Phys. **80**, 026502 (2017).

[12] N. Lu, L. Li, D. Geng, and M. Liu, Org. Electron. **61**, 223 (2018).

[13] M. Kitamura and Y. Arakawa, J. Phys.: Condens. Matter **20**, 184011 (2008).

[14] E. J. Meijer, G. H. Gelinck, E. van Veenendaal, B.-H. Huisman, D. M. de Leeuw, and T. M. Klapwijk, Appl. Phys. Lett. **82**, 4576 (2003).

[15] D. J. Gundlach, L. Zhou, J. A. Nichols, T. N. Jackson, P. V. Necliudov, and M. S. Shur, J. Appl. Phys. **100**, 024509 (2006).

[16] M. Kitamura, S. Aomori, J. H. Na, and Y. Arakawa, Appl. Phys. Lett. **93**, 033313 (2008).

[17] I. Torres, D. M. Taylor, and E. Itoh, Appl. Phys. Lett. **85**, 314 (2004).

[18] H. Hatta, Y. Miyagawa, T. Nagase, T. Kobayashi, T. Hamada, S. Murakami, K.

Matsukawa, and H. Naito, Appl. Sci. **8**, 1493 (2018).

[19] M. Yun, S. Gangopadhyay, M. Bai, H. Taub, M. Arif, and S. Guha, Org. Electron. **8**, 591 (2007).

[20] K. Gooden, A. Laudari, G. Knotts, and S. Guha, Flex. Print. Electron. **1**, 015004 (2016).

[21] W. T. Wondmagegn, N. T. Satyala, I. Mejia-Silva, D. Mao, S. Gowrisanker, H. N. Alshareef, H. J. Stiegler, M. A. Quevedo-Lopez, R. J. Pieper, and B. E. Gnade, Thin Solid Films **519**, 4313 (2011).

[22] M. Estrada, F. Ulloa, M. Ávila, J. Sánchez, A. Cerdeira, A. Castro-Carranza, B. Iñíguez, L. F. Marsal, and J. Pallarés, IEEE Trans. Electron Devices **60**, 2057 (2013).

[23] Y. Shao, Y. Zhang, W. He, C. Liu, T. Minari, S. Wu, M. Zeng, Z. Zhang, X. Gao, X. Lu, and J-M Liu, Semicond. Sci. Technol. **30**, 035005 (2015).

[24] A. Nigam, P. R. Nair, M. Premaratne, and V. R. Rao, IEEE Electron Device Lett. **35**, 581(2014).

[25] Md. Akhtaruzzaman, S. Ohmi, J. Nishida, Y. Yamashita, and H. Ishiwara, Jpn. J. Appl. Phys. **48**, 04C178 (2009).

[26] B. L. Anderson and R. Anderson, *Fundamentals of Semiconductor Devices* (McGraw-Hill Education, NY, USA 2018) 2nd ed. Chap. 7.

[27] B. H. Hamadani, C. A. Richter, J. S. Suehle, and D. J. Gundlach, Appl. Phys. Lett. **92**, 203303 (2008).

[28] F. V. Di Girolamo, M. Barra, V. Capello, M. Oronzio, C. Romano, and A. Cassinese, J. Appl. Phys. **107**, 114508 (2010).

[29] K.-D. Jung, C. A. Lee, D.-W. Park, B.-G. Park, H. Shin, and J. D. Lee, IEEE Electron Device Lett. **28**, 204 (2007).

[30] T. Hayashi, N. Take, H. Tamura, T. Sekitani, and T. Someya, J. Appl. Phys. **115**, 093702 (2014).

[31] C. Ucurum and H. Goebel, Microelectron. J. **44**, 606 (2013).

[32] D. M. Taylor and N. Alves, J. Appl. Phys. **103**, 054509 (2008).

[33] M. Ullah, D. M. Taylor, R. Schwödiauer, H. Sitter, S. Bauer, N. S. Sariciftci, and Th. B. Singh, J. Appl. Phys. **106**, 114505 (2009).

[34] H. Takahashi, M. Kitamura, Y. Hattori, and Y. Kimura, Jpn. J. Appl. Phys. **58**, SBBJ04 (2019).

[35] Y. Kimura, M. Kitamura, A. Kitani, and Y. Arakawa, Jpn. J. Appl. Phys. **55**, 02BB14 (2016).

[36] I. Torres and D. M. Taylor, J. Appl. Phys. **98**, 073710 (2005).

Chapter 6
Conclusions

Organic thn-film transistors (TFTs) have attracted attention because of their potential application to flexible, large-area, and low-cost electronic devices. In this thesis, threshold voltage and carrier mobility in organic TFTs were investigated. The threshold voltage control by oxygen plasma treatment was examined. In addition, the stability of threshold voltage on gate bias stress and the interface states introduced by oxygen plasma treatment were analyzed. Also, the carrier mobility without the influence of contact region was examined by using characteristics of metal-oxide-semiconductor (MOS) capacitors having a large uncovered semiconductor layer with top electrode.

The conclusion of each chapters is described as follows.

In chapter 3, the effect of oxygen plasma treatment of the SiO_2 gate dielectric on the characteristics of pentacene TFTs was investigated. The short-time plasma treatment enables the control of the threshold voltage without a large change in the mobility. In addition, the gate bias stress did not extinguish the threshold voltage change induced by oxygen plasma treatment. Oxygen plasma treatment is considered to be effective for threshold voltage control.

In chapter 4, the characteristics of pentacene MOS capacitors were investigated for evaluation of the interface states induced by oxygen plasma. The interface states between SiO_2 gate dielectric and pentacene were calculated from capacitance characteristics measured by two time-profiles of applied gate voltage. The interface state density distributed near the Fermi level of pentacene increased from 1.5 to 4.5×10^{12} /(cm^2 eV) with oxygen plasma treatment time. And, the interface state density distributed above the Fermi level of pentacene was in the range

of 1×10^{10} to 2×10^{11} /(cm^2 eV). The energy distribution of the interface states can be estimated from the characteristics of MOS capacitor measured by two time-profiles or applied gate voltage.

In chapter 5, the capacitance characteristics and mobility of pentacene MOS capacitors with pentacene area uncovered with the top electrode were investigated. The capacitance characteristics were analyzed by using an equation including a capacitance component based on a distributer constant circuit for the uncovered pentacene area. The mobility of a MOS capacitor with an uncovered pentacene area was calculated from analysis of them. The mobility, which was in the range of 0.48–0.64 cm^2/(V s), was slightly less than calculated mobility from TFTs. The mobility of a MOS capacitor with an uncovered pentacene area is considered as an intrinsic mobility evaluated under a condition of no static lateral electric field.

List of Publications

Scientific Journals Related to This Work

1. Yoshinari Kimura, Yoshiaki Hattori, and Masatoshi Kitamura, "Energy distribution of interface states generated by oxygen plasma treatment for control of threshold voltage in pentacene thin-film transistors", Journal of Physics D: Applied Physics (submitted).

2. Yoshinari Kimura, Yoshiaki Hattori, and Masatoshi Kitamura, "Evaluation of organic metal-oxide-semiconductor capacitors based on a distributed constant circuit", Japanese Journal of Applied Physics **59**, 036503 (2020).

3. Yoshinari Kimura, Yoshiaki Hattori, and Masatoshi Kitamura, "Voltage and Frequency Dependence of Capacitance Characteristics in Organic MOS Capacitors", 2019 Compound Semiconductor Week, 10.1109/ICIPRAM.2019.8819249.

4. Yoshinari Kimura, Masatoshi Kitamura, Asahi Kitani, and Yasuhiko Arakawa, "Operational stability in pentacene thin-film transistors with threshold voltages tuned by oxygen plasma treatment", Japanese Journal of Applied Physics **55**, 02BB14 (2016).

Scientific Journals Related to Other Work

1. Takumi Yoshioka, Hiroki Fujita, Yoshinari Kimura, Yoshiaki Hattori, and Masatoshi Kitamura, "Wide-range work function tuning in gold surfaces modified with fluorobenzenethiols toward application to organic thin-film transistors", Flexible and Printed Electronics **5**, 014011 (2020).

2. Yoshiaki Hattori, Yoshinari Kimura, Takumi Yoshioka, and Masatoshi Kitamura, "Data on optical microscopy and vibrational modes in Diphenyl Dinaphthothienothiophene thin films", Data in brief **26**, 104522 (2019).

3. Yoshiaki Hattori, Yoshinari Kimura, Takumi Yoshioka, and Masatoshi Kitamura, "The growth mechanism and characterization of few-layer diphenyl dinaphthothienothiophene films prepared by vacuum deposition", Organic Electronics **74**, 245 (2019).

4. Hajime Takahashi, Masatoshi Kitamura, Yoshiaki Hattori, and Yoshinari Kimura, "A ring oscillator consisting of pentacene thin-film transistors with controlled threshold voltages", Japanese Journal of Applied Physics **58**, SBBJ04 (2019).

5. Hajime Takahashi, Yuki Hanafusa, Yoshinari Kimura, and Masatoshi Kitamura, "Application of pentacene thin-film transistors with controlled threshold voltages to enhancement/depletion inverters", Japanese Journal of Applied Physics **57**, 03EH03 (2018).

6. Asahi Kitani, Yoshinari Kimura, Masatoshi Kitamura, and Yasuhiko Arakawa, "Threshold voltage control in dinaphthothienothiophene-based organic transistors by plasma treatment: Toward their application to logic circuits", Japanese Journal of Applied Physics **55**, 03DC03 (2016).

International Conference Related to This Work

1. Yoshinari Kimura, Yoshiaki Hattori, and Masatoshi Kitamura, "Voltage and Frequency Dependence of Capacitance Characteristics in Organic MOS Capacitors", Compound Semiconductor Week 2019 (CSW2019), May 19-23, 2019, TuP-J-4.

2. Yoshinari Kimura, Masatoshi Kitamura, Asahi Kitani and Yasuhiko Arakawa, "Operational

stability in pentacene thin-film transistors with threshold voltages tuned by oxygen plasma treatment", 5th International Symposium on Organic and Inorganic Electronic Materials and Related Nanotechnologies (EM-NANO 2015), June 16-19, 2015, OA1-O-3.

3. Yoshinari Kimura, Masatoshi Kitamura, and Yasuhiko Arakawa, "Pentacene thin-film transistors with controlled threshold voltages and their application to pseudo CMOS inverters", International Conference on Solid State Devices and Materials (SSDM2014), September 8-11, 2014, K-8-1.

4. Yoshinari, Kimura, Kazuma Katsuki, Masatoshi Kitamura, and Yasuhiko Arakawa, "Threshold voltage control by oxygen plasma treatment", The 40th International Symposium on Compound Semiconductors (ISCS2013), May 19-23, 2013, MoPC-09-04.

International Conference Related to Other Work

1. Hiroki Iwata, Kouta Iwasa, Yoshinari Kimura, and Masatoshi Kitamura, "Current Stability in SnO_2 Thin-Film Transistors with Ultra-Thin Channel Layers toward Gas Sensor Application", 7th International Workshop on Epitaxial Growth and Fundamental Properties of Semiconductor Nanostructures (SemiconNano2019), September 24-27, 2019, P-15.

2. Kouta Iwasa, Hiroki Iwata, Yoshinari Kimura, and Masatoshi Kitamura, "A *p*-Channel SnO_x Thin-Film Transistor with a SiO_2 Passivation Layer", 7th International Workshop on Epitaxial Growth and Fundamental Properties of Semiconductor Nanostructures (SemiconNano2019), September 24-27, 2019, P-14.

3. Hiroki Fujita, Yoshinari Kimura, Yoshiaki Hattori, and Masatoshi Kitamura, "Bottom-Contact Pentacene Thin-Film Transistors with Threshold Voltages Controlled by Oxygen

Plasma Treatment", International Conference on Solid State Devices and Materials (SSDM2019), September 2-5, 2019, PS-7-16.

4. Yuki Matsuda, Yoshinari Kimura, Yoshiaki Hattori, and Masatoshi Kitamura, "Surface properties of oriented polytetrafluoroethylene films with a micrometer pitch", 10th International Conference on Molecular Electronics & Bioelectronics (M&BE10), June 25-27, CP2-06.

5. Yoshiaki Hattori, Yoshinari Kimura, and Masatoshi Kitamura, "Nucleation and shape of 2D islands of DPh-DNTT thin-films prepared by vacuum evaporation", Compound Semiconductor Week 2019 (CSW2019), May 19-23, 2019, ThE-1-5.

6. Shotaro Watanabe, Yoshinari Kimura, Yoshiaki Hattori, and Masatoshi Kitamura, "Thin-Film Transistors Based on Copper Phthalocyanine Deposited on a Gate Dielectric Rubbed with Poly(tetrafluoroethylene)", Compound Semiconductor Week 2019 (CSW2019), May 19-23, 2019, TuP-J-2.

7. Yoshiaki Hattori, Yoshinari Kimura, Takumi Yoshioka, and Masatoshi Kitamura, "Growth Mechanism and Electrical Characterization of DPh-DNTT Films Prepared by Vacuum Deposition", International Conference on Solid State Devices and Materials (SSDM2018), September 9-13, 2018, K-8-05.

8. Hajime Takahashi, Masatoshi Kitamura, Yoshiaki Hattori, and Yoshinari Kimura, "Logic Circuits Consisting of Pentacene Thin-Film Transistors with Controlled Threshold Voltages", International Conference on Solid State Devices and Materials (SSDM2018), September 9-13, 2018, K-5-03.

9. Asahi Kitani, Yoshinari Kimura, Masatoshi Kitamura, and Yasuhiko Arakawa,

"Dinaphthothienothiophene thin-film transistors with threshold voltage shift induced by oxygen plasma", 8th International Conference on Molecular Electronics and Bioelectronics (M&BE 8), June 22-24, 2015, A-P08.

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